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# Low Power Design Methodologies

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***Abstract:*** ***With the demand of addition of more and more system on chip, the number of transistors are getting added which leads to the increase in power dissipation in the devices. Recently, due to the continuous scaling of feature size, a massive development has been taken place in the field of portable devices. Two main features of low power design are battery lifeline (especially in portable devices) and reliability Present electronics market is full of battery operated highly complex gadgets and multifunctional portable devices. The power consumption in these devices has become the pivotal constraint. The main objective of this paper is to focus on various perspectives of low power design in VLSI circuits.***
***Keywords: low power VLSI, Device scaling, MTCMOS, DTMOS, Power dissipation***

## I. INTRODUCTION

The increased demand of portable devices led the researchers to concentrate on low power design, rather than in the field of VLSI design to meet out the emerging challenges of twenty first century electricity. The power consumption in VLSI circuits can be explored at different levels of abstraction starting from the lowest i.e., device level, circuit level, logic level, block level, architecture level and up-to system level. Power optimization techniques at the higher level requires, dedicated study of the application considered for optimization. Whereas power optimization techniques applied at the lower levels (circuit and device level) can be generally applied to any circuit. At the device level, due to the advancements in the semiconductor technology, power consumption is reduced, but the fabrication cost is increased. Several techniques have been proposed for low power design at circuit level, including Clock Gating], Transistor Sizing, Gate Reorganization, Pre-computation logic.

## II. NEED FOR LOW POWER VLSI

As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation. New generations of processing technology are being developed while present generation devices are at a very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integration circuits. Another factor that fuels the needs for low power chips is the increased market demand for portable consumer electronics powered by batteries. Limited battery life, higher operating frequency, increased chip density and packaging problems are some main factors which causes the researchers to shift their mind from high speed to low power design

## III. SOURCES OF POWER DISSIPATION

Sources of power dissipation in CMOS circuits can be divided into two categories: Dynamic power consumption and Static power consumption, i.e.

$$P_{total} = P_{dynamic} + P_{static} \quad [1]$$

1) *Dynamic Power:* There are three main components of dynamic power dissipation. First is switching power second is short circuit power and the third is power consumption due to unwanted glitches presents in digital circuits.

$$P_{dyamic} = P_{switching} + P_{short\text{-}circuit} + P_{glitching} \quad [2]$$

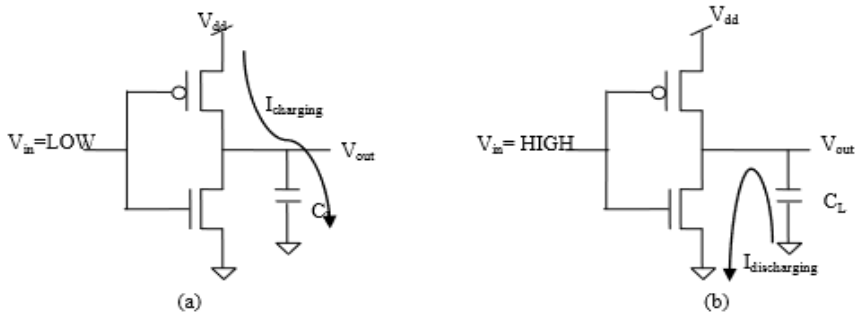



Fig 1: Basic CMOS Inverter (a) Charging Mode (b) Discharging Mode

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2) *Switching Power:* The dynamic power consumption occurred due to the switching activities of the logical inputs from logic HIGH to LOW or vice-versa. All logical switching activities provide the foundation for internal capacitive nodes to either charge from 0V to Vdd through pull-up network or to discharge the nodes from Vdd to ground through pull-down network. This charging and discharging action is shown in figure 1 using basic CMOS inverter. Charging activity draws current from the power supply, whereas discharging action flows current from node to ground and hence the power is consumed. The average power being delivered by charging and discharging circuitry is given by

$$P = CV^2_{dd}f \qquad [3]$$

3) *Short Circuit Power:* When input voltage of CMOS inverter is greater than Vthn of NMOS then, NMOS transistor will be in ON state and when input voltage is less than (Vdd - Vth)) then, PMOS transistor will be in ON state. Short circuit power in CMOS circuits represents the power consumed during a condition in which both PMOS and NMOS logic is in ON state. When input switches (from LOW to HIGH or vice versa), there is a short duration for which input level lies between Vthn and (Vdd - Vthp) and both transistors turned ON. A short circuit path is established between Vdd and ground so that, short circuit current will flow which causes power consumption.

4) *Glitching Power:* The glitching power is another form of dynamic power consumption, which includes both power consumption due to switching and power consumption due to short circuit. Power consumption due to glitch generally occurs when output of a logic circuit changes momentarily changes its state before going into steady state. This is a condition occurs when more than two inputs has changes their state. For example in the figure 1, if input changes from "111" to "010", output jumps to logic HIGH for a moment and then come back to logic LOW level. Presence of glitch at the output is the result of unequal rise and fall delay of logic gates at different level. Problem of glitch can be resolved by applying proper logic optimization technique to the circuit i.e., by latching the outputs and synchronized it with a clock signal, so that inputs to the next block are synchronized. The glitching power is given by

$$P_{glitch} = V^2_{dd} C_L f_{glitch} \qquad [4]$$

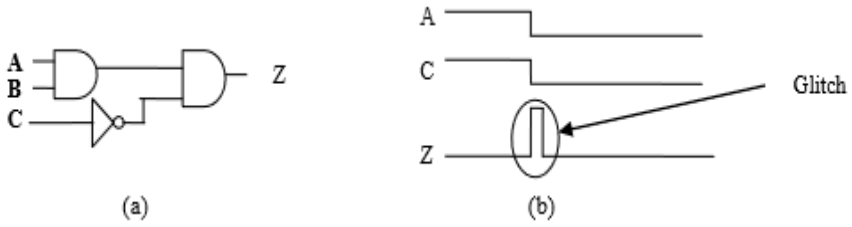



Fig 2: Glitch (a) Example circuit (b) Input- Output waveform showing glitch

5) *Leakage Power-* is due to the sum of all the currents which is flowing through the MOS device in standby mode. Due to the regular scaling of supply voltage, the threshold voltage is also decreased, where the design enters into the sub-threshold region. Leakage power is a result of leakage current that flow from the gate oxide and p-n junctions. The three main components of leakage current in MOS are sub-threshold leakage, gate leakage and source to body or drain to body reverse biased leakage current. Sub threshold current is also known as weak inversion conduction current, which flows between drain to source when gate voltage is below Vth. Due to regular scaling of MOS devices sub threshold leakage current leads the total power consumption due to leakage. Gate leakage current is due to the direct tunnelling of electrons or holes from substrate to the gate terminal.

## IV. LOW POWER DESIGN METHODOLOGIES

### A. *Dynamic Power Reduction Techniques*

Dynamic power consumption is directly proportional to the capacitance C, square of the supply voltage $V_{dd}$ and operating frequency f. Hence for minimizing the dynamic power consumption, it is needs to minimize the parameters C, $V_{dd}$ and f. merely decreasing these parameters is not a solution to power consumption problem. It is big a challenging issue for the designers, as it degrades the system performance and leading to increasing delay

1) Device Scaling The basic idea of scaling is to reduce the dimensions of MOS devices and the connecting wires in the circuits. Scaling achieves the same electric field pattern in the smaller transistors by reducing the applied voltage, also with the thickness of the oxide layer; this is known as voltage scaling In constant E-field scaling, the dimensions, voltage and doping concentration are all modified by a common factor α. Constant E-field scaling results in increase in chip density by $\alpha^2$, as the length of the connecting wires & device dimensions are reduced. The speed of the small device is improved by a factor of α

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because capacitance C of the every node is now decreased. Therefore the power dissipation per circuit is reduced by a factor $\alpha^2$. In constant voltage scaling, the device dimensions are scaled by the scaling factor α, while the supply voltages and terminal voltages are kept constant. Constant voltage scaling results in the increase in drain current same factor and decrease in the delay by $\alpha^2$ with an increase in the power dissipation of the device.

*2)* Transistor Sizing is an effective and efficient circuit level low power design technique. Sizing the transistor up or down to achieve desired circuit/system performance is one of the important techniques of low power design. Transistor sizing can be used to reduce dynamic power consumption by reducing the junction as well as overall gate capacitance of the circuit. It is also important to minimize the circuit area with minimized power consumption and high performance level. Transistor reordering is used together with the transistor sizing. In this technique, switching power is reduced by reordering the transistors connected in a serial mode

*3)* Pre-computation logic: The basic principle of pre-computation logic is that the designer has to provide a block that selectively pre-compute the output logic values before one clock cycle prior to their requirement, and then use these pre-computed values to reduce internal activities. This reduces the switching capacitance and hence the dynamic switching power is reduced

*4)* Clock gating has been proved as an efficient and effective technique for power saving in synchronous circuits. By shutting down the inactive portion of the large synchronous circuit, lots of power can be saved. Clock gating is also helpful in reducing the glitching power by stopping redundant inputs to apply to the circuit

### *B. Static Power Reduction Techniques*

With the technology scaling, due to the reduced channel length, static power consumption becomes more significant problem than dynamic power consumption. Lower threshold voltage in CMOS circuit will result in increase in leakage current. Due to this, leakage power turned out to be an important portion of the total power consumption. Various techniques have been proposed by researchers to reduce leakage power reduction techniques at circuit level.

*1)* Drain gating is another important technique of leakage current reduction. In this technique, series connected PMOS and NMOS transistors acting as sleep transistor are inserted between pull-up and pull-down networks. Problem of state voltage reduction is removed using drain gating.

*2)* Multithreshold CMOS (MTCMOS) technique to reduce leakage power involves the use of HIGH threshold MOS devices for sleep transistor, whereas the LOW threshold MOS devices are used to implement the logic circuit. Logic circuits with LOW threshold voltage are fast but have high sub threshold leakage current while logic circuits with HIGH threshold voltage are slower and have much reduced sub threshold leakage currents. The leakage power in standby mode is reduced due to the HIGH threshold sleep transistors and in active mode performance of the circuit is maintained by LOW threshold devices in logic circuit.

*3)* Dual Threshold MOS (DTMOS) Use of dual threshold is another important technique to reduce leakage current. However this technique is based on the capability of circuit designer to search out the critical and non-critical paths between input and output. In dual threshold MOS technique, low threshold voltage is used for transistors present in critical path to maintain the performance, while the high threshold is used for non-critical paths to reduce the leakage current and hence the leakage power.

### *C. Architecture level Low Power Design*

At architecture level, it becomes important to reduce system clock frequency and to decrease the number of critical paths, so that number of transitions can be reduced. Dynamic power management (DPM) is another low power design methodology that dynamically reorganizes the system such that the requested services and performances can be achieved with minimum number of active components

## V. CONCLUSIONS

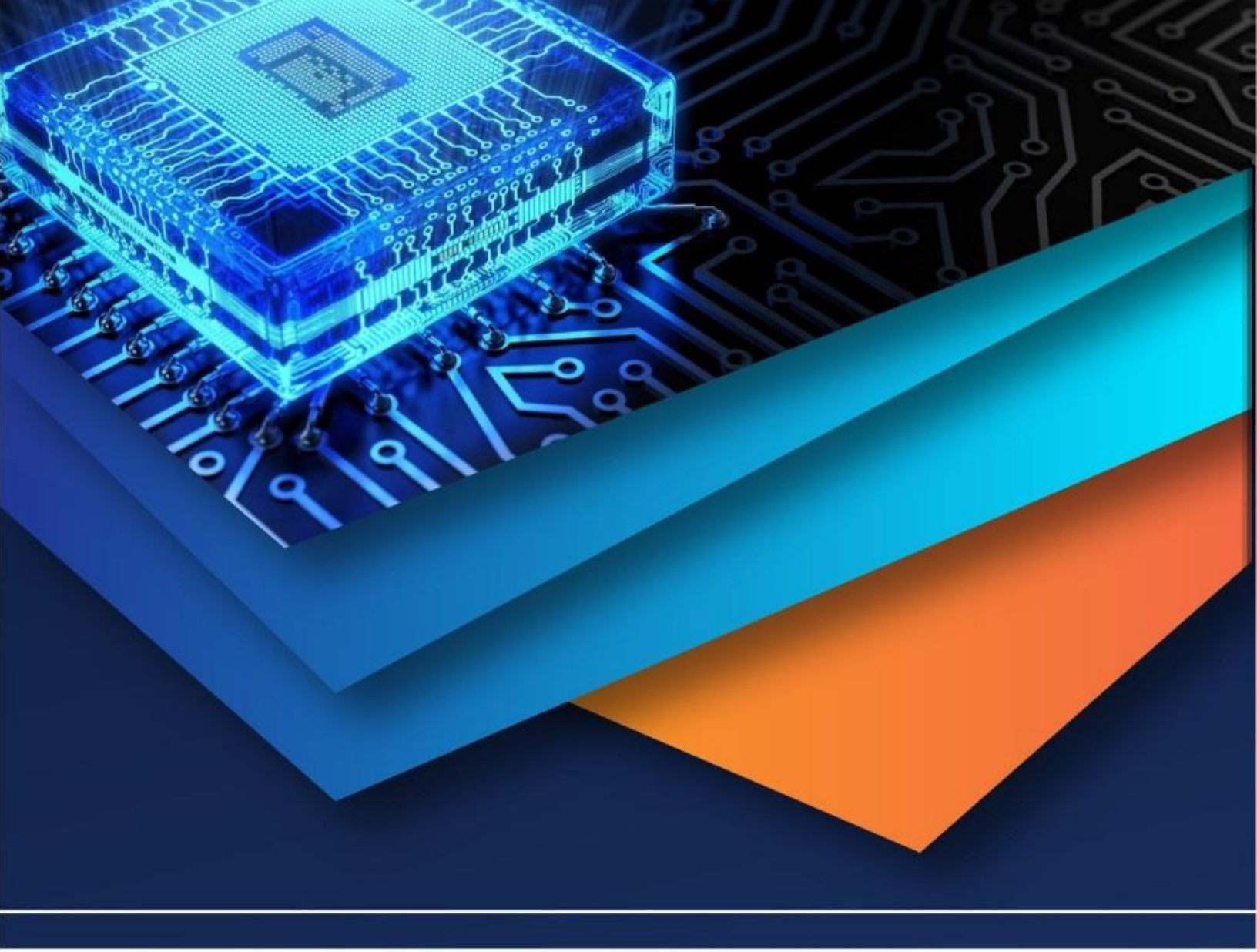
Power dissipation in CMOS VLSI circuits has been considered as an important factor for the low power VLSI design. In this paper the different design techniques are discussed for different abstraction level. At circuit level and device level, transistor sizing and device scaling are the effective techniques to reduce power. Clock gating, precomputation logic and dynamic power management are the techniques to reduce power dissipation at gate/architecture-level design.

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