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10-20 GHz CMOS Low Noise Amplifier with Coplanar Line for Wireless Communication

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Abstract*—Recently, CMOS amplifiers remain to be challenge at radio frequencies. In this paper, a 10-20GHz CMOS Low noise amplifier (LNA) with 50Ω matched coplanar line is proposed. This new technique may improve the integration level and enhance the performance of existing amplifier devices. Architecture of LNA is designed using CMOS 90nm TSMC design kit and simulated in ADS v.11 platform. According to simulation results, CMOS LNA resonates at 14GHz and 16.5GHz within wideband of 10-20 GHz frequency and achieves return loss of -24dB, with forward gain of 15.7dB. The best achievement of LNA architecture is obtaining low noise figure of 2.8dB.
Keywords*— CMOS LNA, Noise figure, Coplanar waveguide line (CPW)

I. INTRODUCTION

The fastest growth of wireless communication industry is establishing a big new market opportunity. Current researchers are searching new solutions everyday that would be implemented into the existing wireless system network for providing broader bandwidth, high quality and new value added services [1]. The extensive progress of complementary metal oxide semiconductor (CMOS) technology has enabled its application in Ku band based receivers. The Ku band is a portion of the electromagnetic spectrum in the microwave range of frequencies ranging from 11.7 to 12.7GHz downlink frequencies and 14 to 14.5GHz uplink frequencies. Ku-Band communication is used in Ultra Low Noise Amplifiers which are specially designed for satellite earth station and other telecommunications applications. Ku-band Low Noise amplifier is designed to fully match a 50Ω input and output impedance. The driving designs criteria for the LNA is the maximization of its gain. Secondly the noise figure has to be as good as possible, with a very small compromise on gain. Due to the gain criteria, the input and output match are also optimized. Stability wise the LNA has to be unconditionally stable over very broad frequency range [2]. In terms of linearity, the system analysis does not impose stringent requirements. Moreover, the CMOS technology is one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [3].
In radio frequency (RF) receivers, the input signal from the receiving antenna first passes through band pass filter to the low noise amplifier (LNA) that amplifies the signal suppressing noise contributed from preceding stages [4-5]. Hence, a good impedance matching is essential for low noise figure and high gain required by the receiver system for achieving system reliability. In present scenario, a 10-20GHz two stage common gate-common source (CG-CS) LNA is designed using 90nm CMOS technology which achieves more than 10dB gain with good reverse isolation parameter enough to prove system reliability.

II. ANALYSIS OF COPLANAR WAVEGUIDE LINE

Coplanar Waveguide (CPW) is an alternative to microstrip and Strip line that place both the signal and ground currents on the same layer. The conductors formed a center strip separated by a narrow gap from two ground planes on either side. The dimensions of the center strip, the gap, the thickness and permittivity of the dielectric substrate determined the effective dielectric constant, characteristic impedance and the attenuation of the line. The gap in the coplanar waveguide is usually very small and supports electric fields primarily concentrated in the dielectric. In CPW the characteristic impedance is determined by the ratio of the centre strip width W to the gap width s, so size reduction is possible without limit, the only penalty being higher losses. This makes the design of a CPW line with particular impedance unique because an infinite range of W and s values will result in a specific impedance requirement. Now Fig1. Shows layout of CPW line with 50Ω source and load which achieves wide band of 5GHz within range of 13.9 to 18.5 GHz. Using these CPW lines in CMOS LNA for looking wideband configuration. The detail explanations of CMOS LNA with CPW line are shown in next section.

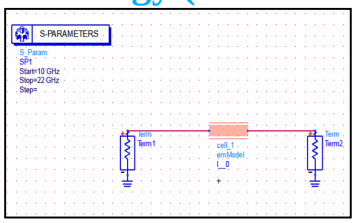

Fig1. Layout of coplanar waveguide line

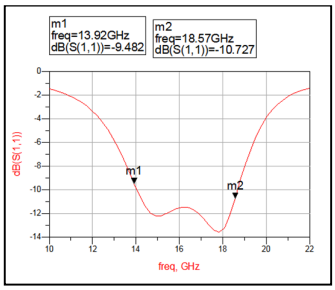

Fig2. Return loss Vs Frequency

III. DESIGN ANALYSIS OF CMOS LNA WITH CPW

According to the requirements of LNA design, different topologies like common source (CS), Common Gate (CG) etc. could be used for performance parameters which are briefly discuss below.

A. CG-CS Topology

The common source (CS) and common gate (CG) LNA topologies are one of the most popular design choices which are widely used to LNA. The CS with the source inductor degeneration technique can be achieved higher gain with the ideal noiseless components and gives minimal noise figure whereas common gate offers wideband operating performance with good linearity and input-output isolation property [6]. The parasitic capacitance of the transistor degrades the CG LNA performance for high frequencies. This problem can be address by connecting the first stage of CGLNA with the similar next stage through a bonding wire and achieving the broadband operating performance as well holding the beauty of original CGLNA architecture [7-9]. Hence, a CGLNA is designed for achieving good reverse isolation with 50Ω proper impedance matching. Another single stage of CSLNA is added to the CG design through a coplanar waveguide (CPW) providing low noise and high gain characteristics.

B. Circuit Design

Fig.3 shows proposed schematic of CG-CS LNA. A 10-20GHz two stage CMOS LNA design using 90nm commercial TSMC design kit in Agilent™ advanced design system. The two stages of CGLNA is composed of CPW1, C_{in} and dc power of V_{GG1}, V_{GG2} with low Q factor are analyzed and achieve a good reverse isolation and input impedance of 50Ω calculated by equation (1) and (2). Selecting on-chip inductor is the key to design a matching network, because it determines the quality of the matching network.

$$Zin = \frac{1}{g_m + j\omega C_{gs}} \qquad (1)$$

$$S_{11} = 20.log_{10}\left(\left|\frac{Z_{in-}R_S}{Z_{in} + R_S}\right|\right) \qquad (2)$$

Where g_m is transconductance, ω is operating frequency and C_{gs} is gate to source capacitance. To overcome the loss parameters (like noise figure, gain, etc.), the next stage i.e. CS with source degeneration is used thus achieving best gain. The cascode topology is used to reduce the miller effect, improving the stability to achieve higher gain. The input-output match is accomplished with a LC impedance transformation network. Two 208-fF output capacitors in series are implemented to desensitize the process variation. Parasitic capacitance of input and output RF bond pads is also considered in the circuit simulation. The chosen design specifications and technologyof MOS transistors under low supply voltage of 1.8V for the simulation are shown in Table1.

Table 1 show components values of CG-CS LNA

	Device Width (µm)	Length (µm)	Biasing (V)
M1	36	.09	0.93
M2	21	.09	0.92

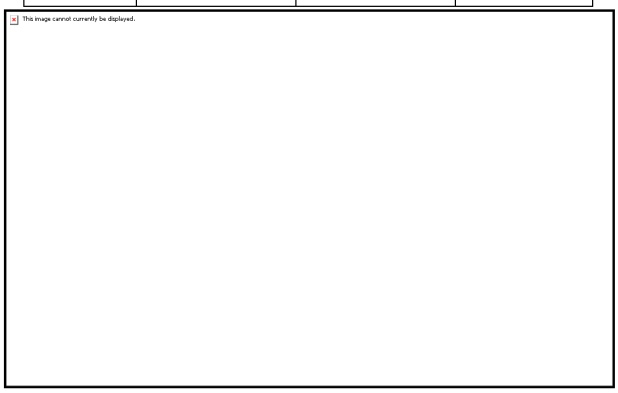

Fig.3 Schematic circuit of CG-CSLNA at 10-20GHz

IV. SIMULATION AND DISCUSSION

According to previously discussed the analysis of LNA, we have check the performance of complete design with the support of simulation tool in ADS2011. To optimize the design it is necessary to determine the specification of the CG-CS LNA by an accurate system simulation. For maximum signal transfer, input of the wideband LNA should provide an impedance of 50Ω to match with output impedance of antenna. In LNA design there is tradeoff between the best input match and lowest noise figure. Owing to the necessary for Ku band frequency operation, the source inductor value is quite small. In our case, the value of the inductor is chosen about 1nH. The quality factor is about 9.3 for Ku band, the inductance value is quite match for simulation. The input and output matching by the way of high impedance co-planar waveguide line with λ/4 wavelength is used in the above figure. When LNA is operating at the Ku band, it has around -10dB input reflection and the lowest value of VSWR of 1.2 at 14GHz and 1.3 at 16.5GHz within band range of 10-20GHz wide bandwidth. A high gain of 15.7dB and around 2.8dB approximately flat noise figure is achieved in this work. It well known that if we design a receiver system needs a high gain for passes the signal from antenna to the RF connector of end port of LNA. All simulation results of receiver system are also given below in Figs 4-7 respectively.

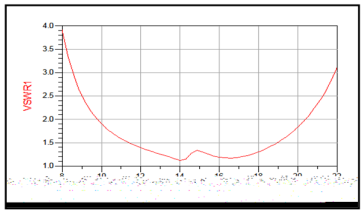

Fig.4 Return loss Vs frequency

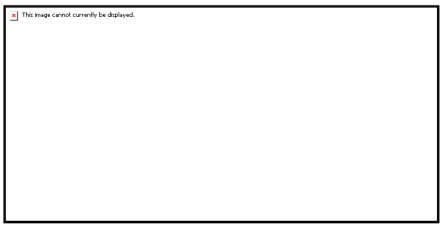

Fig.5 Input impedance Vs frequency

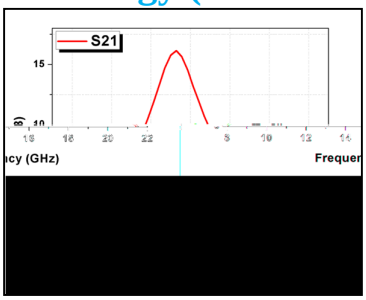

Fig.6 Gain Vs frequency

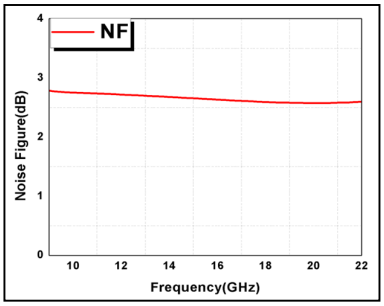

Fig.7 Noise Figure Vs frequency

V. CONCLUSION

A 10-20GHz LNA is designed for Ku band applications based on CMOS technology. The double-ended two stages of LNA are designed using 90nm CMOS. Performance standards are met for this new tri-design technique. Simulation results of the designed circuit signify a gain of 15.7dB, noise figure of 2.8dB, $S_{11}$of –24dB and with DC power dissipation 25mW under 1.8V power supply. The proposed method of receiving system for Ku band applications, increase the level of system integration, reducing chip area size thus escalating the overall system gain.

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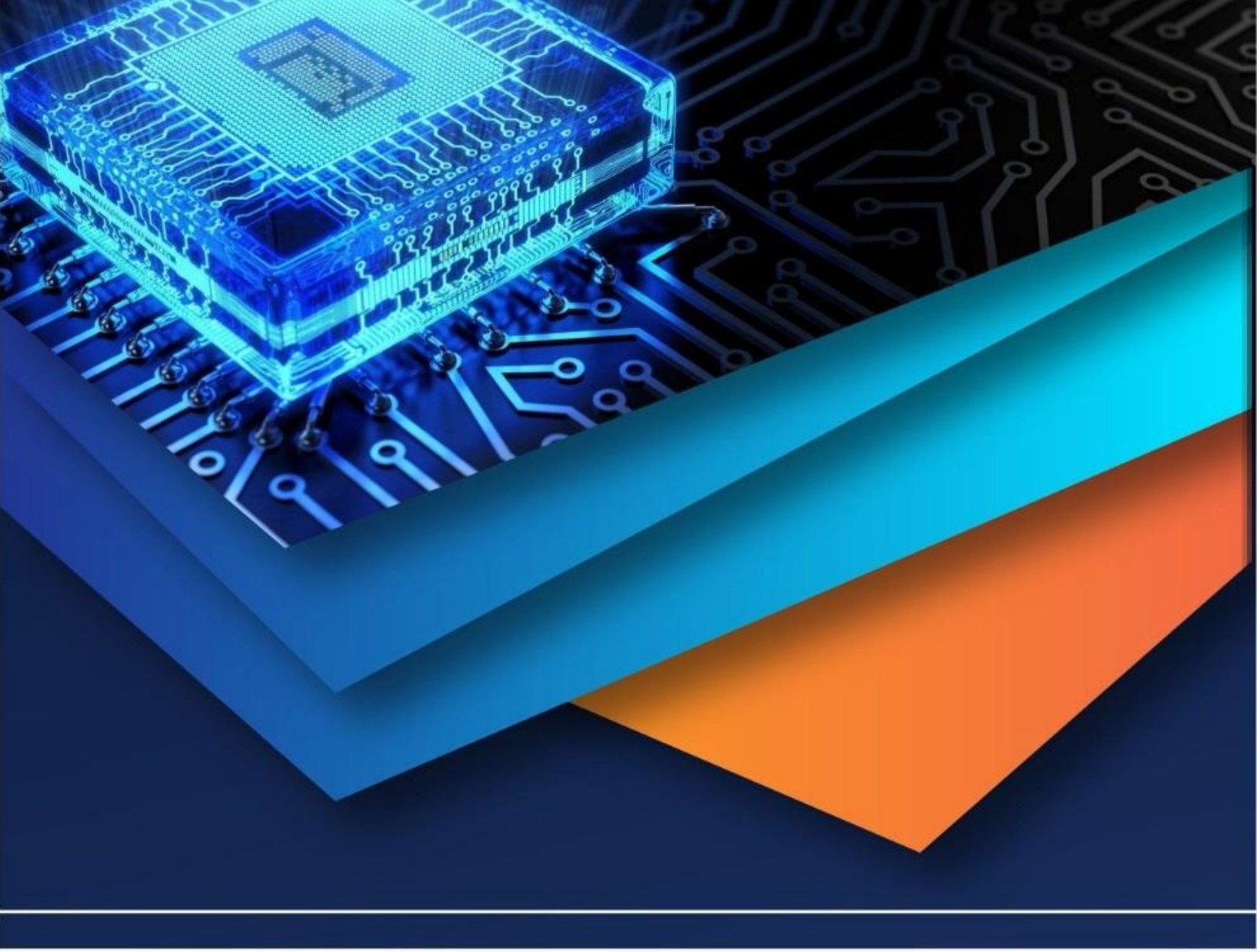

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