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Design and Simulation of Low Power 10T Full Adder using Cadence 16nM Technology

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Abstract: ***This paper presents the design of low voltage low power 10T full adder with minimum leakage power, and its transient analysis with cadence tools. Adder is the basic building block of Arithmetic in digital circuits, the area and power consumption of adder plays a vital role in portable devices. The low voltage low power full adder circuits are widely used in portable applications as it improves the battery lifetime. In this paper we have presented the design, simulation and comparative analysis of 27T and 10T full adder topologies with various supply voltages and lower technology node at Cadence Virtuoso TSMC 16nM technology.***

Keywords: Adder, Full-Adder, 10T Full-Adder, Cadence, Low Voltage, Low Power, TSMC 16nM.

I. INTRODUCTION

Due to increase in portable devices, VLSI research is more trending towards the miniaturization, scaling down the size of transistors leads to lot of challenges like leakage current, but the benefits are less area, low voltage, and low power. Today technology comes from micrometre to nanometre with reducing the length of gate. In this paper we have considered the 16nM TSMC technology libraries, by using lower technology we can achieve the higher densities.

For any digital devices like Microprocessors, Microcontrollers, Digital Signal Processors an Adder is the basic building block, for all the arithmetic operations in ALU's adders are used, 1bit full adder is the basic cell which is used in comparators, Integrators, Differentiators, Multipliers. They are also used in DSP transformations like FFT, IFT computations. In image processing also adders are used for pixel additions, Bayer's patterns etc. So, the miniaturization of Adder size will increases the density.

We know that the power consumption has the nonlinear (square) relation with the supply voltage, hence power consumption of the circuit can be minimized by reducing the power supply or operating at the lower voltages. In this paper we have made a comparative analysis for the supply voltage of 1.8v and 0.8v with two topologies.

There are many research papers presented in different types of topologies for full adder based on logic expressions and different logical structures, in this paper we are concentrating on 10T full adder circuit as our main concern is area, and power consumption.

This paper consists of five sections, Section I gives the Introduction, Section II gives the block diagram, and information about full adder, Section III gives the circuit diagram and simulation results, Section IV gives the conclusion and future scope, then followed by acknowledgement and references.

II. BLOCK DIAGRAM OF FULL ADDER

A one bit half adder takes two one bit signals and generates two one bit outputs sum and carry, where as one bit full adder is a device which takes A, B as inputs, in additional carry C_{in} also as an input and generates outputs as sum and carry out. The block diagram of 1bit full adder is given by,



Fig. 1 Block diagram of full adder

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A. Equations for 1 Bit Full Adder

The equations of the full adder is given by

1) For SUM

$$SUM = A \oplus B \oplus C_{in}$$

(Or)

$$SUM = (A \oplus B) \oplus C_{in}$$

2) For Carry

$$C_{out} = AB + BC_{in} + C_{in}A$$

(Or)

$$C_{out} = A.(A \oplus B)\text{“} + (A \oplus B).C_{in}$$

The full adder can be implemented by using two half adders (with the help of above equations) such as shown in below figure.2,

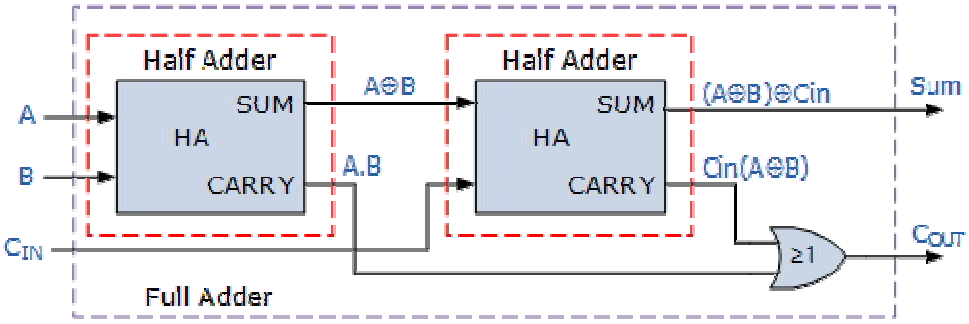


Fig. 2 Full adder using two half adders

The full adder can be implemented by using a multiplexor and ex-or gates as,

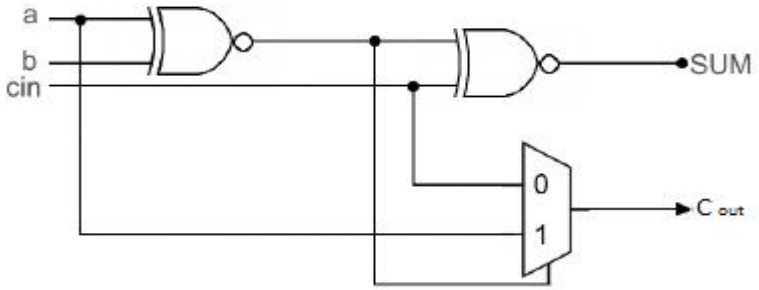


Fig. 3 Full adder using two half adders

The truth table of the one bit full adder is given by

TABLE I
TRUTH TABLE OF 1-BIT FULL ADDER

Inputs			Outputs	
A	**B**	**C_{in}**	**Sum**	**C_{out}**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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III.CIRCUIT DIAGRAM & TRANSIENT ANALYSIS

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A. Circuit Schematics

The full adder circuit schematic in cadence virtuoso for 27 transistors topology is given by

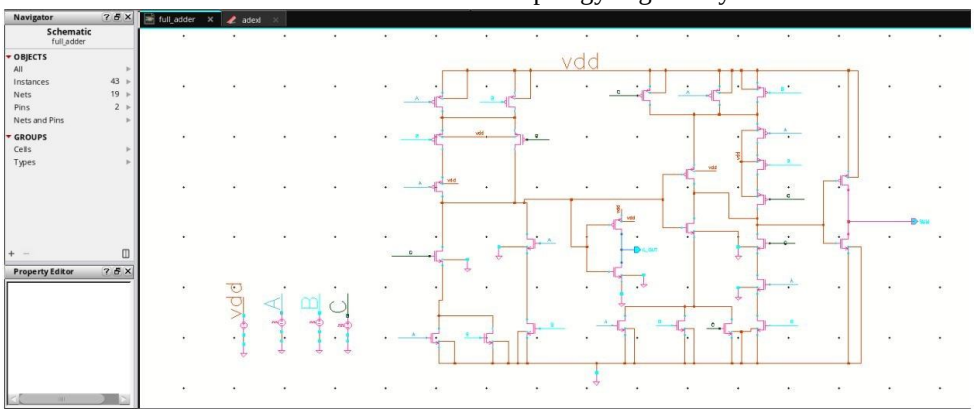


Fig. 4 Full adder 27T schematic

The full adder circuit schematic in cadence virtuoso for 10 transistors topology is given by

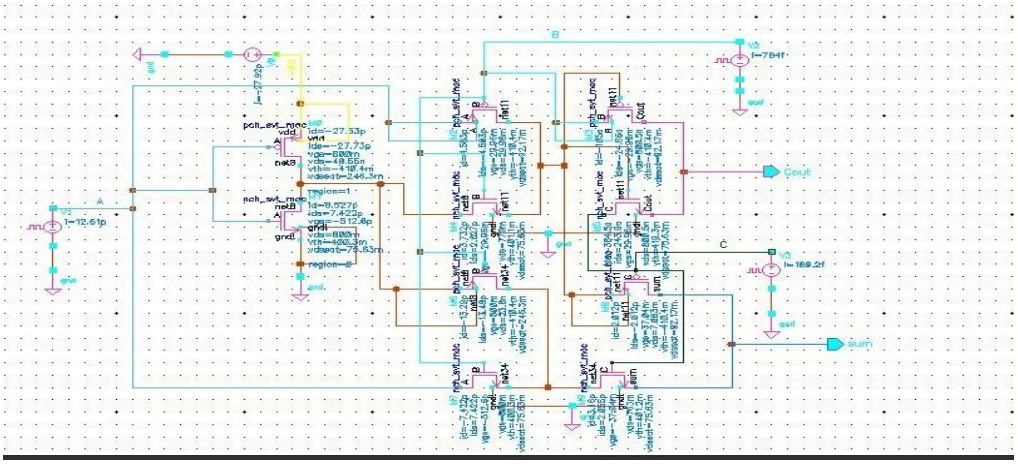


Fig. 5 Full adder 10T schematic

B. Transient Analysis

Simulation waveforms of 27T is given by

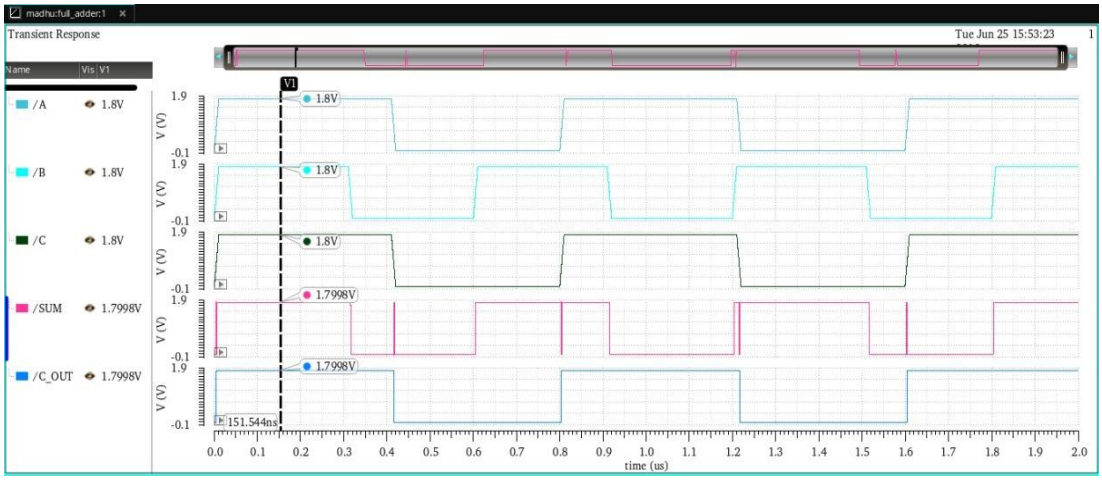


Fig. 6 Transient analysis of 27T full adder

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Simulation waveforms of 10T is given by

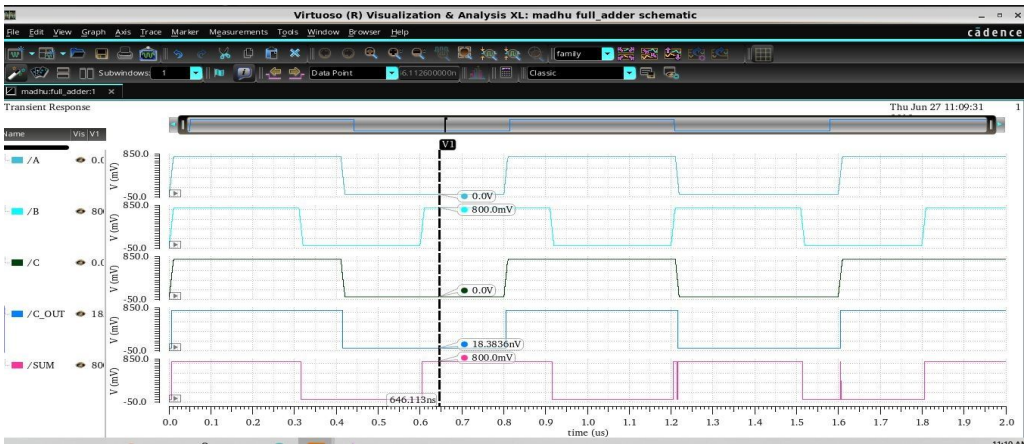


Fig. 7 Transient analysis of 10T full adder

C. Comparative Analysis

The comparative analysis of the above two topologies and also with respect to pervious published journals given by the following table.

TABLE II
Comparative analysis of Power Consumption

S.No	Topology	Full Adder Topologies			
		Number of transistors	Technology	Supply Voltage	Power Consumption
1	10T Full Adder [2]	10	45nM	1V	39.29pW
2	27T Full Adder	27	16nM	1.8V	1.2uW
3	10T Full Adder	10	16nM	0.8V	22.34pW

IV. CONCLUSION & FUTURE SCOPE

In this paper we have presented a low voltage low power 10T full adder using cadence TSMC 16nM technology, with power consumption of 22.34pW and also compared with the recently published journals. As the research increases further we are looking forward to work on circuits with Cadence 7nM technology for miniaturization of integrated circuits, low-power and portable applications.

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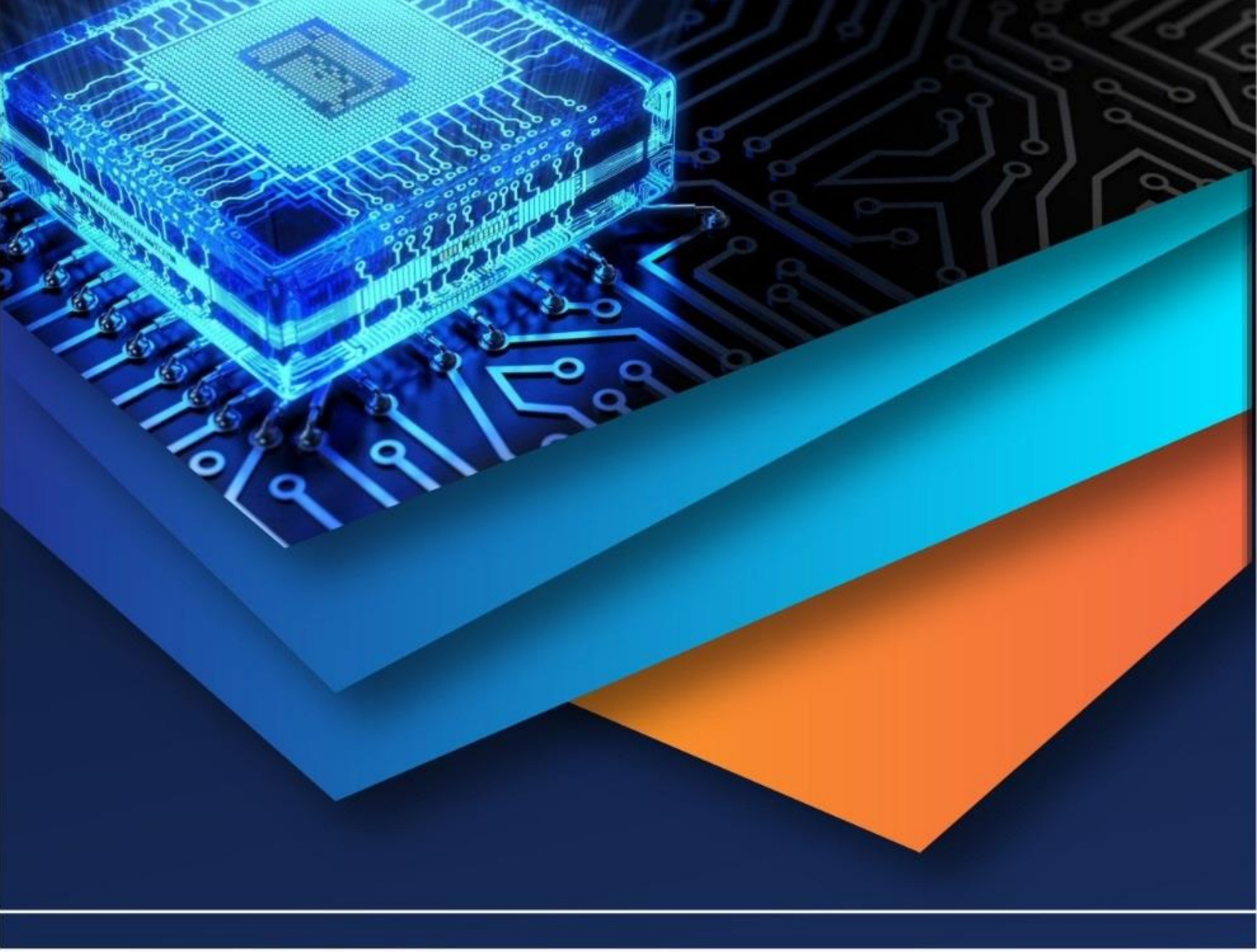
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