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Simulation and Analysis of LG SOI TFET

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***Abstract:** In this paper, LG SOI TFET is proposed and simulated. The tunneling junction in the LG SOI TFET is perpendicular to the channel direction that facilitates the implementation of a relatively large tunneling junction area which leads to increase in the drain curent. The channel is mainly distributed in the vertical direction, reducing the device area. This device feature high current drivability and abrupt on-off transition. The proposed LG SOI TFET shows higher on-current (I_{ON}). All the simulation is performed by using Sentaurus TCAD including nonlocal BTBT model.*

***Keywords:** Tunnel Field Effect Transistor (TFET), L-Shaped Gate, Tunneling Junction, ON State Current (I_{ON}), OFF State Current.*

I. INTRODUCTION

As the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is scaled down for the low power consumption because MOSFET cannot have a Subthreshold Swing (SS) below to the conventional limit of 60mv/dec at the room temperature [1, 2]. To maintain a high ON current, Subthreshold Swing (SS) needs to be reduced. To overcome these limitations the Tunnel Field Effect Transistor (TFET) has proposed as one of the most promising device. TFET has attracted a great deal of attention for its low Subthreshold Swing (SS) and high ON state current at low power supply (V_{dd}) [3, 4].

kink effect exists in the I_d-Vg graph and it originates from abrupt change in source doping. Due to this subthreshold swing (SS) and on-state current (I_{on}) of TFETs have been degraded. To improve SS and I_{on} the kink effects should be avoided and rounding off the sharp edge of source corner [5].Hump effects of L-Shaped TFET have been discussed. Hump effect seem to be originated from the extended source region so there are two TFETs in parallel whose Turn-on voltages ($V_{turn\text{-}on}$) are different., Non local tunneling model and Quantum mesh are to be used for accurate calculation. During the fabrication process, source junction should be designed carefully [6]. High turn on voltages is problematic for low power application. By introducing n-type dopants in tunneling regions, the design of L-Shaped TFET has been improved . When N_D increases,both subthreshold swing and $V_{turn\text{-}on}$ decrease. N-type dopants in tunneling Junction area can lower $V_{turn\text{-}on}$ while keeping SS low and I_{on} high [7]. The tunneling junction is perpendicular to the direction of channel that provides large tunneling junction area. The U-Shaped Channel in the vertical direction that reduces the device area and makes the channel distribute in the vertical direction. Between source and intrinsic region , a N^+ pocket has been introduced to improve the characteristics of device. N^+ pocket region and gate overlap in vertical direction as well as lateral direction to enhance the electric field . That resulting in the 50% increment in ON state current as compared to other L- Shaped TFETs [8]. A PNPN TFET with L-Shaped gate is proposed for on- state current (I_{on}) enhancement. The line and point tunneling between the source and N^+ pocket by which the tunneling area has been enlarged effectively [9]. The three different types of tunneling structures are discussed on the basis of their single event transient performance, such as the conventional planar TFET, Planar TFET with pocket and L-Shaped TFET. Among all three TFET structures the L-Shaped TFET is far better [10].

In reality, the conventional planar silicon-based TFET has an inherent disadvantage of low ON-state current (I_{ON}) because of silicon's relatively large band gap [11]. To improve ON state current, various techniques have been reported with simulation and experimental results. According to our previous research results, the former is originated from the small cross sectional area of tunneling junctions which is determined by channel inversion layer thickness. The latter is originated from the dependency of tunneling barrier width on the gate voltage (*V*g) [12**].**

II. DEVICE STRUCTURE AND SIMULATION METHOD

The proposed LG SOI TFET structure is illustrated in Figure 1. The gate resembles the alphabet "L" (PINK COLOUR). The proposed device makes band-to-band tunneling in both vertical and horizontal direction, which can effectively improve the device performance. LG SOI TFET has P-type doping of $1x10^{20}$ cm^{-3} and $1x10^{17}$ in source and channel region respectively and N-type doping of $1x10^{18}$ drain region. Simulation of the proposed device is carried out using Sentaurus TCAD including nonlocal BTBT model[13].

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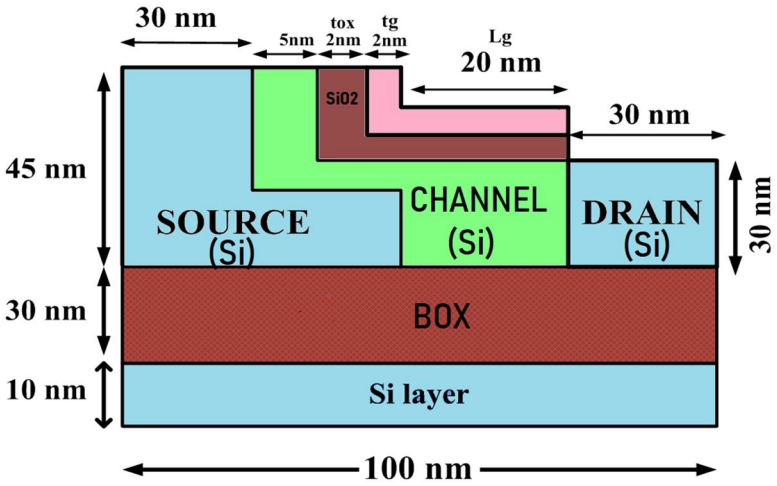


Figure 1. The Schematic Structure Of LG SOI TFET

TABLE 1
Device Parameters Used For The Simulation

PARAMETER NAME	SYMBOL	VALUE	UNIT
Gate Oxide Thickness (SiO_2)	t_{ox}	2	nm
Source Height	H_S	45	nm
Drain Height	H_D	30	nm
Gate Length	L_g	20	nm
Channel Thickness	t_{ch}	5	nm
Channel Width	W_{CH}	30	nm
Source Doping	N_S	$1x10^{20}$	cm^{-3}
Drain Doping	N_D	$1x10^{18}$	cm^{-3}
Channel Doping	N_i	$1x10^{17}$	cm^{-3}
Drain Voltage	V_{dd}	0.1	v

III. RESULTS AND DISCUSSION

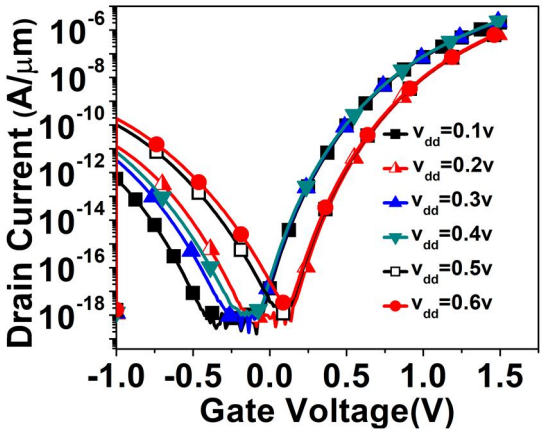


Figure 2. Transfer characteristics curves of the LG SOI TFET with different Drain Voltage (V_{dd})

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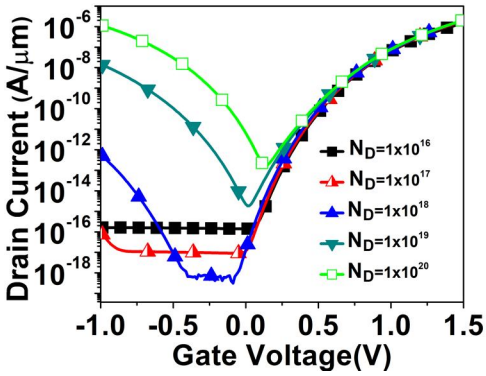


Figure 3. Transfer characteristics curves of the LG SOI TFET with different Drain Concentrations (N_D) at V_{dd}=0.1v

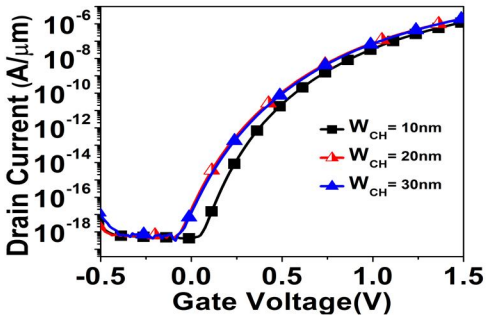


Figure 4. Transfer characteristics curves of the LG SOI TFET with different Channel Width (W_{CH}) at V_{dd}=0.1v

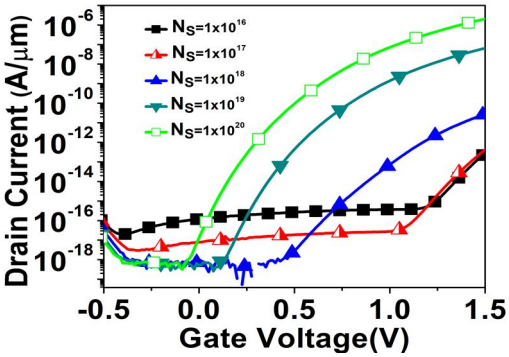


Figure 5. Transfer characteristics curves of the LG SOI TFET with different Source Concentrations (N_S) at V_{dd}=0.1v

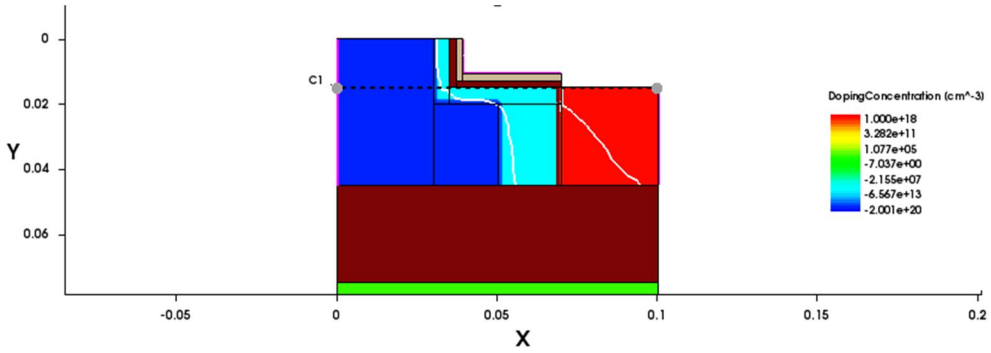


Figure 6. Schematic Diagram Of the LG SOI TFET

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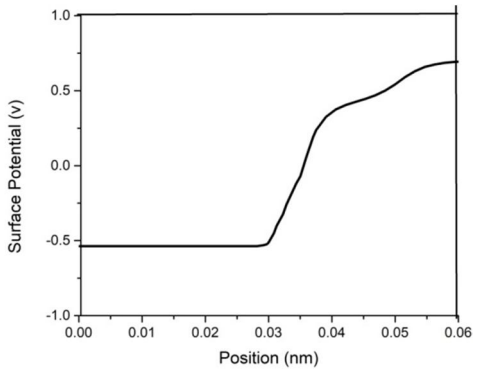


Figure 7. Surface Potential On Cut Line (C1) at Gate Voltage V_g= 1.5v

The transfer characteristic curves of the LG SOI TFET with the different Drain Voltage (V_{dd}) are shown in the Figure 2. It can be clearly observed from Figure 2 that OFF State leakage cuurent (I_{OFF}) is lowest and ON state current (I_{ON}) is highest at Drain Voltage 0.1v which means this device is suitable fow Low Power Applications. In Figure 3, the transfer characteristics curves with the different Drain Concentrations (N_d) and where we can easily analyze that on increasing the N-type doping in the drain region, the OFF State Leakage current is increasing.

TABLE 2
Drain Doping Variation

DRAIN DOPING (N_d)	I_{ON} (A/µm)	I_{ON} (A/µm)	I_{ON}/I_{OFF}
$1x10^{16}$	$1.425x10^{-6}$	$1.40x10^{-16}$	$1.018x10^{10}$
$1x10^{17}$	$1.878x10^{-6}$	$1.166x10^{-17}$	$1.60x10^{11}$
$1x10^{18}$	$2.035x10^{-6}$	$1.307x10^{-17}$	$1.557x10^{11}$
$1x10^{19}$	$2.012x10^{-6}$	$2.190x10^{-15}$	$9.412x10^{8}$
$1x10^{20}$	$2.077x10^{-6}$	$6.446x10^{-12}$	$3.22x10^{5}$

TABLE 3
Channel Width Variation

CHANEL WIDTH	I_{ON} (A/µm)	I_{OFF} (A/µm)	I_{ON}/I_{OFF}
10nm	$3.275x10^{-6}$	$2.201x10^{-15}$	$1.482x10^{9}$
20nm	$2.046x10^{-6}$	$1.950x10^{-17}$	$1.049x10^{11}$
30nm	$2.035x10^{-6}$	$1.307x10^{-17}$	$1.557x10^{11}$

In Figure 5, the transfer characteristics curves with the different Drain Concentrations (N_d) and resulting in the ON State Current increases with the P-type doping in the source reason. In Figure 6, this is the schematic diagram of the proposed device to just show the cut line (C1) at which the surface potential is to be calculated, although there is the two cut lines in the proposed device but here we have calculated surface potential with respect to only one cut line. In Figure 7, there is the graph between the positions and the surface potential at that particular position and it shows that the surface potential is reached the max at where front-gate ending point exists [14]. Then, the surface potential reduced due to the absence of a front gate, then gradually increased towards the drain side in region V. or we can say that surface potential is high at the channel junction region as well. After all the analysis we conclude that the proposed device is suitable for low power applications and it enables the high ON State Current and the OFF State Leakage Current has also reduced. I_{ON} = $2.035x10^{-6}$ A/µm, I_{OFF} = $1.307x\ 10^{-17}$ A/µm, I_{ON}/I_{OFF}= $1.557x10^{11}$.

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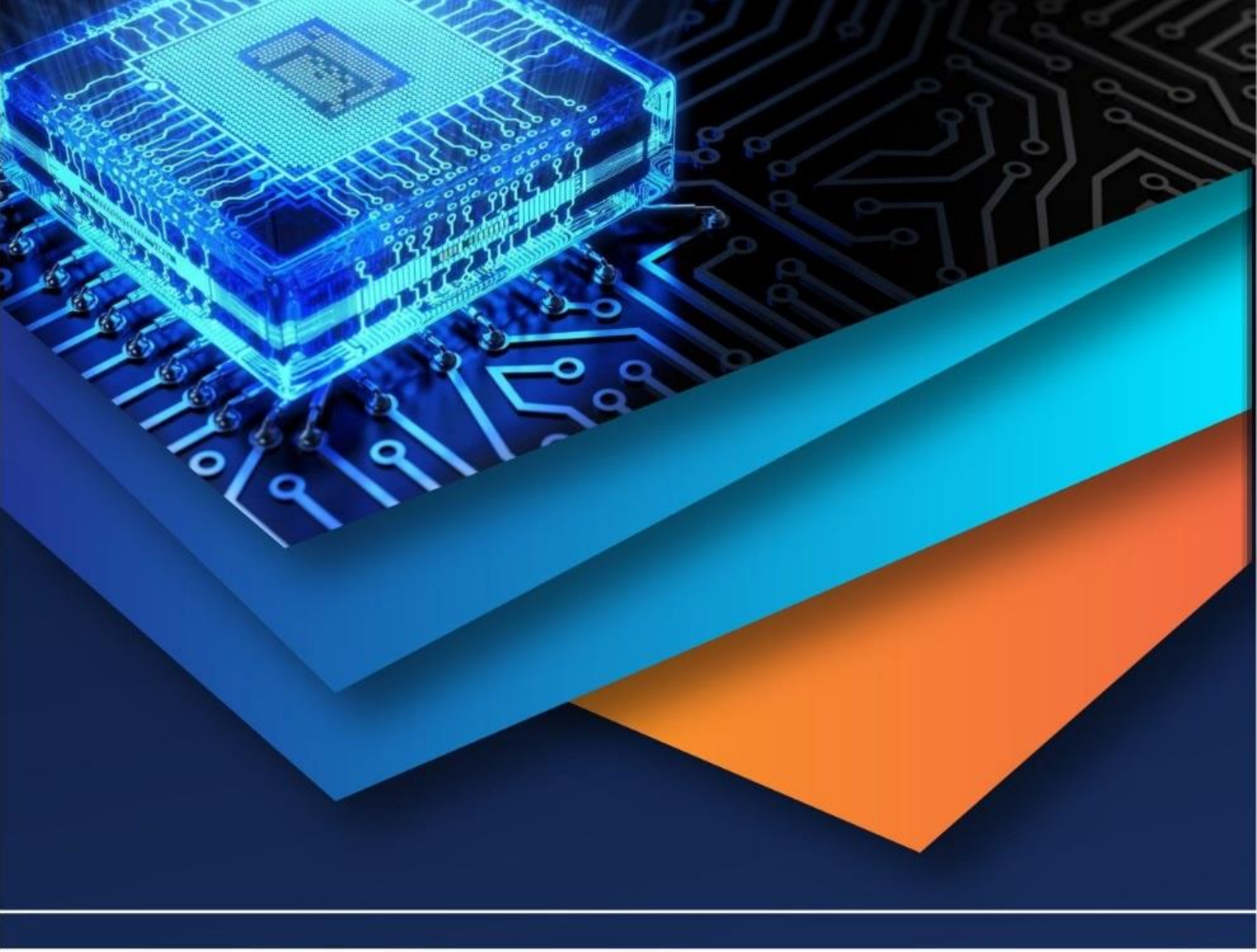
IV. CONCLUSION

In this paper, LG SOI TFET was studied. The proposed device is demonstrated to achieve a significantly improved performance as compared with a planar TFET, in terms of $I_{ON,}$ on-off current ratio and subthreshold swing. The tunneling junction is perpendicular to the channel direction that facilitates the implementation of a relatively large tunneling junction area[15]. Low drain doping and high source doping is resulting in high I_{ON} and low I_{OFF}.

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