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Power Quality Evaluation of Cascaded Multi-Level Inverter

Aquib Mehdi Naqvi[1], Mohd. Mudabbirul Hasan Mughni[2], Dr. R. P. Payasi[3], Dr. S. K. Sinha[4], Dr. A.S. Pandey[5]
[1, 2] *Student,* [3, 4, 5]*Professor, EED, KNIT, Sultanpur, U.P., India*

Abstract: ***The traditional inverters those consists of 2 levels, have the disadvantages of Harmonics. Construction of multi-level electrical converter technology has emerged as an honest answer within the space of high power medium-voltage energy management. This paper covers the foremost necessary topologies of MLI like diode-clamped MLI (or neutral-point clamped), capacitor-clamped MLI (or flying capacitor), and cascaded multi-cell with separate dc sources.***
This paper presents the basic concept of MLI and analysis of THD and harmonics by using MATLAB simulation of traditional two-level, SPWM controlled 3-level and cascaded five-level and cascaded seven-level MLIs.
Keywords: Inverter, Multilevel inverter, Cascaded Multilevel, THD, PWM, Simulink.

I. INTRODUCTION

A multilevel inverter is a power electronic device that provides desired alternating voltage level at the output using multiple lower-level DC voltages as an input. Conventionally, a two-level inverter is used in order to generate the AC voltage from DC voltage source but that generates the output with two voltage levels but it has high switching losses and harmonic voltage causes the flow of the harmonic current in the circuit and produces the losses. [1]
The power produced by the photovoltaic cell or the power stored in the battery exists in DC mode but the residential and industrial loads like the motor that drives the wheels and the most equipment we are using nowadays are usually consuming AC power. Here, the need for power converters rises that can convert DC to AC. For this conversion, Inverters are used, the simplest and commonly used topology for this conversion is the 2-level inverter that consists of 4 switches. Each switch needs an anti-parallel diode, so there should be also 4 anti-parallel diodes. There are also other complex topologies for inverters are available for better output as per the requirement. A multilevel inverter is a power electronic system that synthesizes a multilevel or stair-cased voltage output that is nearly sinusoidal from several DC sources. These DC sources can be batteries, fuel cells, solar-PV cells, ultracapacitors, etc. The term MLI starts with the 3-level inverter presented by Nabae *et al.* [2]. An increment in the levels of the inverter, the output voltages have more steps producing a staircase waveform, which has a reduces the harmonic distortion. MLIs have three types.
Diode-clamped MLIs, flying capacitor MLIs and cascaded H-bridge MLI [2].
Nowadays, MLIs are used in a wide-ranging applications, including motor drives for v/f speed control, utility applications, power quality enhancement at medium voltage and high power levels [3, 4]. An MLI application has been proposed in the field of renewable energy systems based on solar PVs, wind power generation system and fuel cells, to interface with the consumer-end or the utility i.e. power distribution system [3]. The first MLI circuit was diode-clamped, presented nearly 38 years ago [2], the development of MLI was began with a three-level inverter.

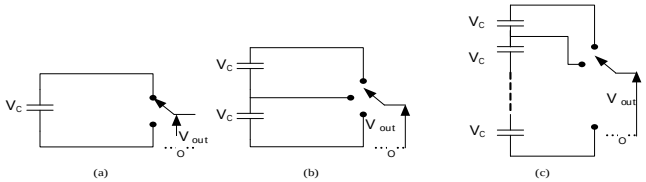


Fig- 1: Single phase leg of an inverter with (a) two levels, b) three levels, and(c) n levels

Fig 1 demonstrates a schematic of an MLI with a number of different levels. As the name of two-level inverter suggest it produces an output voltage with two levels, positive and negative, while in the three-level zero level is also present making the output voltage of three voltage levels, and so on[5, 6]. The series-connected capacitors shown in Fig. 1(c) is expected to divide the voltages equally and hence have the same voltage. This equal value of voltage across each capacitor, En, can be given by the following equation [7,8]

$$\boldsymbol{En = (V_{dc}/n - 1)}$$

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There are several advantages with an MLI when compared with a traditional (two-level) inverter [6]

A. Advantages

1) The staircase voltages produce by MLIs lead to the better and almost sinusoidal waveform, high power quality, and reduced the *dv/dt* stresses.
2) The MLIs draw current with a lower distortion level.
3) Production of common-mode voltage by MLIs is noticeably small.
4) The electromagnetic compatibility (EMC) difficulties are reduced [9, 10].

B. Disadvantages

1) Although a large number of components, such as semiconductor switches are required in MLIs, but these component are cheap due to a lower voltage rating compared with the 2-level inverter. However, the requirement of a gate drive circuit for each device, affects the cost and layout of the circuit design.
2) The complexity of Control increases with the increase in a number of levels.
3) Requirement of additional balancing circuit as MLIs suffers from unbalance of DC-link capacitor voltages [9,10].

Table-1: Comparison between traditional and multilevel inverter [1,11]

SR	Traditional Inverter	Multilevel Inverter
1	The high dv/dt i.e. rate of Voltage variation	The low dv/dt i.e. rate of Voltage variation
2	Losses in switching are high	Losses in switching are low
3	For application in low voltage range	For application in medium and high voltage range
4	Voltage stress is more on switches	voltage stress is less on switches
5	Switching frequency is high	Switching frequency is low
6	Multiple voltage level cannot be produced	Multiple voltage levels can be produced
7	Harmonics are more	A lesser amount of Harmonic is produced

II. ANALYSIS OF DIFFERENT TOPOLOGIES OF MULTILEVEL INVERTER

Following three topologies of MLIs have been presented by researchers in industrial applications:

1) Diode Clamped DCMLI /Neutral Point Clamped NPCMLI
2) Capacitor Clamped /Flying Capacitor FC MLI
3) A Cascaded H-Bridges CMLI

A. Diode Clamped Multilevel Inverters

Among the existing topologies of MLI, commonly used and oldest topology is Diode Clamped MLI (DCMI) [14, 15]. DCMI levels can be used for mono-phase or poly-phase applications.

Fig. 2 demonstrates the topologies of three-level in which this circuit, the input voltage is divided into three levels by series arrangement of two capacitors C_1 and C_2. The middle point, junction of the two capacitors (represented by symbol *'n'*) can be defined as the neutral point. The development of MLI was begun with three-level diode-clamped topology, presented by *Nabae et al.* [10] in 1981 and it is also recognized as the neutral-point clamped (NPC) inverter.

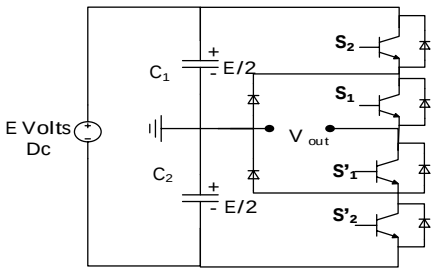


Fig- 2: Diode clamped three-level inverter

The operating states of three-level half-bridge diode clamped inverters have three switching states (*Vdc/2, 0 and -Vdc/2*).

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B. Capacitor Clamped Multilevel Inverter

A topology of Capacitor clamped MLI, which is also recognized as a flying capacitor inverter (FCI) produces the output voltage similar to the diode clamped topology, but its output voltage possesses more flexibility when compared with an NPC inverter. It reduces *dV/dt* stress across the switching device but the cost of the capacitor is more than diodes and this topology needs more capacitors with a higher rating than a diode clamped circuit [6, 11, 13].

The states of operation of a capacitor clamped three-level half-bridge consists of three switching states (*Vdc/2, 0 and -Vdc/2*).

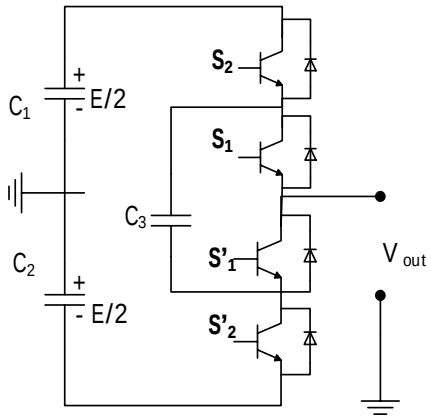


Fig- 3: Capacitor Clamped Three-Level Inverter

C. Cascaded Multilevel Inverter

Cascaded MLI are made up of of H-Bridge cell, connected to separate DC source as input, while output AC side is connected in series. In CMLI as shown in fig.-4, level can be increased by addition of H-bridge along with the DC separate source, and connecting AC side in series, to obtain high power quality. Every connected H bridge inverter generate an output of some voltage level. The output voltage of the cascaded inverter is the sum of all voltage produced by individual inverter cell. For *'n'* number of separate sources, or say inverter H-Bridge cell, the presence of levels in output voltage of CMLI is given by

$$= 2n+1$$

These inverters are usually built from the same type of H-Bridge inverter, but they can also be developed from different inverter topologies; thus, CMLI are also famous as hybrid inverters. The special feature of this inverter is requirement of lesser numbers of components than diode-clamped MLI [1, 14]

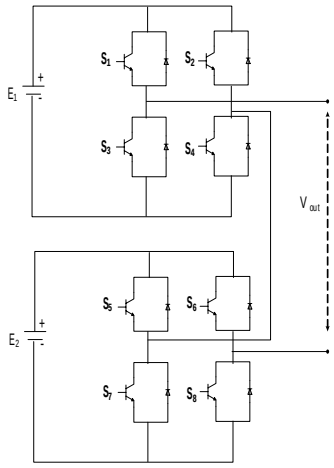


Fig. 4: Five-Level Cascaded H-Bridge Inverter

There are 16 possible states or switching combinations that produce the 5 different output voltage in a five-level CMLI [16]. In the case of E1 = E2 = E volt that makes the CMLI a symmetrical inverter, the inverter will produce: 2E, E, 0, -E and -2E. One possible state for both positive and negative 2E (and -2E), four probable states for both positive and negative E (and –E), and six possible zero voltage states, all these constitute the 16 possible states.

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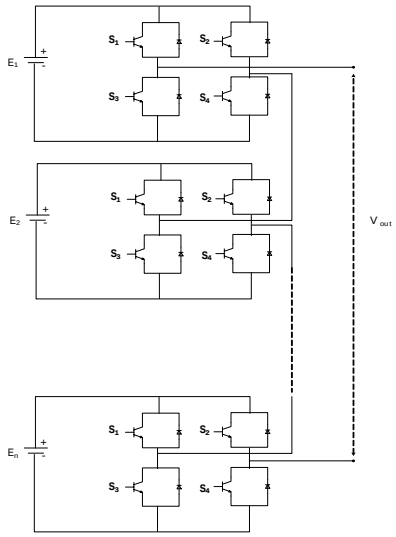


Fig. 5: General Cascaded Multilevel Inverter

III. SIMULINK MODELLING AND SIMULATION OF INVERTERS

In traditional 2 level inverter, sine wave generator is used as a reference along with the four switches. The switching pulses for the control of power switches in each H-bridge are provided by these four switches. Second sine wave generator has phase difference of 180^0.

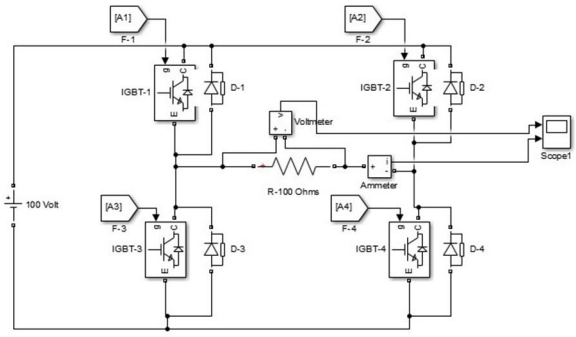


Fig- 6: Simulink Model Of two Level CMLI

In 3 level inverter, PWM control strategy is used, that adds a third level i.e. zero levels (neutral point). For PWM control strategy a repeating sequence is used along with a sine wave generator as a reference. The switching pulses in each H bridge are provided by the four switches.

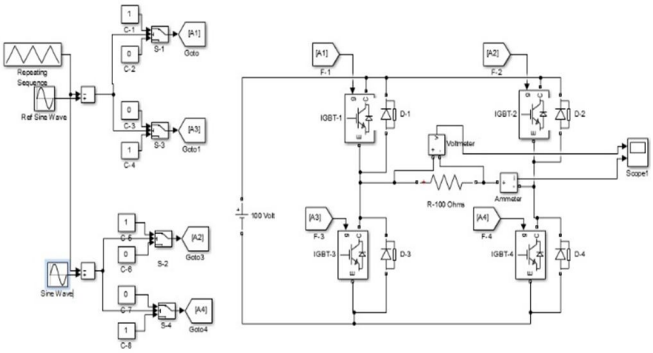


Fig- 7: Simulink Model Of Three Level CMLI

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In order to get the 5 levels cascaded MLI configuration the two H bridges are connected in series as shown in Fig. 7 within the MATLAB/Simulink atmosphere. The output of the primary H bridge is connected in series with the second bridge. Few repeating sequence along with a reference sine wave generator is used is each of H- bridge inverter. The switching pulses in each H bridge are provided by the four switches.

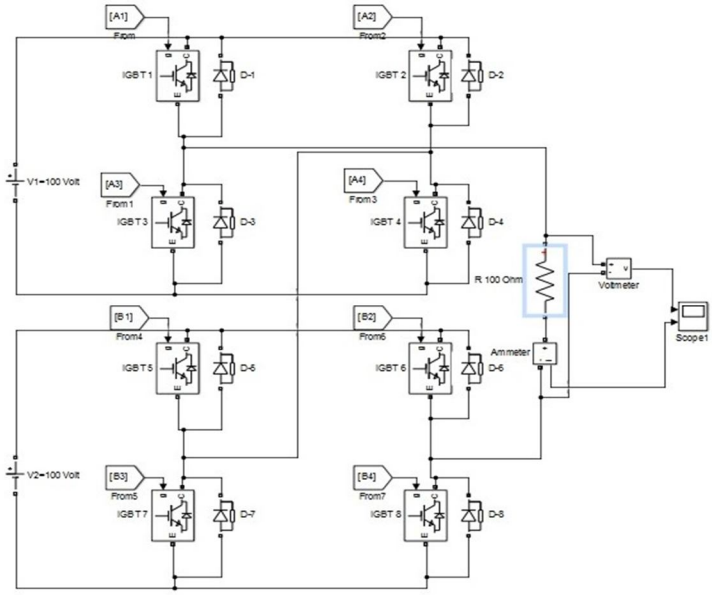


Fig- 8: Simulink Model Of Five-Level CMLI

Similarly, higher-level cascaded MLI can be obtained by connecting more H-bridge inverter in series.

IV. SIMULATION RESULT

MATLAB Simulink model of traditional 2 level inverter, SPWM controlled 3 levels and cascaded 5 levels and 7 levels MLI discussed above is used to obtain the waveforms and their THDs.

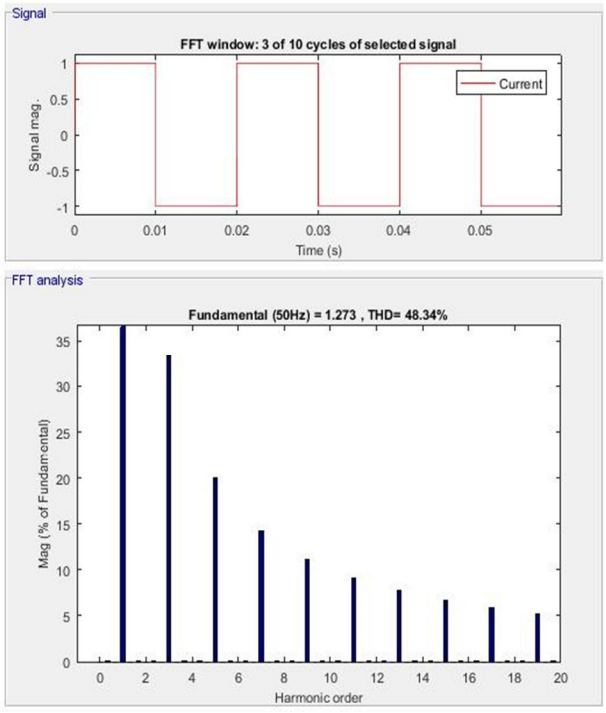


Fig- 9: Waveform and THD of conventional 2 level Inverter

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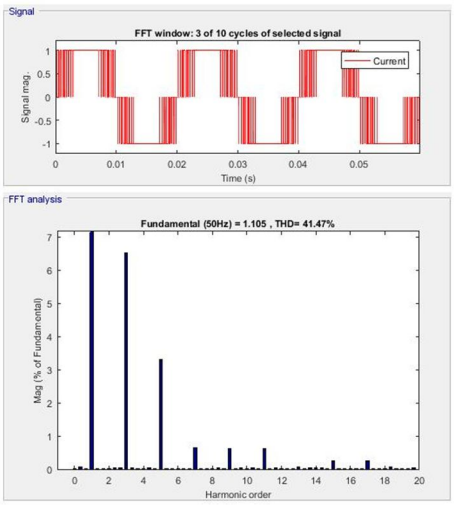


Fig- 10: Waveform and THD of 3 level Multilevel Invert

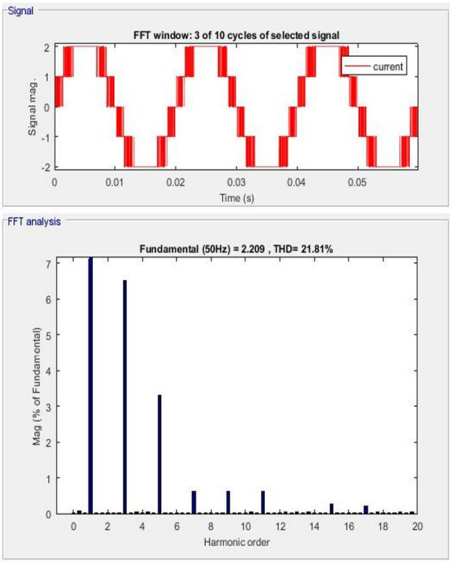


Fig- 11: Waveform and THD of 5 Levels Cascaded Multilevel Inverter

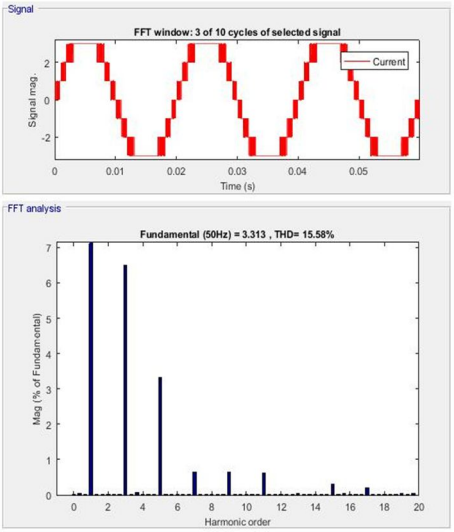


Fig- 12: Waveform and THD of 7 Levels Cascaded Multilevel Inverter

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These waveforms of the voltage across the load and THD are observed with a purely resistive load, i.e. unity power factor. In traditional 2 level inverter, THD is 48.34% and in 3-level inverter, THD decreases to 41.47%. In 5-level and 7-level inverter, THD is 21.81% and 15.58% respectively when simulated at a modulation index of 1.2 each.

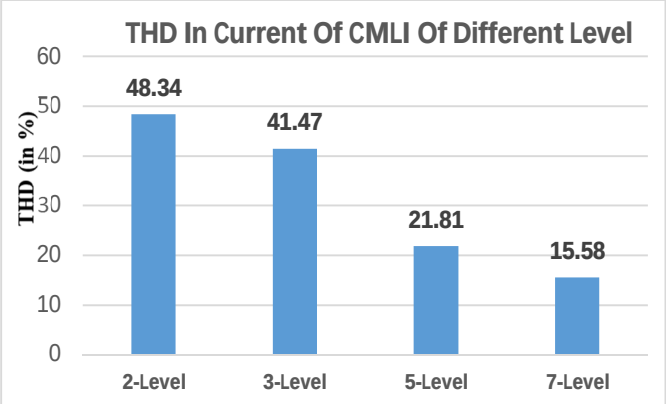


Fig. 13: Comparison of THD of different level's inverter

Table-2: THD of different level's inverter

SR	Level of inverter	THD
1	2-level	48.34%
2	3-level	41.47%
3	5-level	21.81%
4	7-level	15.58%

It can be observed from table 2 that with the increase in the level of inverter there is an improvement in the output waveform and a decrease in the THDs.

Now, the output waveform of different level of the CMLI is observed at different power factor. Commercial and residential load mostly draw power at lagging power factor, so the inductive load is used for simulation. The load is varied as given below so the power factor changes accordingly

Table-3: Load and power factor variation

SR	R (in ohms)	L (in mH)	Power Factor (lagging)
1	100	0	1.0
2	100	115	0.90
3	100	239	0.80

A remarkable change observed in the THDs with the small variation of power factor. In the 2-level inverter, THDs decreases from 48.34% to 18.65% when the load is varied from purely resistive to the inductive load.

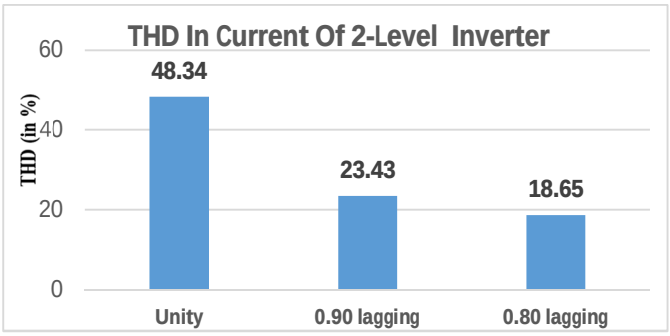


Fig- 14: THD in 2-level inverter at the different power factor

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Similarly, the load is varied in 3-level, 5- level CMLI and 7-level CMLI, and variation in the THD at different power factor is observed.

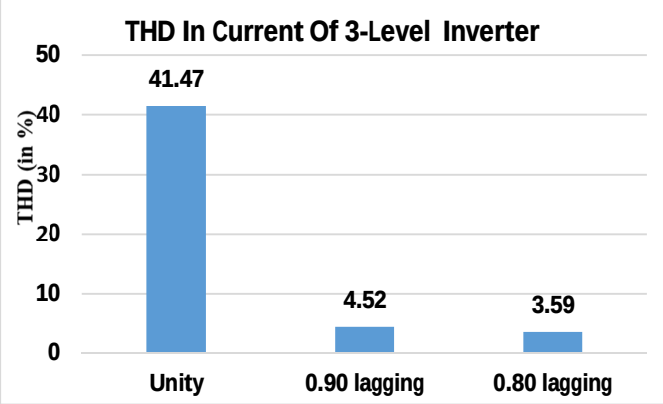


Fig- 15: THD in 3-level's inverter at the different power factor

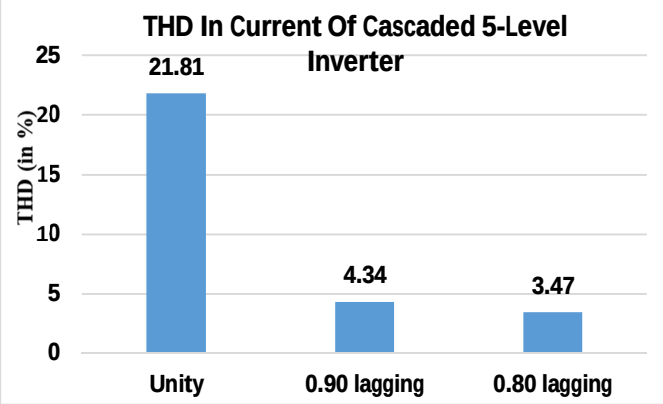


Fig- 16: THD in 5 level inverter at the different power factor

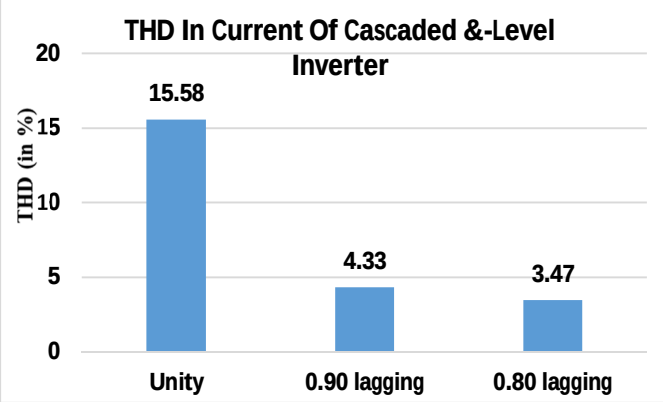


Fig- 17: THD in 7-level inverter at the different power factor

For a better understanding of this simulation work, here fig. 18 and table 4. Shows the variation of THDs in 2-level. 3-level, 5-level CMLI and 7-level CMLI with the variation in load (or say power factor). Here, we can summarize that the THD can be reduced to a very small value by using a higher level inverter, even without using any type of filter.

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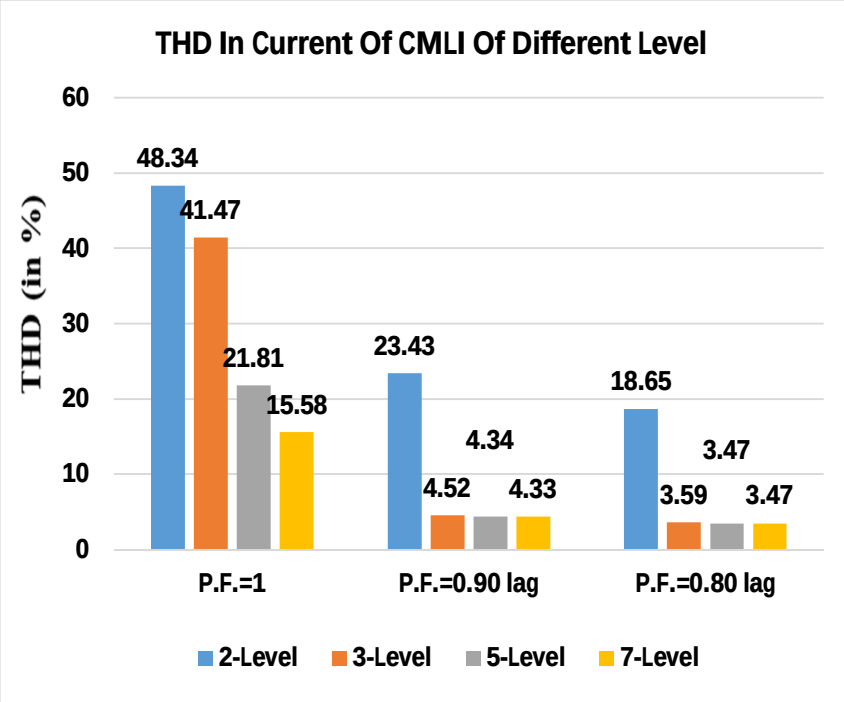


Fig- 18: Comparison of THD in different level's inverter at the different power factor

Table- 4: THD of different level's inverter at the different power factor

	Power factor	2-Level	3-Level	5-Level	7-Level
THD in Current (in %)	Unity	48.34	41.47	21.81	15.58
	0.90 lagging	23.43	4.52	4.34	4.33
	0.80 lagging	18.65	3.59	3.47	3.47

Now the comparision of different type of multiple-carrier SPWM switching technique is done at modulation index=1.2

Switching Technique	THD (in %)
Phase Disposition (PD) MC SPWM	21.66
Phase Opposition Disposition (POD) MC SPWM	21.12
Alternate Phase Opposition Disposition (APOD) MC SPWM	21.89
Phase Shift (PS) MC SPWM	21.81

It can be observed that in POD technique minimum THD is occurred. So, POD is best technique in aspect of power quality.

V. CONCLUSION AND FUTURE SCOPE

Conclusively it can be said that CMLI offers the lower THD with an increase in the level. MLI emerges as a good mean of power quality improvement. Therefore, the multilevel idea has recently attracted the researchers and industry to decrease the harmonic distortion within the output waveform while not decreasing the electrical converter power output.

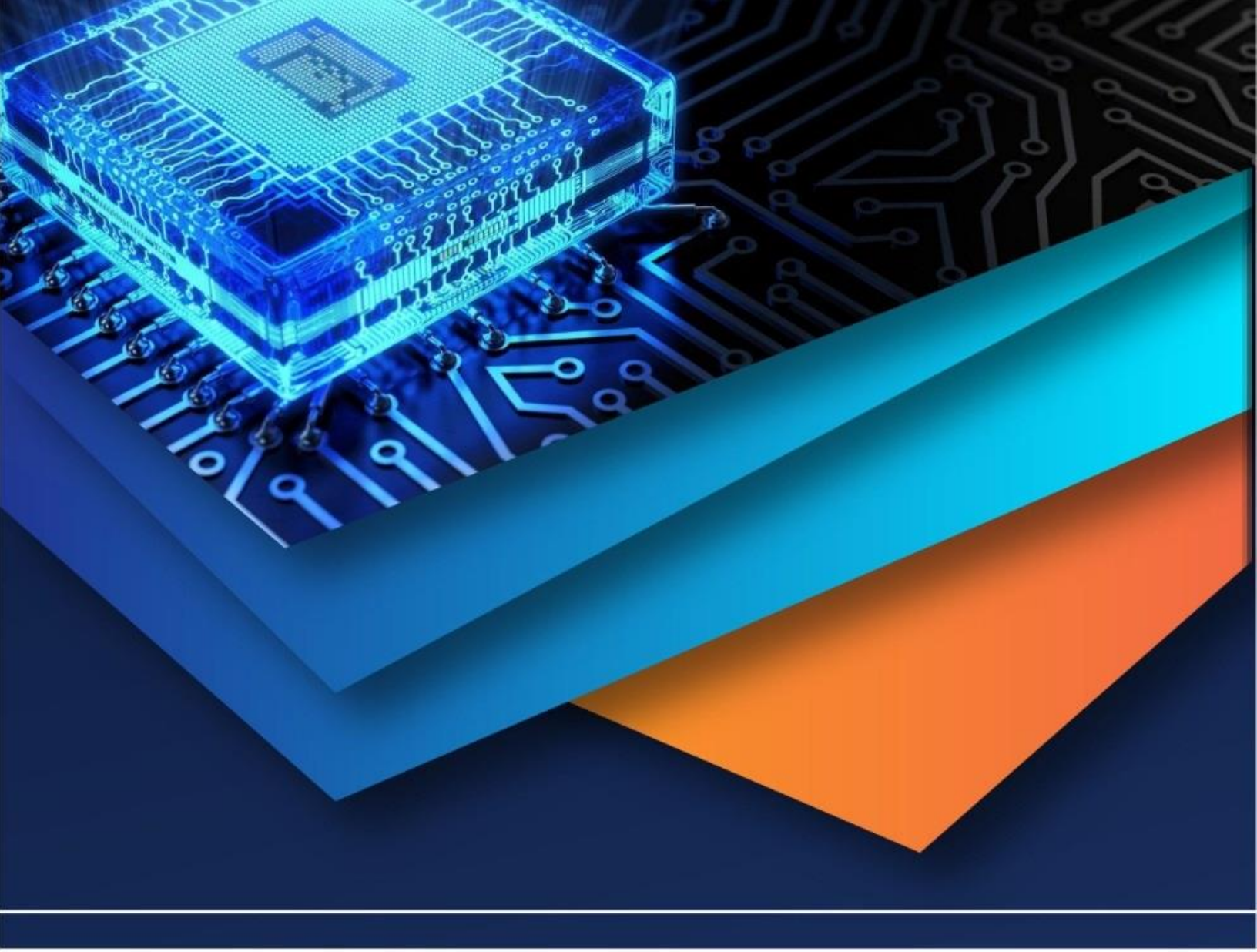
Multilevel inverters are emerge as a good option for the interface of renewable energy, that is solar, wind, fuel cell or combination of few making the system hybrid with the stand-alone loads or grid integrated system. Application of MLIs in drive control, FACT devices and EVs has been proposed by the researchers.

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REFERENCES

[1] Amol Koshti, M. N.Rao “A Brief review on multilevel inverter topologies” in ICDMAI Zeal Education Society, Pune, India, 2017
[2] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point clamped PWM inverter,” IEEE trans. on Ind. App.1981.
[3] C. Ying, Q. Chang, M. L. Crow, S. Pekarek, and S. Atcitty, "A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM With Energy Storage," IEEE trans. on Ind. Electronics, 2006.
[4] L. M. Tolbert, P. F. Zheng, and T. G. Habetler, "Multilevel converters for large electric drives," IEEE trans. on Ind. App., 1999.
[5] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing Renewable Energy Sources to the Utility Grid Using a Three-Level Inverter," IEEE trans. on Ind. Electronics, 2006
[6] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE trans. on Ind. Electronics, 2002.
[7] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of the multilevel inverter," in PESC '91 Record., 22nd Annual IEEE, 1991
[8] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," IEEE trans. on Ind. App. 1983.
[9] E. Cengelci, S. U. Sulistijo, B. O. Woo, P. Enjeti, R. Teodorescu, and F. Blaabjerg, "A new medium voltage PWM inverter topology for adjustable speed drives," in Ind. App. Conference, 1998. Thirty-Third IAS Annual Meeting,1998.
[10] L. Poh Chiang, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," IEEE trans. on Ind. App. 2003.
[11] Anjali Krishna R, and Dr. L. P. Suresh "A Brief Review on Multi-Level Inverter Topologies" in ICCPCT 2016, IEEE trans
[12] R. W. Menzies and Z. Yiping, "Advanced static compensation using a multilevel GTO thyristor inverter," IEEE trans. on Power Delivery, 1995.
[13] J. S. Lai and F. Z. Peng, "Multilevel converters - A new breed of power converters," IEEE trans. on Ind. App. 1996.
[14] S. Wei, Bin Wu, F. Li and Xudong S.” Control method for cascaded H-bridge multilevel inverter with faulty power cells” APEC '03. Eighteenth Annual IEEE Year: 2003,
[15] K. Corzine and Y. Familiant, "A new cascaded multilevel H-bridge drive," IEEE trans. on Power Electronics, 2002.
[16] M. Calais, V. G. Agelidis, L. J. Borle, and M. S. Dymond, "A transformerless five level cascaded inverter based single-phase photovoltaic system," in. PESC, IEEE 31st Annual, 2000.

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