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Performance Evaluation of Ternary Content Addressable Memory and 3T-2R TCAM

K. Vamsi Vardhanarao[1], L. Srikanth[2]
[1]*Post Graduate Student,* [2]*Asst Professor, Department of Electronics communication Engineering, GMRIT Engineering College, RAJAM, AP, India- 532127*

Abstract: ***The content addressable memory (CAM) is implementing the functionality of the lookup table in a one clock cycle. It is utilizing dedicated circuitry. Ternary content-addressable memories (TCAM) is operating at low power dissipation and fast data recovery. The CMOS based TCAMs provides, fast data access by storing information in the SRAM cell, but it consumes high leakage power. The memristors are replaced with the SRAM cell, it gives the best solution for decreases leakage power. It takes less area compared to SRAM cell and also decreases the delay, stand by power of circuit and voltage swing at the matched line ML, by using a memristor device maximum power dissipation can be reduced along with area efficiency compared to Conventional TCAM. Here Comparison between NOR-type TCAM with memristor equivalent 3T-2R TCAM and PE TCAM is done in terms of power, area. The proposed design has 30% area efficiency and high-power consumptions compared to Conventional TCAM. Simulations are performed with the help of cadence software in 45nm technology.***
Keywords: Ternary Content addressable memory (TCAM), 3T-2R TCAM, PE TCAM.

I. INTRODUCTION

Present days in human life one of the most important things is to access the internet with the high speed of data level. And the speed of internet services depends on the performance router. The router can be searching the IP address from the lookup table and packets promoting to the endpoint. The efficiency of the good network depends on the two factors one is a time delay and another one is packet transmission. Overcome these two factors, automatically increases the speed of the internet and the fast lookup table operation is searched and processed to the destination in less time. A software-based search is used. Content addressable memory (CAM) takes data as an input and gives the address as an output, with the help of the CAM user gets the location in which the data is stored. Searching speed of content addressable memory is higher than software-based search algorithms. CAMs are used in many routing applications and hardware such as network router, cache memories, etc… The architecture of cam is shown in fig.1

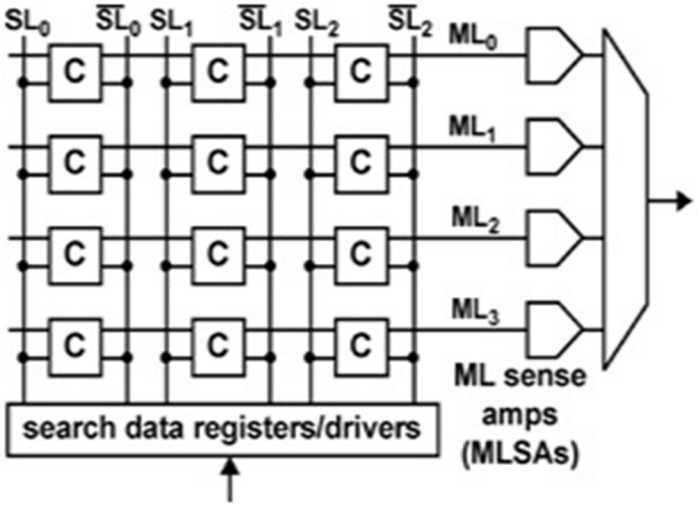

Fig. 1 CAM Architecture

Memristor is a semiconductor device. It has two terminals, in section II, III TCAMS has memristor components in the unit cell. Mainly they are used to store the data. So that here the memristor is replaced with SRAM and the resistance of the memristor is varied by the charge passes through the device. And memristor resistance depends on the amount charge flows through it.
In this work, we observe the performance of the ternary CAMS. And voltage levels of the TCAMS. Mainly in section II describes the Basic TCAM cell operation, section III 3T-3R TCAM operation, and section IV Focused on the PE TCAM operation and voltage levels of the desired circuit.

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II. REVIEW OF LITERATURE

The functionality of the TCAM cell and its circuit diagram is shown in table.1 & fig. 2. The TCAM cell has 12 transistors, and in this circuit two back to back inverters are connected, so it will act as memory. (DL, DLB) Data lines, (SL, SLB) search lines are the inputs of the TCAM cell and it can store two bits and performs three states operation.

1) *When the logic '0' is stored in TCAM:* In the first condition, DL = 0 and DLB = 1 is given to the TCAM cell Logic 0 is stored. If SL = 0, SLB = 1, this case m2 is off, m1 is on, m3 is off, m4 is on. So ml is high. And SL = 1, SLB = 0, this case m2 is off, m1 is on, m3 is off, m4 is on. So ml is low.
2) *When the logic '1' is stored in TCAM:* In the second condition, DL = 1 and DLB = 0 is given to the TCAM cell Logic 1 is stored. If SL = 0, SLB = 1, this case m2 is off, m1 is off, m3 is o, m4 is on. So ml is high. And SL = 1, SLB = 0, this case m2 is off, m1 is on, m3 is off, m4 is on. So ml is low.
3) *When the logic 'x' is stored in TCAM:* In this condition DL = 1 and DLB = 1 is given to the TCAM cell Logic 'x' (0 or 1) is stored. Here DL, DLB is high, then m1, m3 is off state. So that case, ml is always high due to irrespective of search lines. Because of don`t care (x) state, an extra state consumes high power, compared to the BCAM cell.

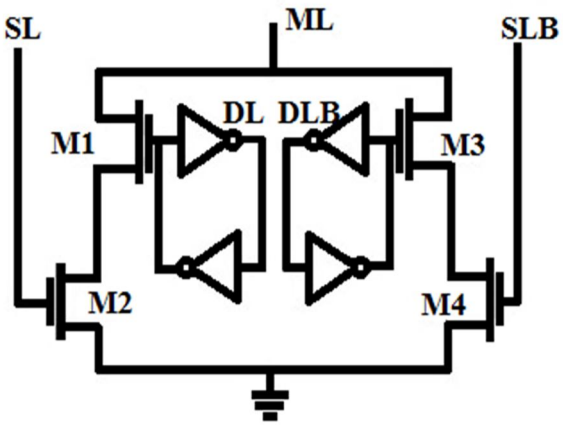

Fig. 2 Basic TCAM cell

Table 1: Functionality of TCAM cell

STORED	DL	DLB	SL	SLB	ML
0	0	1	0	1	HIGH
			1	0	LOW
1	1	0	1	0	HIGH
			0	1	LOW
X	1	1	X	X	HIGH

The 3T-2R TCAM cell has 3 transistors and 2 resistors and the functionality of the 3T-2R Based TCAM is shown in fig.3, a (PMOS) m1 is placed in between two memristors and gate terminal of the (NMOS) m2 & m3 transistors. And Von voltage is applied the m1. Pre is connected to the ground terminal, preb is connected to the gate terminal of m4 and the output of matched line is connected to the drain terminals of the m2 & m3. The tabular form of the 3T-2R TCAM is shown in table.2.

4) *When the logic '0' is stored in 3T-2R TCAM; [R1 = LOW R2 = HIGH]:* If R1 = RL, R2 = RH then the stored value is '0'. And if SL = 0, SLB = 1 Then therefore searched data matches with the stored data matched line will be high And R1 = RL, R2 = RH and SL = 1, SLB = 0 Then stored data doesn't match with searched data therefore ML discharges to ground.
5) *When the logic '1' is stored in 3T-2R TCAM; [R1 = HIGH R2 = LOW]:* If R1 = RH, R2 = RL then the stored value is '1'. And if SL = 1, SLB = 0 Then therefore searched data matches with the stored data matched line will be high And R1 = RL, R2 = RH and SL = 0, SLB = 1 Then stored data doesn't match with searched data therefore ML discharges to ground.
6) *When the logic 'x' is stored in 3T-2R TCAM; [R1 = HIGH R2 = HIGH]:* In this case of don't care R1 = RH, R2 = RH and then irrespective of searched data ML becomes at high.

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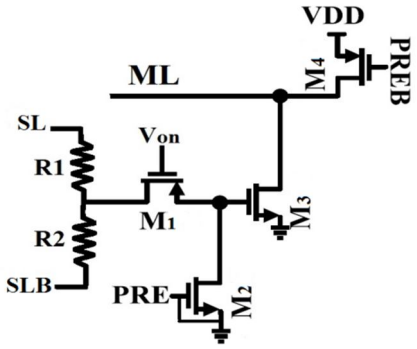

Fig.3 3T-2R TCAM unit cell structure..

Table 2: Functionality of 3T-2R TCAM cell

STORED	R1	R2	SL	SLB	ML
0	RL	RH	0	1	HIGH
			1	0	LOW
1	RH	RL	1	0	HIGH
			0	1	LOW
X	RH	RH	X	X	HIGH

III. PRIORTY ENCODER TCAM

The operation of the PE TCAM design is similar to the 3T-2R TCAM. The NMOS transistor M1 is placed in between two memristors and gate terminal of the (NMOS) m2 & m3 transistors. Search data and stored data operations are the same as a 3T-2R TCAM cell. And this cell reduces the overhead of PE and it controls the three-phase of VLV. The comparison circuit memristors having different voltage levels according to the search outcome. Therefore using a sophisticated control method of the current flow through M3 (matched line current) IML based on 3T-2R TCAM to execute the priority encoding function during the search process. M4 is connected to the matched line (ML). The PE TCAM cell is connected to M4 that makeup one word. M4 is used to increase the ML voltage. M1 and M4 are the main components of the PE TCAM operation. These two transistors are used to control the priority encoding operation, The PE TCAM cell performs two phases of functions in a single operation. One is the evaluation phase and another one is the encoding phase. In the evaluation phase the search inputs SL/SLB is applied R1 and R2, The M1 is on at that time M4 is off state. M1 transfers the node point of the M2 and M3 to be different from one another according to the comparison result. Then matched line voltage preserves a precharge level Vss has no current path in between ML. And the second phase, during the encoding period M1 is off and M4 is on. In this case current flow through M4, ML voltage increases. Here Von changes from high level to low level, the current driving capability of ML is determined by VLV, which acts to block the charge accumulation of the matched line. The current flowing through the m2 reduces the matched line current. In this section, the process to explain the operation of the PE TCAM cell and shown in fig.4.

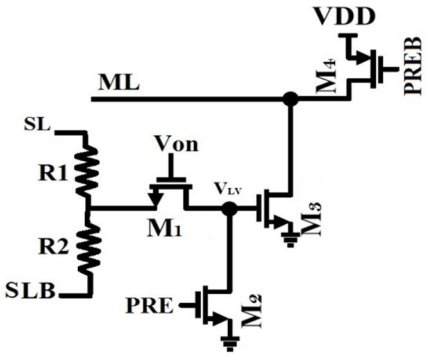

Fig. 4 PE TCAM cell

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Table 3: Functionality of PE TCAM cell

STORED	R1	R2	SL	SLB	ML
0	R L	R H	0	1	HIGH
			1	0	LOW
1	R H	R L	1	0	HIGH
			0	1	LOW
X	R H	R H	X	X	HIGH

IV. RESULT AND DISCUSSION

The Ternary CAM, 3T-2R TCAM, and PE TCAM cells are implemented using cadence software 45nm technology. The Waveforms of TCAM, 3T-2R TCAM, and PE TCAM cell are shown in figures 5.3, 5.6 and 5.9 respectively. The waveforms we observed, the average power and the area values are shown in table.4.

Table 4: performance of TCAM, 3T-2R TCAM & PE TCAM

Parameter	BASIC TCAM	3T-2R TCAM	PE TCAM
Technology	45nm CMOS		
Supply voltage(V)	1V	1V	1V
Average power(µw)	19.55	126.78	121.27
Area(µm²)	9.57	4.79	4.63

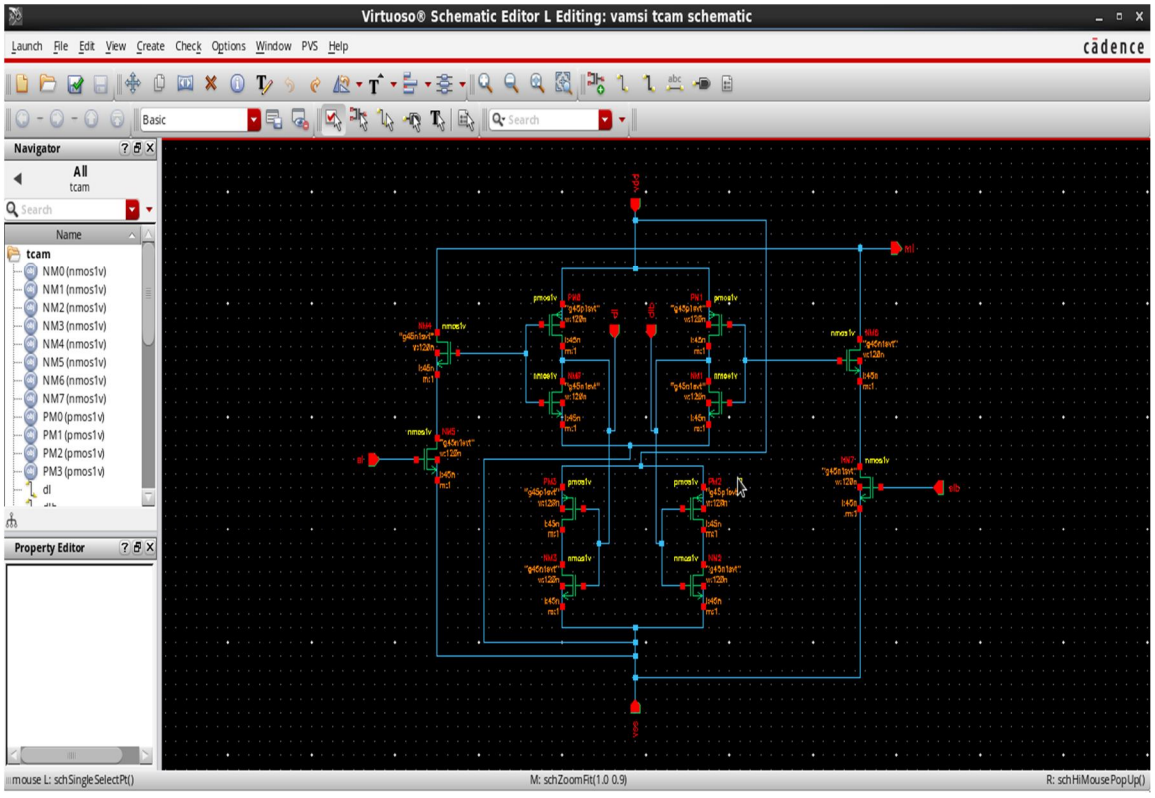

Fig. 5.1 TCAM Schematic

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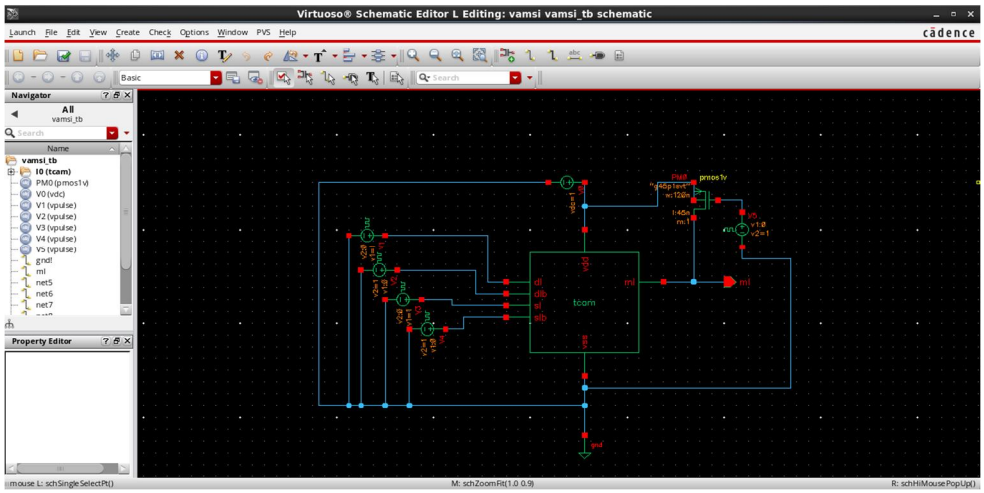

Fig. 5.2 Test Bench of the circuit

By using cadence virtuoso software draw the schematic diagram and test bench of the tcam circuit. And shown in fig 5.1, fig 5.2.

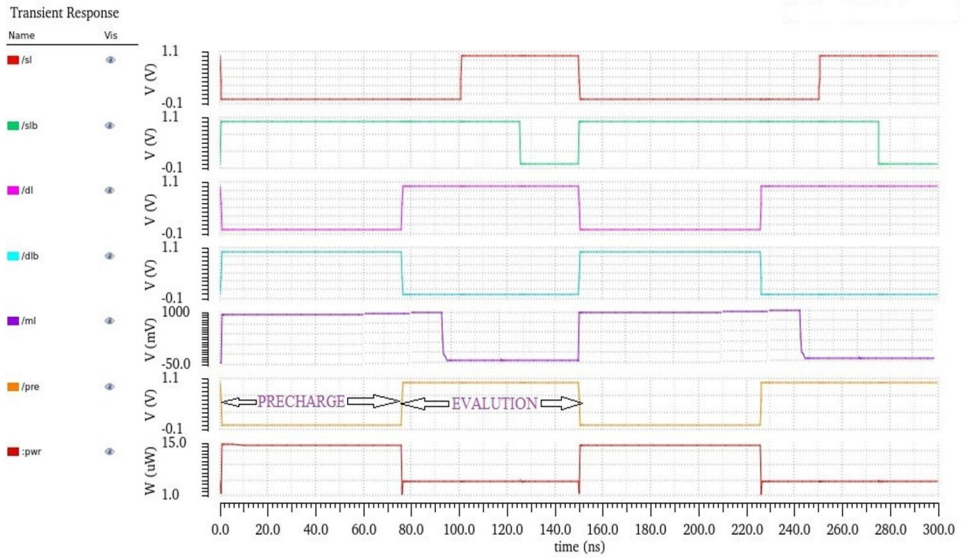

Fig. 5.3 Simulation waveforms of TCAM

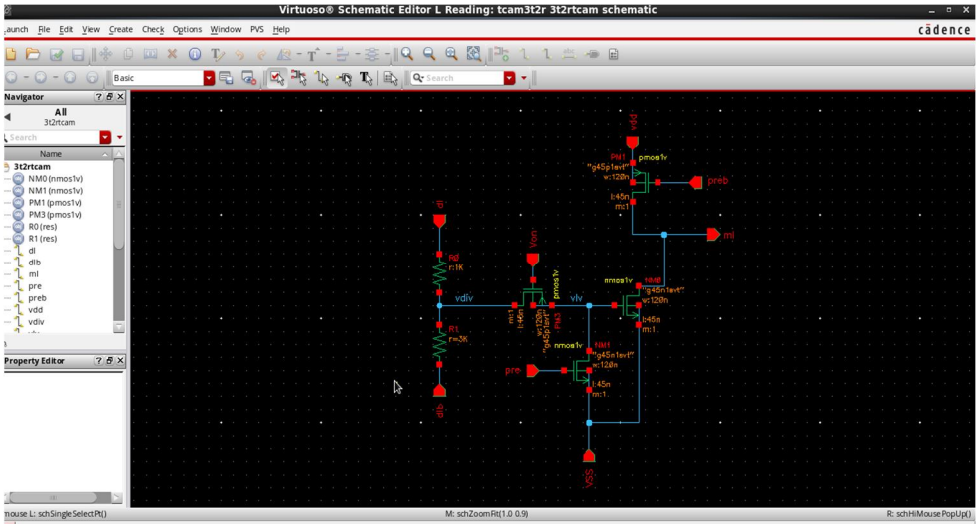

Fig. 5.4 3T-2R TCAM Schematic

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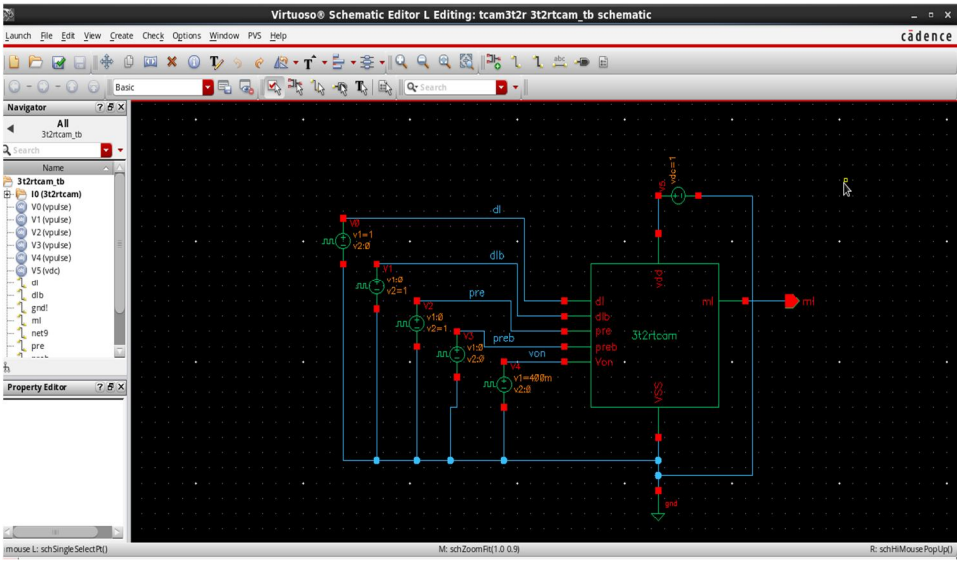

Fig.5.5. Test Bench of the 3T-2R TCAM circuit

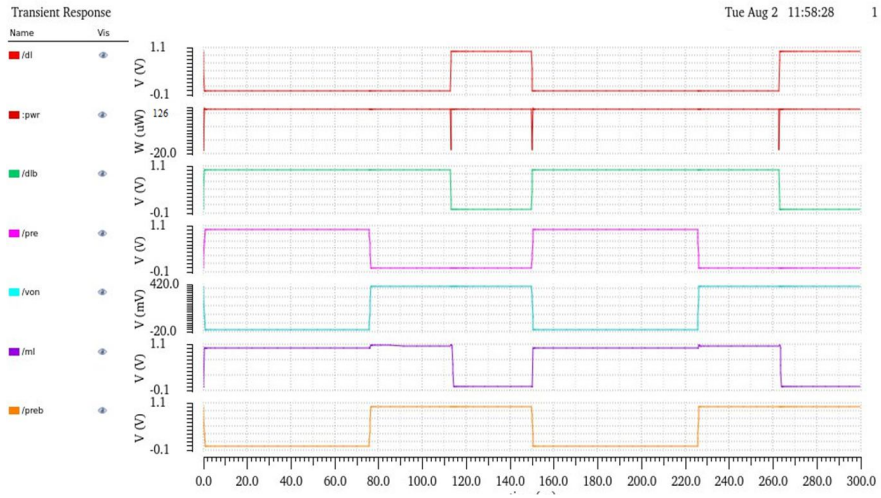

Fig. 5.6 waveforms of 3T-2R TCAM cell

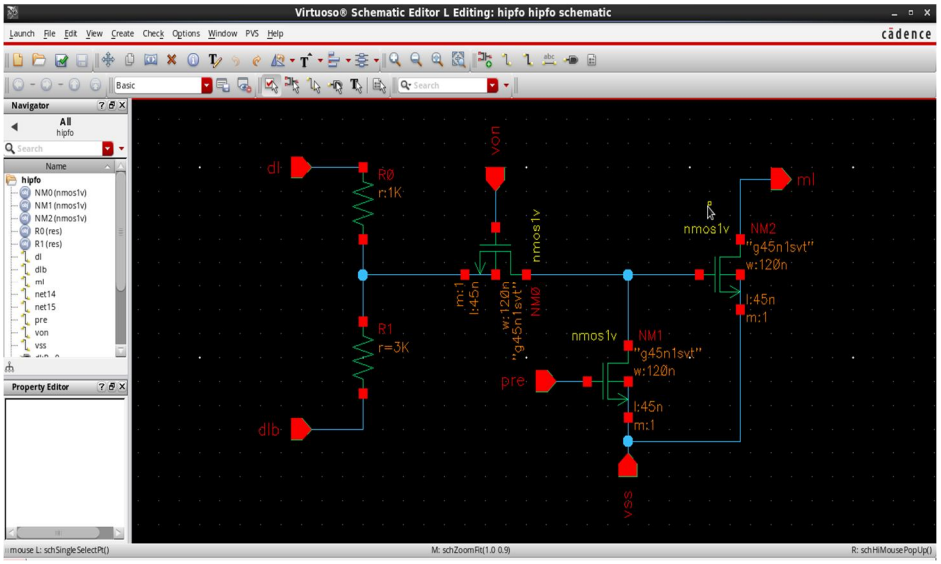

Fig. 5.7 PE TCAM Schematic

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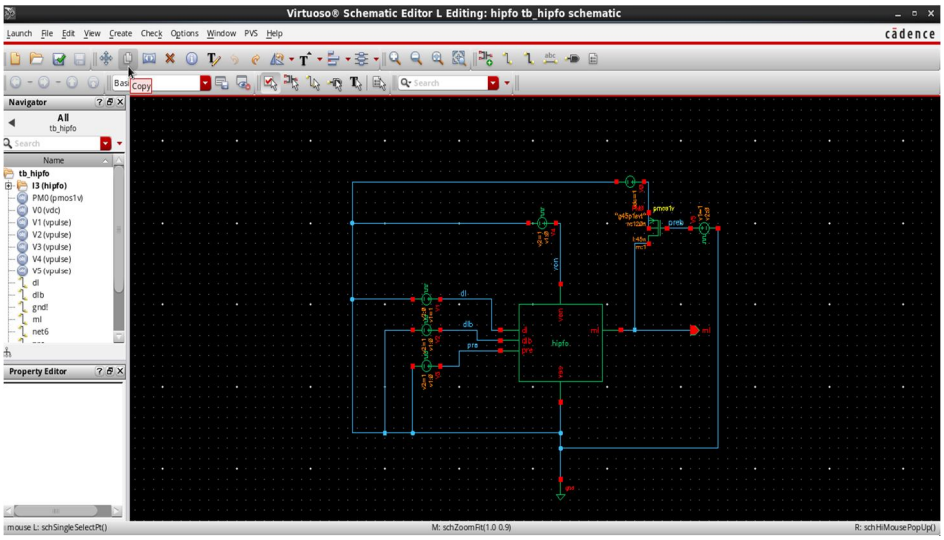

Fig. 5.8 PE TCAM Test Bench

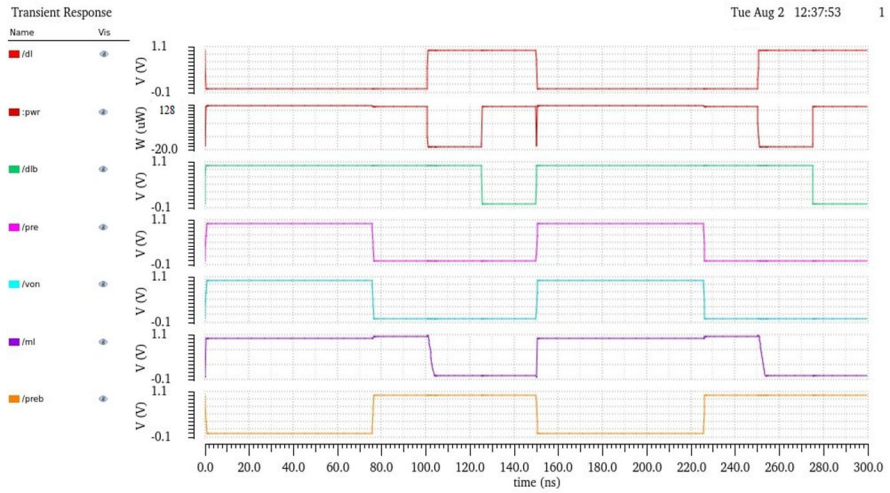

Fig. 5.9 Simulation waveforms of PE TCAM cell

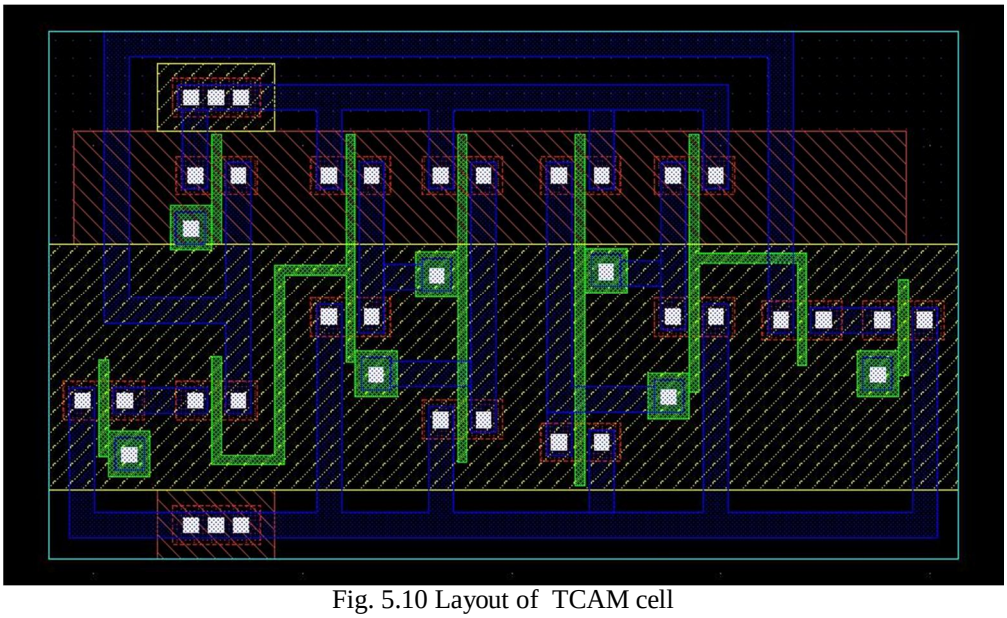

Fig. 5.10 Layout of TCAM cell

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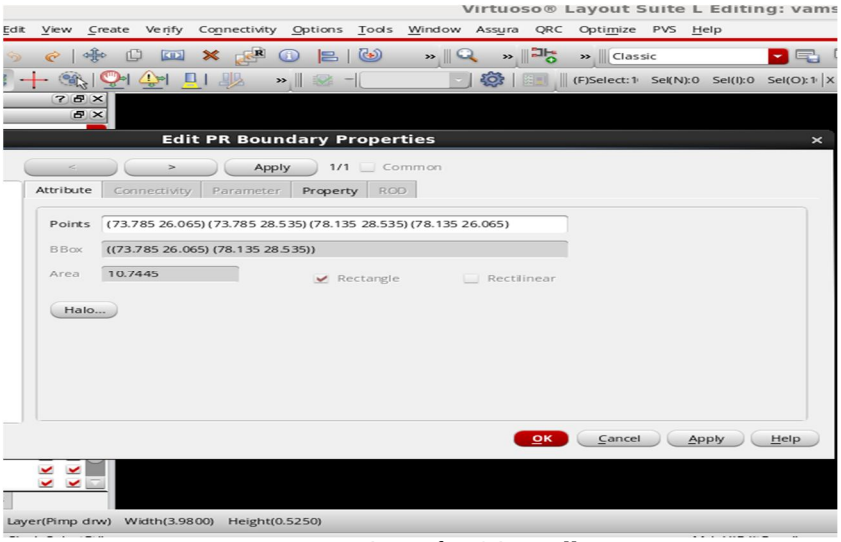

Fig. 5.11 Area of TCAM cell

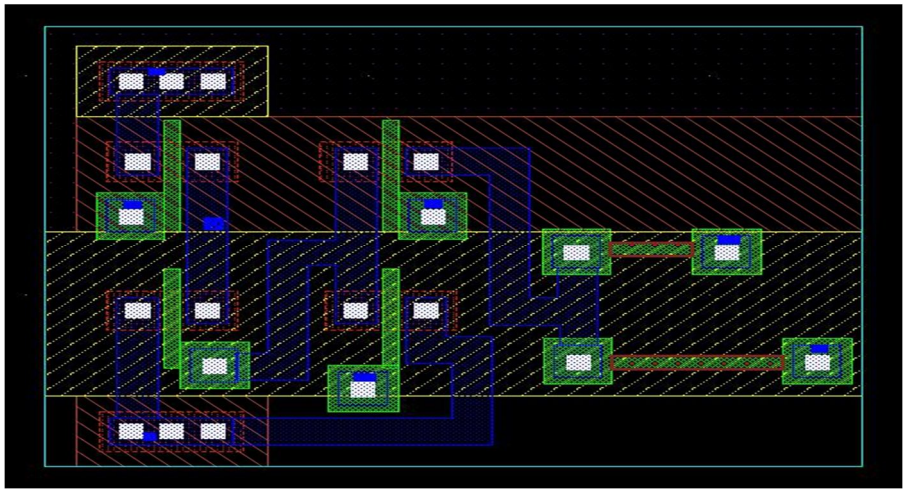
Fig. 5.12 layout of 3T-2R TCAM cell

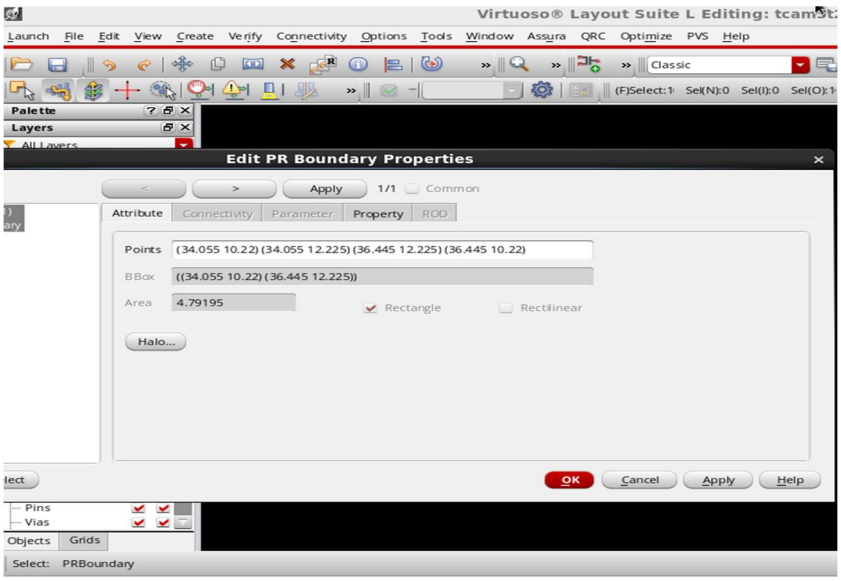

Fig. 5.13 Area of 3T-2R TCAM cell

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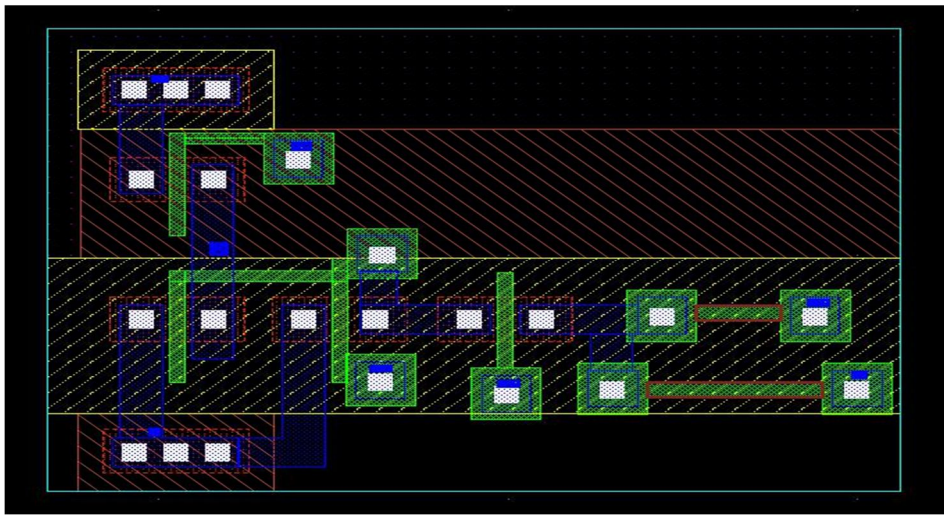

Fig. 5.14 Layout of PE TCAM cell

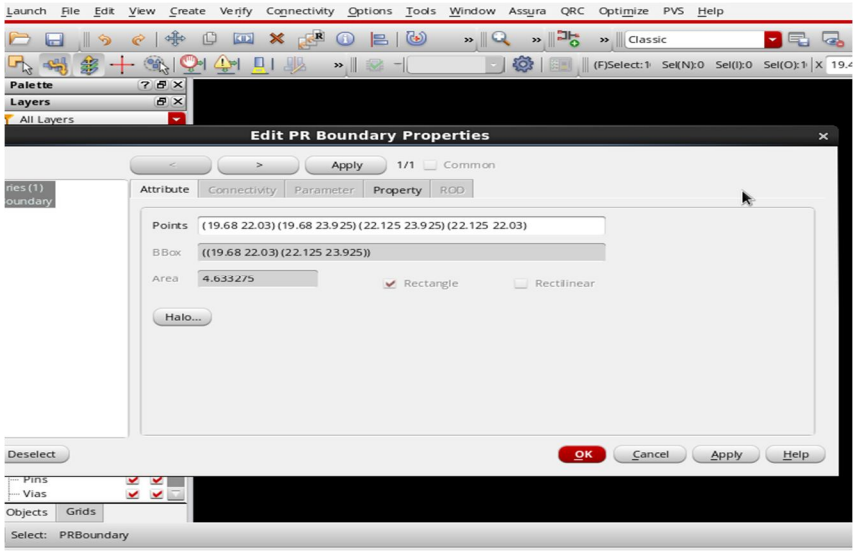

Fig. 5.15 Area of PE TCAM cell

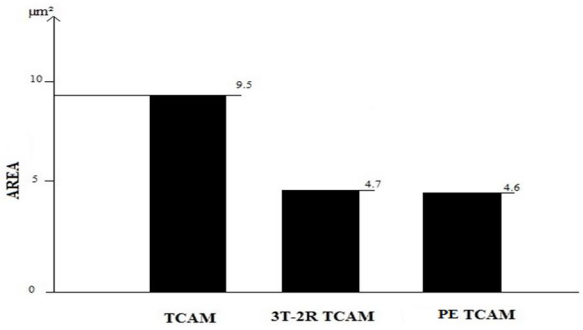

Fig. 5.16 Area comparison in diffent cams

V. CONCLUSION

Ternary content-addressable memory proposed with memristor devices. It provides fast retrieval of data along with low power consumption and high area efficiency. But in memristor equivalent, TCAM develops 10% area efficiency and high-power consumption over Conventional TCAM. In electronics approaches the limits of silicon, memristor components will play a very important role in ensuring steady performance gains, faster and high capacity storage at less cost and low power consumption.

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AUTHORS PROFILE

K Vamsi Vardhanarao Received the B.Tech degree in (ECE) from JNTUK in 2016, Now he pursuing M.Tech Specialization in (VLSI&ESD) (ECE Dept.) from GMRIT in JNTU Kakinada. His areas of interest are Low power electronics circuits and low power VLSI.

L. Srikanth, Assistant Professor in Department of ECE, GMR Institute of Technology, GMR Nagar, Rajam-532127, Srikakulam Dist. Andhra Pradesh, India.

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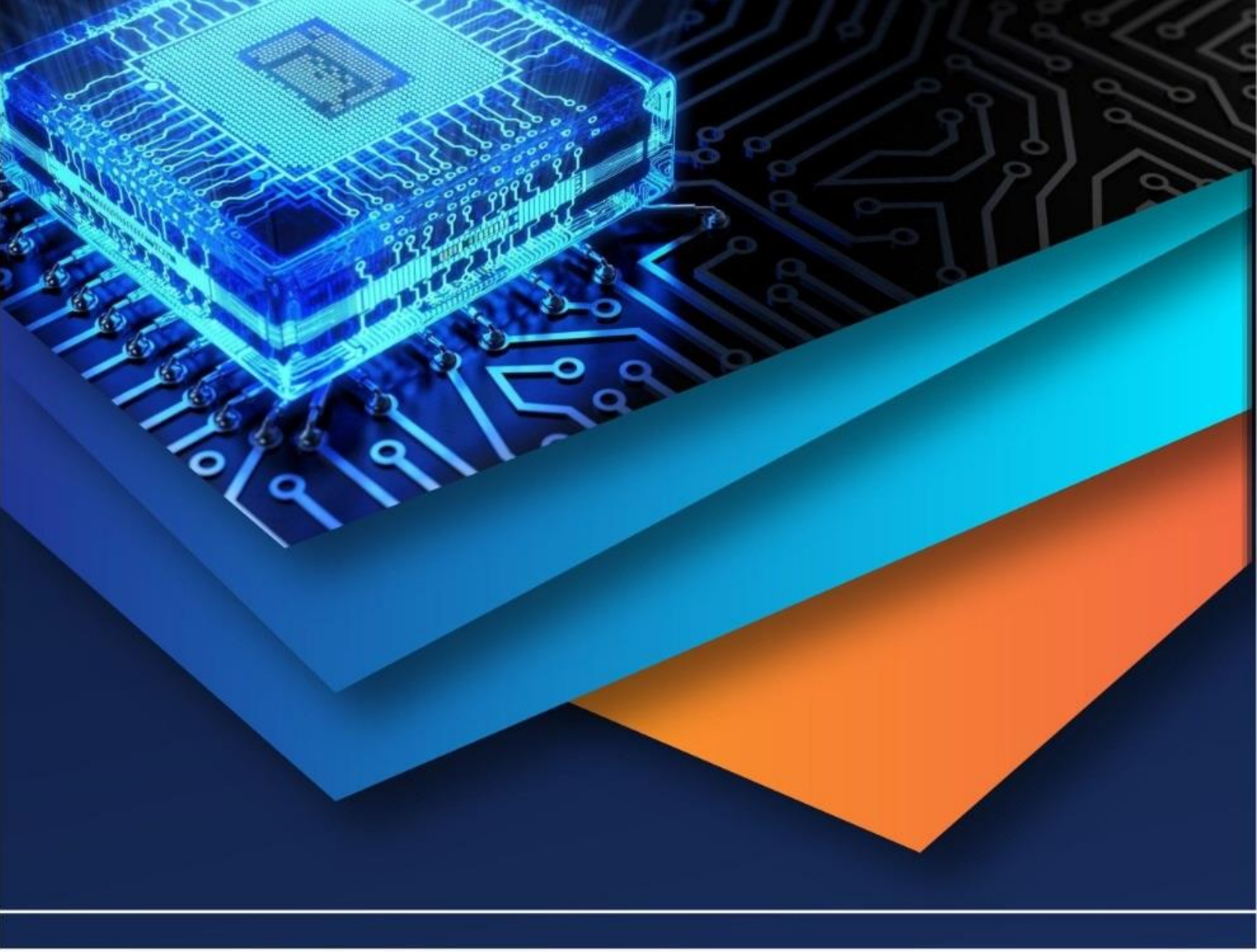

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