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Physical Aware Timing ECO for Faster Timing Convergence :16nm FinFET

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Abstract: ***In the standard Physical Design flow, the implementation tool is used for P&R (Place n Route). The implementation tool has in-built extraction and timing engines to report the timing based on CCS timing and noise libraries. These in-built engines are not very accurate. To overcome these shortcomings, the routed database is taken through extraction tool, to created spefs, and then to timing tool, to run timing analysis across multiple corners. The timing tool generates ECOs (Engineering Change Order) which is implemented to fix the timing. The changes are made on cell-by-cell basis to do what-if analysis and the result is implemented in implementation tool to reflect the changes.***
The designer can use implementation tool and timing tool from different vendors. The resulting timing correlation may be poor between the 2 tools and the correlation may not be proper even between tools from the same vendor. The timing tool not having the adequate physical information to implement the changes cannot accurately predict timing changes introduced by changes in cells.
The purpose of this paper is to create an automated flow to do physical-aware timing ECO with the timing tool. The flow can be used at an initial stage to implement the timing and DRC across multiple scenarios by providing PnR information to the timing tool. The early estimation with the help of timing tool can help us to reduce to turnaround time
Keywords: ECO, Physical Aware, Primetime, Innovus, MMMC

I. INTRODUCTION

With the technological advances in the VLSI industry, to meet the demands for higher performance and richer SoC features, design complexity also increased with time. To develop chips with higher device density and faster speeds the industry moved into the Deep Sub- Micron (DSM) technology domain to meet the demands and follow the Moore's Law as strictly as possible. The newer technologies brought along more complexities and challenges with them. With the number of gates in a single chip touching as high as 1 billion, the designers face a challenge to meet the foundry rules (Physical DRCs) while also enabling the devices to meet the higher frequencies.

The designers implement the design on a software (also called tools). The design is taken forward on other tools to check the integrity on the design. Different physical and timing checks are implemented to check the integrity and fix any issues found. This is normally a lengthy flow.

The adoption of a predictable ECO flow that eliminates violations in all signoff scenarios without inadvertently introducing new ones helps reduce the number of timing iterations required for final signoff. Static timing analysis tools provide predictable, signoff-accurate guidance to implementation tools with the following capabilities:

A. Fix design rule constraint (DRC), setup, and hold violations without creating new violations (therefore preventing a "ping pong" effect).
B. Perform pessimism reduction techniques such as advanced on-chip variation (AOCV), parametric on-chip variation (POCV), and path-based analysis (PBA) across all scenarios.
C. Consider physical design information to achieve best quality of results (QoR) and reduce major perturbations for designs already placed and routed.

Today's ECO guidance solutions must also be scalable to rapidly turnaround large complex designs, so design teams can quickly identify and repair numerous violations.

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II. IMPLEMENTATION FLOW AND SIGNOFF FLOW

A. Implementation Flow

The implementation flow involves the design of the chip. It also known as PnR Flow. The flow involves different steps (Floorplanning, Placement, Clock Tree Synthesis, Route) to design the product. The timing and congestion are checked at each step, prior to route step, to ensure that the figures are within certain limits and can be fixed in the signoff stage. The designer often takes the design based on technology requirements and personal experiences. The most commonly used tools for implementation flow are Innovus by Cadence and ICC by Synopsys.

B. Signoff Flow

Signoff flow involves checking the integrity of the design as per design rules and chip requirements. The Signoff flow involves the timing closure and physical checks. The tools used for signoff are called Golden tools .Timing Closure — It is also known as Static Timing Analysis (STA), to ensure that the chip meets the frequency requirements and there are no timing violations that degrade the chip's functionality. The major checks are setup, hold, transition time and capacitance. Timing closure involves use of different set of tools ensure accurate checks. The tools do checks over a large number of corners to predict functionality across different scenarios. The tools used are PrimeTime by Synopsys and Tempus by Cadence. In the DSM nodes net capacitance is as important as gate capacitance. Before timing closure, it is necessary to properly extract capacitance values, which are then used for calculating delays across the design. The tools used are StarRC by Synopsys and Quantus by Cadence Physical Checks — Known as Physical Verification. It is the process of ensuring that routing does not violate any foundry design rules and routing is done properly across the design. Certain checks also involve checking the logical functionality of the chip. The tools used are Calibre by Mentor Graphics, IC Validator by Synopsys, and Assura by Cadence.

III. ENGINEERING CHANGE ORDER (ECO)

ECO refers to the minor changes done in the netlist, after the implementation has been completed, to meet the specifications of the design. Making changes to the design in this fashion saves a lot of time in the designing process as the designer does not have to redo the implementation process. The changes may be made to standard cells directly (eg. adding an buffer or delay cells, changing cell size or vt-swap) or can be implemented by making the changes to metal layers directly.

The ECOs may be done to meet the timing of the design or may be implemented to meet the design rules or solve any other functional issues in the design. The implementation of an ECO may lead to other issues in the design This is called 'ping-pong' effect and, therefore a designer has to go through several cycles of ECO to solve all the issues in the design. Owing to the importance of the ECOs and the design time saved, all the implantation tools support

The direct changes to the design with only place & route step needed for the new modifications. The nearby nets and cells may be moved to incorporate the new changes. This may lead to new issues in the design.

As shown in Fig. 1, after implementation the signoff checks are performed on the design and the results of the checks are analysed and ECOs, is any needed, are implemented directly in to the routed design. The whole process is performed multiple times until the designs meets the specifications.

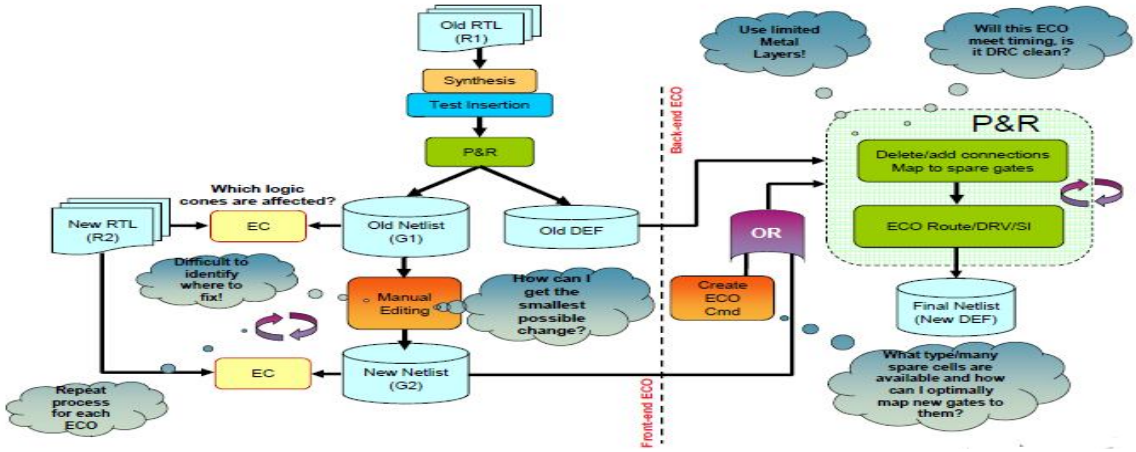

Fig. 1 ECO Cycle

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A. Correlation between Implementation Tool and Timing SignOff Tools

Implementation tools use timing-driven algorithms for placement, clock tree synthesis, and routing. They share common timing engines with signoff timing tools, of the same suite, to ensure close correlation between physical design and signoff timing results. Timing violations can still arise after place and route for the following reasons:

1) Implementation tools might not have constraints for all scenarios. This can lead to new violations during signoff as the signoff timing tool identifies violations from these new, additional scenarios
2) The extractions approximation in the implementation tools is different
3) Design reuse continues to grow, IP design teams sometimes over-constrain selected blocks to ensure operation at higher frequencies than required for the current design. While this approach enables reuse in other chips, it can lead to different timing
4) Implementation tools do not use calculation intensive Graph Based Analysis (GBA), hence leading to inaccurate timing calculations.
5) Implementation process takes longer times, as compared to signoff process, and may take even several days for the larger blocks. Therefore, the implementation tools tend to save the implementation time by reducing the accuracy of calculations

B. Multi-Mode Multi-Corner (MMMC)

MMMC analysis refers to performing STA across multiple operating modes, PVT corners and parasitic interconnect corners at the same time.

1) *Mode:* A mode is defined by a set of clocks, supply voltages, timing constraints, and libraries. Many chip have multiple modes such as functional modes, test mode, sleep mode, and etc.
2) *Corner:* A corner is defined as a set of libraries characterized for process, voltage, and temperature variations. Corners are not dependent on functional settings; they are meant to capture variations in the manufacturing process, along with expected variations in the voltage and temperature of the environment in which the chip will operate.

C. Path Delay Calculation Methods

There are two methods to calculate delay across the path - PBA and GBA

1) *Graph Based Analysis (GBA):* The tool takes the worst slew (for setup), or best slew (for hold) at all the input pins of all the combinational cells on a path. Consequently, the tool picks up worst delays (or best delays) on all nets on a path. This approach is very pessimistic but runtime is low, hence it is preferred method of delay calculation.
2) *Path Based Analysis (PBA):* The tool takes the actual slew values, so the calculated delays are actual delays. The slack calculated with this method is accurate but PBA takes a longer runtime. PBA is not utilized by implementation tools, to save runtime, but can be used by timing tools to get accurate results.

IV. PHYSICAL AWARE TIMING ECO

In standard cycle the physical data (def) is provided to the extraction tool which generates spef file, containing the parasitics information of the design. This spef file is provided to the timing tool. The timing tool uses the takes into consideration the total load seen on the driver (net capacitance + driven gate capacitance) and calculates the total delay seen because of the load. In the DSM node, the delays caused by wire parasitics are equivalent to date delays, hence play a major role in delay calculation. Since the timing tool does not have any physical information it is not able to determine the changes in the routing caused by any changes (cell sizing & buffer insertion) to the design.

The additional delay calculated is purely based on delay caused by the new cell. Any delay caused by the changes in routing or placement does not come into picture as the timing tool does not have any physical information, leading to crude estimations. These estimations may be far off from the actual values. These changes may lead to some new timing DRCs due to over-fixing of the nets or even the existing violations may not be fully fixed. Moreover, the user estimates delay for one scenario which not be feasible in other scenarios.

Therefore, the designers need to run this cycle multiple times to fix all the violations across all the scenarios, as show in Fig. 2. The user implements these fixes manually. The whole process consumes a lot of time. The routing and manual addition of cells may also need to new physical DRCs. A few extra cycles are required to fix these violations taking up a lot of time and effort.

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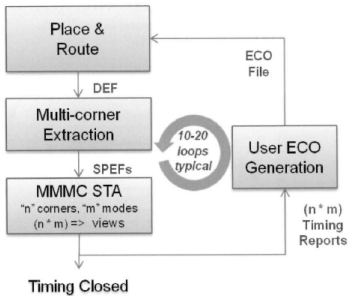

Fig. 2. Standard Timing ECO Cycle

As shown in Fig. 3, in the physical aware timing ECO flow, the timing tool is not only provided the spef from extraction tool but also the def generated from the implementation tool is provided. Also, the designer provides the physical information of the standard cells and the routing layers by reading in (library exchange format) .lef and (technology file) .tf. This enables the tool to estimate the shape and size of new cell being added along with the cells already present. The def and lef provided to the timing tool makes it physically aware. The timing tool can now estimate any physical changes in the design. The tool is able to select a proper location for the newly added cell and also able to calculate the changes in the routing in the design due to the addition of new cell. The flow also estimates any movements of other non-targeted cells that may lead to potential violations. The tool is also able to estimate the changes in routing and their effects with the help of .tf file. Any physical DRCs that may be caused by the changes are avoided beforehand by the tool. This reduces the number of cycles taken to fix the violations and subsequently reduce the time taken by the designer to manually fix the violations.

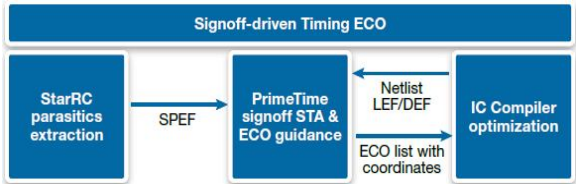

Fig. 3. Physical Aware Timing ECO Flow

Finally, the tool dumps out an ECO file along with the location of the new cells added to the design. It also dumps out the location of the cells being moved due to the ECO. The difference between the two flows are listed in table 1.

A. Use Of PrimeTime For ECO Guidance To Deliver Scalable, Resource-Efficient Results

The PrimeTime ECO guidance architecture is scalable across numerous scenarios in both runtime and capacity. This approach provides predictable results while delivering ECO guidance to implementation tools in a fast, memory efficient manner. PrimeTime ECO guidance uses the following technologies:

1) ECO timing graph
2) Composite graph view
3) Calibrated estimation

Standard ECO Flow	Physical Aware Timing ECO Flow
Contains no Physical information of the design	User provides the physical information with the help of .def. lef and .tf
The delay calculations after changes do not take into considerations the changes in routing and placement,	The delay calculations include changes in routing and placement, also calculates changes in spef due to net breaking
Sometimes it roughly estimates and may cause new violations	Calculations are accurate and cause negligible additional violations
The Complete fix requires multiple cycles (10-20 for blocks < 1M instances)	The Complete fix may be implemented in less than 5 cycles for blocks < 1M instances
The ECO consists only of names of instance and its cell type (for vt swaps and cell size) and list of buffers with their corresponding loads or drivers	The Eco file consists of new cell type and its instance along with its location and orientation (for buffer insertion)

Table 1. Comparison of Standard ECO Flow and Physically Aware Timing ECO Flow

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B. Use Of Physically Aware PrimeTime ECO To Reduce Number Of Cycles

Placement and routing topologies of a design often present opportunities to achieve the best single-pass fix rate with minimal impact to the physical design. A PrimeTime ECO technology deploys a lightweight physical interface that can populate the composite timing graph with physical information without affecting the tool performance or capacity. With the available placement information, PrimeTime ECO can consider placement congestion and blockages and provide precise ECO guidance with location. Accurate ECO timing estimation can also be achieved by separating the original net parasitics based on the target location and recalculating cell and net delays as well as crosstalk effects. ECO guidance with location and accurate timing estimation ensures predictable signoff timing closure after implementation. PrimeTime ECO also utilizes available space along the net route to increases success rates for ECO fixing in congested regions. Expanding the search space from the proximity of the driver or load pin to the entire net route vastly increases the possibility of an available space for buffer insertion. Fig. 4 shows examples where placement-aware ECO:

1) Prevents cell displacement by constraining cell upsizing to the available neighbouring free space

2) Recognizes placement blockage and inserts an ECO buffer on route

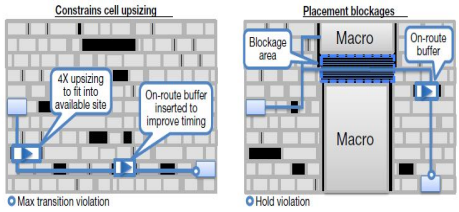

Fig. 4 Predictable Results with Placement-Aware ECO

Furthermore, expanding the solution space onto the net route is critical for achieving the optimal fix for design rule violations. Inserting buffers along the net route is the most ideal method to improve DRC violations caused by long or high fanout nets. Fig. 5, shows examples where routing-aware ECO can improve the fix rate and quality of results for max transition violations by inserting buffers according to the route topology.

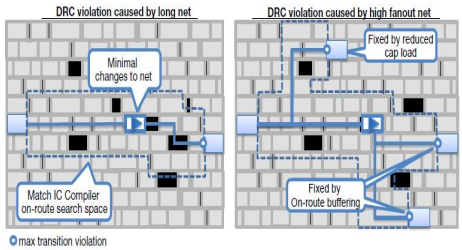

Fig. 5 Improved Fix Rate with Routing-Aware ECO

For the most challenging timing violations where no single space is available around the target pins or along the route, instead of relying on the enormously time consuming process of manual fixing by the designer, PrimeTime generates ECO guidance with the location on a target path that has the lowest placement density. During the ECO implementation legalization step, the implementation tool can move cells in this local area to create available space for the ECO changes. Fig. 6, shows an example where the ECO flow considers the placement density and successfully fixes violations with limited free space.

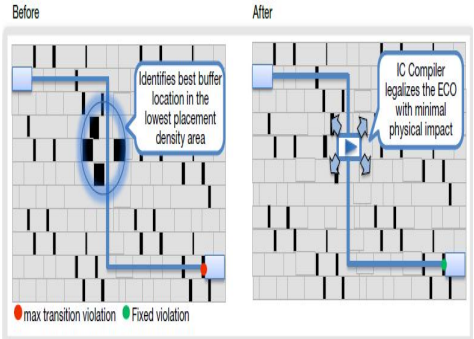

Fig. 6 Placement Density-Aware ECO for Highly Congested Regions

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While physically-aware ECO can take advantage of fixing opportunities on net routes, recognizing the voltage domain is critical for successful timing closure in advanced designs with complex voltage areas. In these designs, while driver and load pins can reside in the same voltage domain, the net route can travel through different voltage domains.

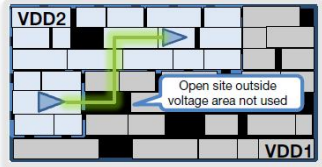

Fig. 7 Voltage Area-Aware ECO for Multivoltage Designs

Fig. 7, shows an example where PrimeTime recognizes voltage areas in multi voltage designs and avoids ECO fixes that could introduce electrical rule violations.

C. Recover Power and Area With Accurate Signoff Timing Analysis

Power consumption is a key factor of design quality, especially for energy-efficient designs that run on battery power. In the implementation flow, a designer can apply power and area recovery technologies throughout the flow from logic synthesis to post-route optimization. On timing paths with positive timing slack, power and area recovery technologies replace existing cells with lower power or smaller cells. Swapping existing cells with higher threshold voltage (Vth) cells induces no change to placement or routing while often reducing leakage power by orders of magnitude. In addition, downsizing cells not only reduces dynamic and leakage power, it also frees up valuable space for other ECO opportunities, especially in highly utilized regions.

At the timing closure stage, PrimeTime uses various pessimism reduction technologies, including path-based analysis (PBA), waveform propagation analysis, and advanced and parametric on-chip variation technologies, to uncover additional recovery opportunities. Validating the ECO guidance using the signoff timing engine in all scenarios before submission is critical to ensure successful design closure and eliminate additional ECO iteration while achieving the best possible design quality.

D. ECO Implementation with Minimum Physical Impact

Routing changes during ECO implementation can introduce unexpected impact to signoff timing due to the change in wire load or crosstalk effects.

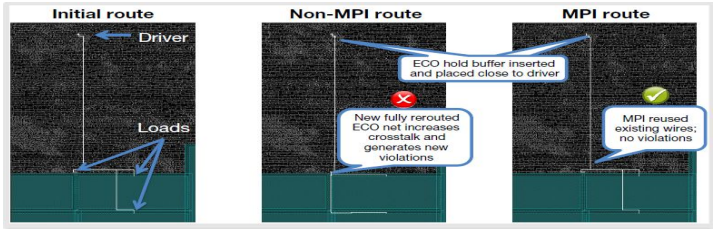

Fig. 8 ECO Routing with Physical Aware ECO Guidance

The PrimeTime physically-aware ECO guidance, which suggests ECO locations close to the target pin or original net route and restricts the route changes to only the local segment necessary for the newly inserted ECO cell as shown in Fig. 8.

By reusing the majority of the original net route, the change in wire load or crosstalk effects are minimal and highly predictable, ensuring timing closure after ECO implementation. Furthermore, in congested regions, PrimeTime physically-aware ECO can take into account fragmented free spaces and placement density surrounding the target location when determining the feasibility of a new ECO cell.

The PrimeTime ECO guidance moves existing cells to consolidate the fragmented free spaces and accommodate the new ECO cell as shown in Fig. 9.

Fig. 9 ECO Placement with Guidance

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E. Customized Physically Aware Timing ECO Flow

1) *Parameters To Be Set Before Starting Eco Fix:* The user needs to set certain variables within the design to enable the tool to ignore filler cells and use them as open sites for placement. The designer also needs the tool to enable to read parasitics for the location to enable it to estimate the changes in net delay. The designer has the flexibility to decide the prefixes for new cells and nets. The designer also has the flexibility to set the maximum size of final cell after swapping. The user can set false on certain paths to avoid fixing on them
2) *Automated ECO fixes and Suggested Sequence for Fixing:* The Primetime has inbuilt commands to do automated fixes as per user needs. It gives user the option to fix Design Rule Violations (DRV like max transition and max capacitance), setup, leakage power and hold. The user has the option to utilise PBA (Path Based Analysis) to calculate path timing for fixes. The user can use the method for fixing - cell sizing (includes cell sizing as well as Vt swap) and cell addition (buffer or inverter pair). The user can define the cells to be used for insertion. For leakage fixing the user has the option to set the priority of the available Vt to be swapped to. While doing any fixes the Primetime avoids trying to setup any further on a path while fixing it. The user has the option to set the allowed setup slack on the net if needed be. The user can give option to use only open sites or any occupied sites (for congested designs) for cell addition.

The user must update timing after every change to reflect the change across the design and the new timing.
The priority for different fixes is as per following:

a) DRV: The user can use cell sizing and cell addition for this. Setup and hold maybe altered need (can provide override).
b) Setup: Uses cell sizing and Vt swap for fix. Does not violate any DRVs while fixing
c) Leakage Fix: Uses Vt swapping for fixing. Does not degrade timing but may fix hold.
d) Hold: Uses cell sizing, Vt swapping and buffer (or inverter pair) insertion.

Avoids any setup or DRV degradation (can provide override for setup).

3) *Writing out ECO file and Implementation:* The designer can write out the changes in a file in different formats. Here, the timing tool does not support the ECO format of implementation tool. Hence, post processing was required to convert to the format of implementation tool (Tcl script). For implementation, the designer needs to first delete any existing filler cells in the design and set the implementation tool to ECO mode. Then read in the ECO file and refine the placement (if needed) and reroute the affected nets.

F. Limitations of Physically Aware Timing ECO Flow

As there are multiple tools available for both timing and implementation tool from different EDA companies, there may be compatibility issues between the implementation tool and timing tool. Some of the features described earlier may not function properly. Hence proper care needs to be taken while implementing the ECO files from the timing tool. Standard file formats like DEF, LEF, etc. do not change across the VLSI industry so can be used without any changes.
The timing tool will avoid affecting the setup slack of any path, unless any margin is available, or override used. This may cause certain path to remain unfixed and need to
be manually fixed. If the tool does not find sufficient resources, for fixing, for any path, it will not fix those paths. PrimeTime will try to avoid disturbing the route as much as possible but it still may create some new physical DRCs leading to extra ECO cycles. PrimeTime may not be able to differentiate the filler cells from the standard tools. Hence, filler cells may have to be removed from the DEF.

V. RESULTS

A. Design Overview

Frequency	1GHz
No. of macros	68
No. of Standard cells	1.2M
Utilisation	0.65
No. of PVT Corners	24
No. of Modes	test and func
Power domains	1

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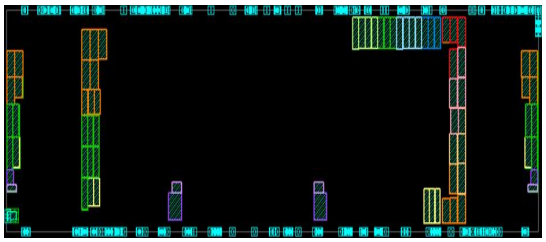

Fig. 10 Design Overview

B. Results Before and After First Round of Physically Aware Timing ECO Flow

	Before	After
TNS	1.2ns	800ps
WNS	80ps	40ps
No. of Failing Endpoints	515	123
No. of Failing Transitions on regtoreg path	189	12
Worst Violating Transition Value on regtoreg paths	400ps	42ps
No. of Failing Capacitance on regtoreg paths	121	13
Worst Violating Capacitance Value on regtoreg paths	103pF	18pF
Leakage Power	9.871e-07(0.52%)	7.001e-07(0.41%)
No. of Physical DRCs	713	718

Table 2 Comparison of Results Before and After First Round of Physically Aware Timing ECO Flow

No. of cells added = 97
No. of cells swapped (or sized) = 29
No. of cycles required with Standard Flow = 8
No. of cycles required with Physically Aware Timing ECO Flow = 4

Fig. 11 Snapshot of few Newly Added Cells

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VI. CONCLUSION

The Physical aware Timing ECO flow has advantages over the conventional ECO flow as it reduces the convergence time. The major challenges are an integration of ECO script for the timing and implementation tool.

Future work can include merging the timing tool into the implementation tool to get an accurate estimation in the implementation stage and optimize accordingly.

VII. ACKNOWLEDGMENT

First and foremost, I would like to express my deepest gratitude to Mr. Ankur Shukla, Sr. Engineer, Qualcomm for his invaluable support, guidance, motivation and encouragement throughout the period of this work.

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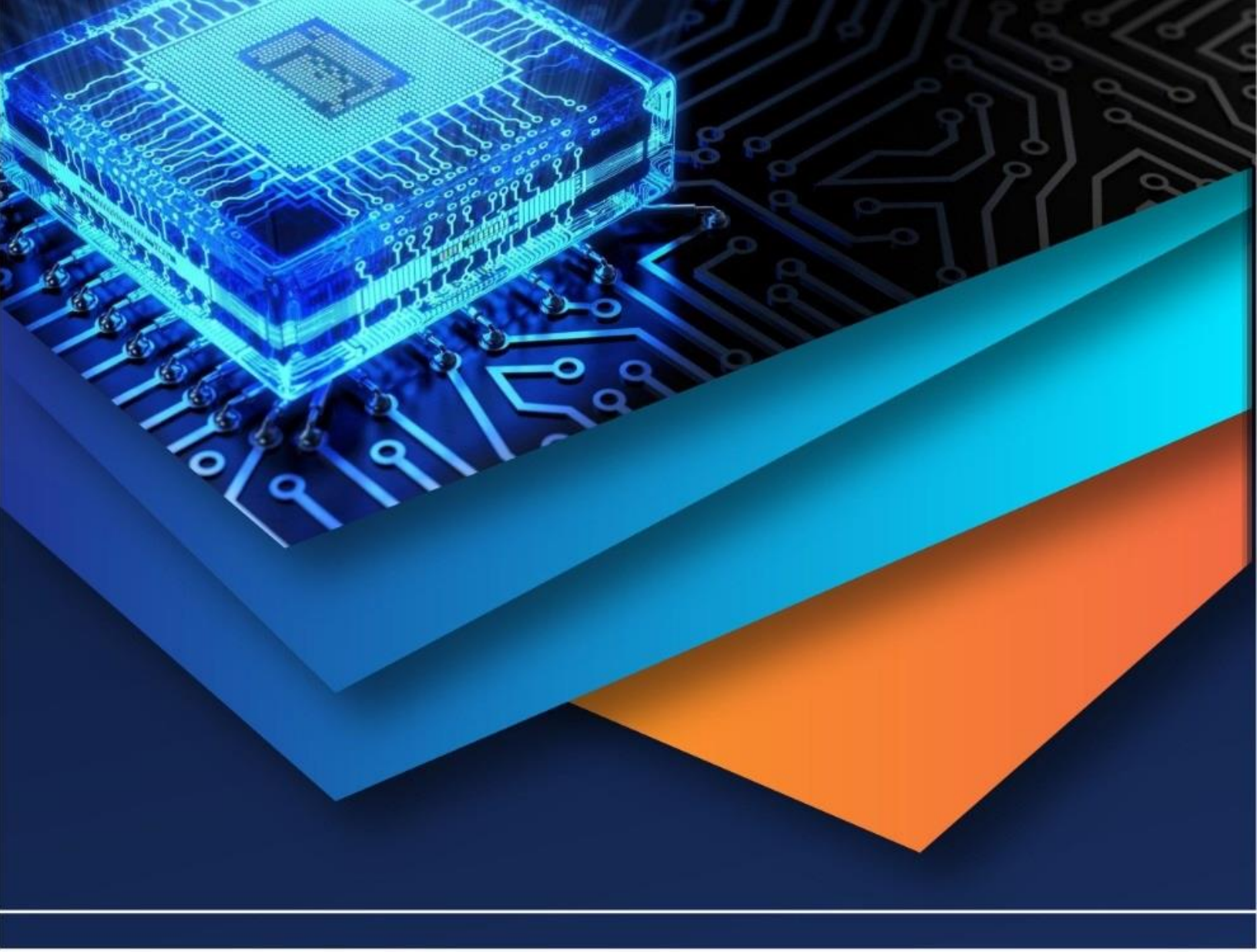

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