iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 7 **Issue:** IX **Month of publication:** September 2019

DOI: http://doi.org/10.22214/ijraset.2019.9089

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue IX, Sep 2019- Available at www.ijraset.com

A Practical Approach to Layout versus Schematic (LVS)

Swasti Pujari[1], Smitha M R[2], Amit Singh[3], Mukul Anand[4]
[1, 2, 3]*Engineer, Einfochips Ltd. (An Arrow Company)*
[4]*Technical Lead, Einfochips Ltd. (An Arrow Company)*

Abstract: ***ASIC design implementation has become progressively complex and sophisticated with deep down the submicron technologies. Multiple processor cores, I/O s, several types of memories, analog circuits, and digital synthesized logic are being designed and implemented onto the same chip. Advanced IP integration proficiencies are needed to realize today's complex systems-on-chip designs and to keep up with the high demand in the semiconductor market. Ensuring product reliability to meet design goals and to achieve good yield is of significant and continuous concern.***
Layout Versus Schematic (LVS) is process in the Chip Design and implementation that ensures if the layout (physical connectivity) of a specific Circuit matches with the actual Schematic (Circuit Diagram) of the design or not.
Keywords: LVS, Calibre, GDSII, Circuit Design, Schematic.

I. INTRODUCTION

Layout vs Schematic (LVS) check is performed in three basic steps:

1) *Extraction:* The tool takes GDSII file containing all the layers and uses polygon-based approach to determine the components like transistors, diodes, capacitors and resistors and also connectivity information between devices presented in the layout by their layers of construction. All the device layers, terminals of the devices, size of devices, nets, vias and the locations of pins are defined and given unique identification.
2) *Reduction:* All the defined information is extracted in the form of netlist.
3) *Comparison:* The extracted layout netlist is then compared to the netlist of the same stage using the LVS rule deck. In this stage the number of instances, nets and ports are compared. All the mismatches such as shorts and opens, pin mismatch etc. are reported. The tools also check topology and size mismatch.

A. *Inputs for LVS*

The following Design inputs are required for running LVS as depicted in Fig. 1.

1) Graphical Database System (GDS) layout database of the design
2) Schematic Netlist of the design
3) Cell definition file consisting of Intellectual property files and standard cells, Pad reference file.
4) LVS rule deck: - a set of codes that is written in Standard Verification Rule Format (SVRF) or TCL Verification Format (TVF).

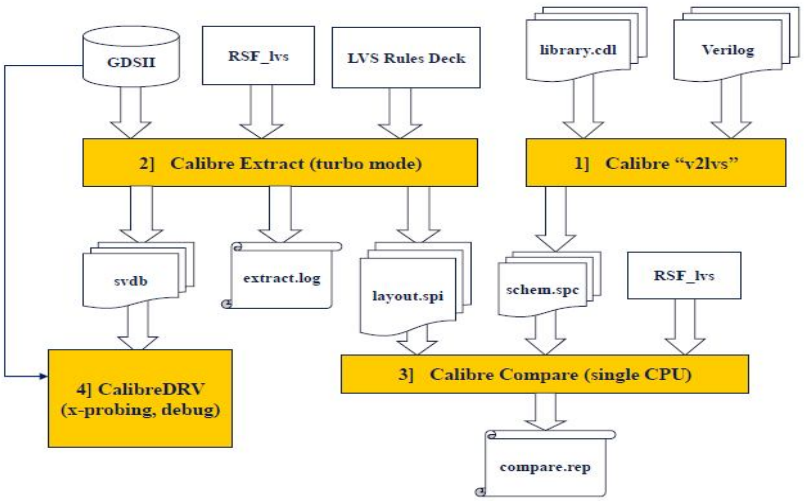


Fig. 1. Mentor Graphics Calibre LVS Flow – Overview

a) Step 1:- Generating Schematic spice Netlist (v2lvs)

i) LVS Comparison is done using SPICE Netlist format as shown in Fig. 2.

ii) Input: Verilog + CDL

iii) 'v2lvs' converts the Verilog into SPICE,

iv) CDL Netlist will be added as INCLUDE.

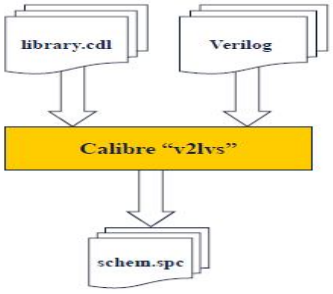


Fig. 2. Generating Schematic spice Netlist

b) Step 2:- Extracting Layout data (GDS2SPICE)

i) LVS rules to extract connectivity is an input as shown in Fig. 3.

ii) PWR – GND detected at this stage.

iii) LVS ISOLATE SHORTS YES – This switch gives us the PWR- GND Shorts if any.

iv) View with RVE as DRC database and fix it before LVS compare

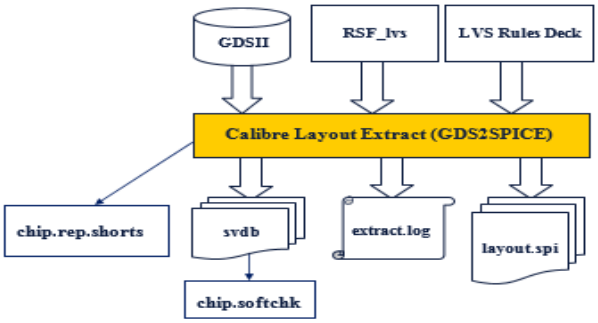


Fig. 3. Extracting Layout data (GDS2SPICE)

c) Step 3:- Comparing Schematic and Layout (NVN)

The Layout & Schematic SPICE files are compared and a report and below files are generated as the output as depicted in Fig. 4.

i) LVS.rep - Hierarchical LVS report

ii) SVDB (used by Calibre RVE) is a binary connectivity database containing all LVS information.

iii) LVS report - having the Schematic / Layout netlists.

iv) Contains the Probing / Cross probing information for all the nets.

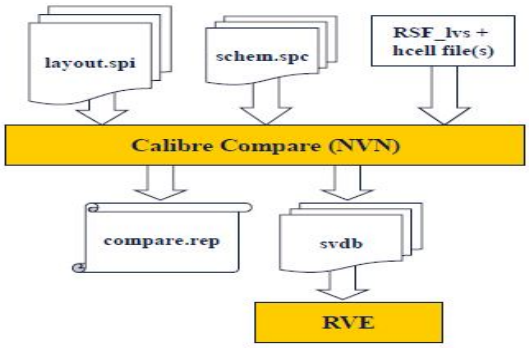


Fig. 4. Comparing Schematic and Layout (NVN)

B. LVS output files

1) lvs.rep: ASCII

a) Summary of comparison results (CORRECT/INCORRECT)
b) Detailed cell based information
c) Device extraction, connect Information
d) Runtime, number of executed rules

2) lvs.rep.ext: ASCII

a) Label report

3) lvs.log: ASCII

a) Copy of used setup
b) Cell names/layer info
c) Rule deck commands, rules info
d) Hierarchy mod. Information (expand cell, flatten cell, …)
e) Comparison Information (device count, net count, …)

4) svdb: BINARY DB

a) Probing Database for RVE tool

C. Calibre LVS report – Overview

1) Report format has two columns - LAYOUT :: SCHEMATIC
2) Header - gives a cell summary and reports CORRECT or INCORRECT
3) Hierarchical report
a) LVS information included for every cell
b) Devices/ports/nets BEFORE and AFTER transformation
c) Common error types are classified as follows:

i) Incorrect nets
ii) Incorrect instances
iii) Property errors
iv) Detailed instance connections

4) Use the detailed instance connections to debug the ERROR
a) Use layout coordinates to correlate with the netlist

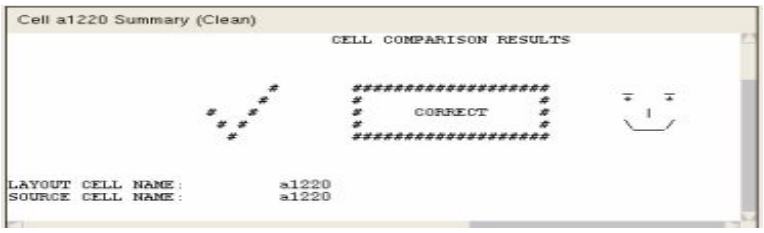


Fig. 5. Calibre LVS report – Overall comparison results

CELL SUMMARY

Result	Layout	Source
CORRECT	R150_CSAN12	R150_CSAN12
CORRECT	R150_CSBUF16	R150_CSBUF16
CORRECT	R150_CSBUF16	R150_CSBUF16
CORRECT	R150_CSCLK14	R150_CSCLK14
CORRECT	R150_CSEO	R150_CSEO
CORRECT	R150_CSFD2QSV	R150_CSFD2QSV
CORRECT	R150_CSHA1	R150_CSHA1
CORRECT	R150_CSIV1	R150_CSIV1
CORRECT	R150_CSIV2	R150_CSIV2
CORRECT	R150_CSTSD4	R150_CSTSD4
INCORRECT	PMMTRCM	PMMTRCM
INCORRECT	pll_clock_top	pll_clock_top

Fig. 6. Calibre LVS report – Hierarchical summary

```
INITIAL NUMBERS OF OBJECTS
--------------------------

                  Layout     Source          Component Type
                  ------     ------          --------------
Ports:              1187       1187

Nets:             159268     159268

Instances:        158871     158872     *     MN (4 pins)
                  159215     159216     *     MP (4 pins)
                  ------     ------
Total Inst:       318086     318088

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                  Layout     Source          Component Type
                  ------     ------          --------------
Ports:              1187       1187

Nets:             157418     157418

Instances:        149915     149915          MN (4 pins)
                  150259     150259          MP (4 pins)
                  ------     ------
Total Inst:       300174     300174
        * = Number of objects in layout different from number in source.
```

Fig. 7. Calibre LVS report – Transformation

```
                    Matched      Matched      Unmatched      Unmatched      Component
                     Layout       Source         Layout         Source      Type
                    -------      -------      ---------      ---------      ---------
  Ports:               1187         1187             0              0
  Nets:              157418       157418             0              0
  Instances:         149915       149915             0              0      MN(N)
                     150259       150259             0              0      MP(P)
                    -------      -------      ---------      ---------
  Total Inst:        300174       300174             0              0

o Statistics:

  28148 layout mos transistors were reduced to 10236.            1850 connecting nets were deleted.
    14212 mos transistors were deleted by parallel reduction.
    3700 mos transistors and 1850 connecting nets were deleted by split-gate reduction.
  28152 source mos transistors were reduced to 10238.            1850 connecting nets were deleted.
    14214 mos transistors were deleted by parallel reduction.
    3700 mos transistors and 1850 connecting nets were deleted by split-gate reduction.
```

Fig. 8 Calibre LVS report – Matching device summary

D. Calibre LVS Report – Correspondence points

1) Labels that correspond to netlist ports listed are here and all points should correspond.

2) Ports give Calibre a starting point for connectivity. It is important to first debug any ports that are mismatching, especially power/ground.

```
        o Initial Correspondence Points:

Ports:          VDDN GND X_TA_TEST_EN ES_SINFO_ADDR_11[1] ES_SINFO_ADDR_21[9] ES_SINFO_ADDR_16[2]
                ES_SINFO_ADDR_17[1] ES_SINFO_ADDR_20[0] ES_SINFO_ADDR_7[10] ES_SINFO_ADDR_3[7]
                ES_SINFO_ADDR_2[3] ES_SINFO_ADDR_2[4] ES_SINFO_ADDR_3[0] ES_SINFO_MULTI[15] O_POWER_DOWN[1]
                O_ENA_FAC_LOOP[0] PSE_RDATA[0] PSE_RDATA[12] ES_RDATA[13] ES_RDATA[24] SP_LOS[1]
                PS_O_SYNC_RESET[2] PS_DOUT_0[2] PS_DOUT_0[9] PS_DOUT_1[14] PS_DOUT_1[5] PS_DOUT_1[0]
                PS_DOUT_1[13] SP_LOF[1] O_ENA_EQU_LOOP[0] PS_DOUT_1[10] PS_DOUT_0[14] O_ENA_EQU_LOOP[2]
                PS_DOUT_1[11] PS_DOUT_1[6] PS_DOUT_1[16] PS_DOUT_2[2] PS_DOUT_1[9] PS_DOUT_0[11]
                PS_DOUT_1[4] PS_DOUT_1[3] PS_DOUT_0[15] PS_DOUT_1[1] PS_DOUT_1[12] PS_DOUT_2[0]
                PS_DOUT_0[0] PS_DOUT_0[16] PS_DOUT_1[15] PS_DOUT_1[8] PS_DOUT_0[1] PS_DOUT_2[1]
                O_ENA_FAC_LOOP[2] SCANOUT_1 ES_SINFO_ADDR_0[0] FF_MULTI_DE_QUEUE[22]
```

Fig. 9. Calibre LVS report – Correspondence points

E. Calibre LVS report – LVS Mismatches

The Typical LVS mismatches are as follows:

1) Different number of ports
2) Different number of nets
3) Connectivity errors
4) Cells with non-floating extra pins
5) Layout gate problems
6) Incorrect Supply nets
7) Property errors
8) Problems with Source netlist

F. Calibre LVS report - LVS Mismatch, summary

1) First of all, check the overall comparison results.
2) This will contain a summary of all LVS errors and warnings.
3) Full error details appear later in the report.

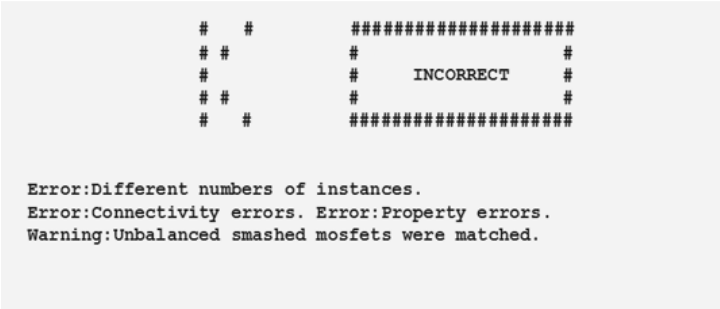


Fig. 10. LVS Mismatch, summary

G. Calibre LVS report - LVS Mismatch, Device/net Problem

Check the device comparison statistics.

1) This section will detail exactly what type of devices are mismatching and by how many numbers.
2) The first priority is to check that the number of ports match.
3) If there is a mismatch of one or two ports and all N-types or P-types or all of both are mismatching, then it is likely that the power supply connections need to be debugged.

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	1187	1187	0	0	
Nets:	157417	157417	1	1	
Instances:	149915	149915	1	0	MN(N)
	150258	150258	0	1	MP(P)
Total Inst:	300173	300173	1	1	

Fig. 11. *LVS Mismatch, device/net problem*

H. Calibre LVS report - LVS Mismatch, Open/Short

1) Discrepancy #1 - SHORT

a) Source nets “QUEUE_8[10]” & “QUEUE_9[1]” are shorted together in the layout to form the single layout net “QUEUE_8[10]”.

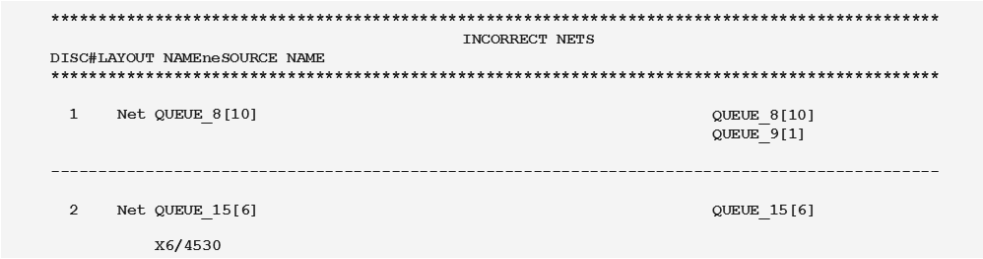
2) Discrepancy #2 - OPEN

a) Layout nets “QUEUE_15[6]” & “X6/4530” should be connected together so that they correspond to the single source net “QUEUE_15[6]”.

I. Calibre LVS report - LVS Mismatch, layout Gates

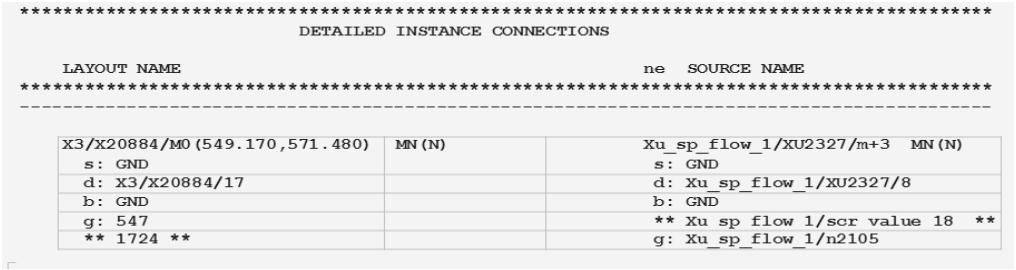
1) Debug Mismatched layout Gates first.

2) Look in the Detailed Instance Connections section of the report



```
*****************************************************************************************
                                    INCORRECT NETS
DISC#LAYOUT NAMEneSOURCE NAME
*****************************************************************************************

  1    Net QUEUE_8[10]                                          QUEUE_8[10]
                                                                QUEUE_9[1]

-----------------------------------------------------------------------------------------

  2    Net QUEUE_15[6]                                          QUEUE_15[6]

       X6/4530
```

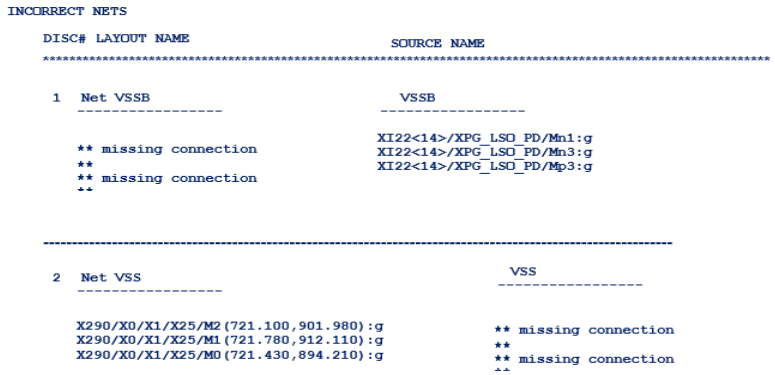
Fig. 12. LVS Mismatch, OPEN/SHORT



```
*****************************************************************************************
                        DETAILED INSTANCE CONNECTIONS

    LAYOUT NAME                                          ne  SOURCE NAME
*****************************************************************************************
-----------------------------------------------------------------------------------------

  X3/X20884/M0(549.170,571.480)  MN(N)          Xu_sp_flow_1/XU2327/m+3  MN(N)
    s: GND                                       s: GND
    d: X3/X20884/17                              d: Xu_sp_flow_1/XU2327/8
    b: GND                                       b: GND
    g: 547                                       ** Xu sp flow 1/scr value 18  **
    ** 1724 **                                   g: Xu_sp_flow_1/n2105
```

Fig. 13. *LVS Mismatch, layout Gates*

J. Calibre LVS report - LVS Mismatch, Incorrect Supply Nets



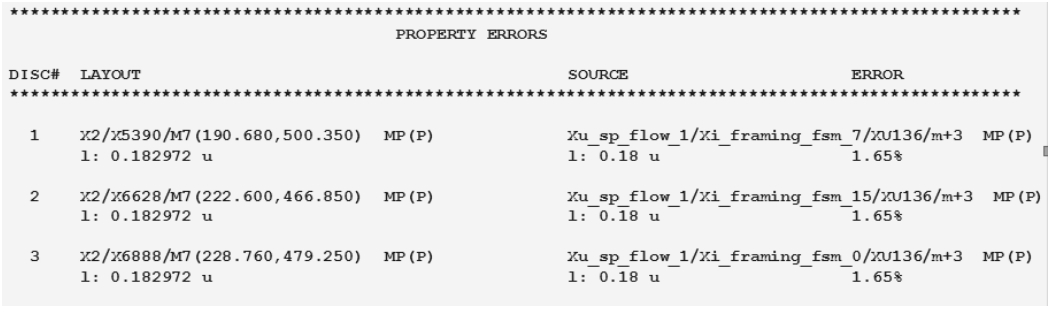
```
INCORRECT NETS

    DISC# LAYOUT NAME                              SOURCE NAME
*****************************************************************************************

  1  Net VSSB                                      VSSB
     ------------------                            ------------------

     ** missing connection                        XI22<14>/XPG_LSO_PD/Mn1:g
     **                                           XI22<14>/XPG_LSO_PD/Mn3:g
     ** missing connection                        XI22<14>/XPG_LSO_PD/Mp3:g
     **

-----------------------------------------------------------------------------------------

  2  Net VSS                                       VSS
     ------------------                            ------------------

     X290/X0/X1/X25/M2(721.100,901.980):g          ** missing connection
     X290/X0/X1/X25/M1(721.780,912.110):g          **
     X290/X0/X1/X25/M0(721.430,894.210):g          ** missing connection
                                                   **
```

Fig. 14. *LVS Mismatch, Incorrect Supply Nets*

K. Calibre LVS report - LVS Mismatch, Property Errors

1) When Calibre extracts circuitry from the layout, it also extracts device size information.

2) Any device parameters that do not match the sizes specified in the netlist are listed in this section of the LVS report.



```
*****************************************************************************************
                                  PROPERTY ERRORS

DISC#  LAYOUT                                        SOURCE                      ERROR
*****************************************************************************************

  1    X2/X5390/M7(190.680,500.350)  MP(P)          Xu_sp_flow_1/Xi_framing_fsm_7/XU136/m+3  MP(P)
       l: 0.182972 u                                l: 0.18 u                   1.65%

  2    X2/X6628/M7(222.600,466.850)  MP(P)          Xu_sp_flow_1/Xi_framing_fsm_15/XU136/m+3  MP(P)
       l: 0.182972 u                                l: 0.18 u                   1.65%

  3    X2/X6888/M7(228.760,479.250)  MP(P)          Xu_sp_flow_1/Xi_framing_fsm_0/XU136/m+3  MP(P)
       l: 0.182972 u                                l: 0.18 u                   1.65%
```

Fig. 15. *LVS Mismatch, Property Errors*

II. CALIBRE LVS DEBUGGING AND VERIFICATIONS METHODS

Many Debugging methods can be used to verify the LVS results:

A. LVS Black Boxing
B. Layout / Schematic Black Boxing
C. Short isolator (Short locator)
D. Layout/Schematic cross probing
E. Virtual connection
F. Exclude Cells
G. LVS report Options
H. Spice netlist Manipulation
I. [Spice netlist viewer]

III.LVS BLACK BOXING

1) Black boxing can filter out cells from the LVS
2) Connectivity is checked to the cell boundary and pins, inside not
3) The following options are set in the RSF file…
a) *"LVS BOX "cell name" (Schematic black boxing)*
i) Full layout extraction is done first
ii) Black boxing works with schematic cell names
iii) Problems if shorts/stamping errors inside the cell (no clean netlist to use)
b) *#Define Layout Box (Layout black boxing)*
i) Enhancement to LVS BOX command
ii) Exclude full cell contents from LVS layout extraction, abstract kept
iii) That means block can truly be filtered and cell internal problems will not impact top level
iv) Very useful in case of shorts or stamping errors
v) Can also be used to debug hierarchical LVS errors

A. Short Isolator

1) "LVS Isolate Shorts yes By Layer" (rules)
2) "Hierarchical Short Isolation started" (log file)
3) "*.lvs.rep.shorts" is output (DRC type database)
4) Use CalibreRVE to graphically find the short location
5) RVE use different colours for each shorted net.• User could define which part of the short DB is related to which net, else the net part is defined as "unknown" (>=2008r01)
6) Watch the date stamp.

B. LVS cross Probing Using RVE

1) Calibre cross probing information is contained in the "SVDB" database

C. LVS Debugging methods – Others

1) *Virtual Connect*
a) Use Virtual connect command to get one step further, special for Supply shorts (limited usage for final verif.)
2) *Exclude Cell*
b) Remove cells complete from LVS run (for final verif. NOT ALLOWED)
3) *LVS Report Options*
a) Reduce/Enhance LVS report informations
b) E.g.: NOK option remove all CORRECT entries
4) *Spice Netlist Manipulation*
a) Local manipulation of Input netlists to reproduce an error on layout or schematic side (for final verif. NOT ALLOWED)

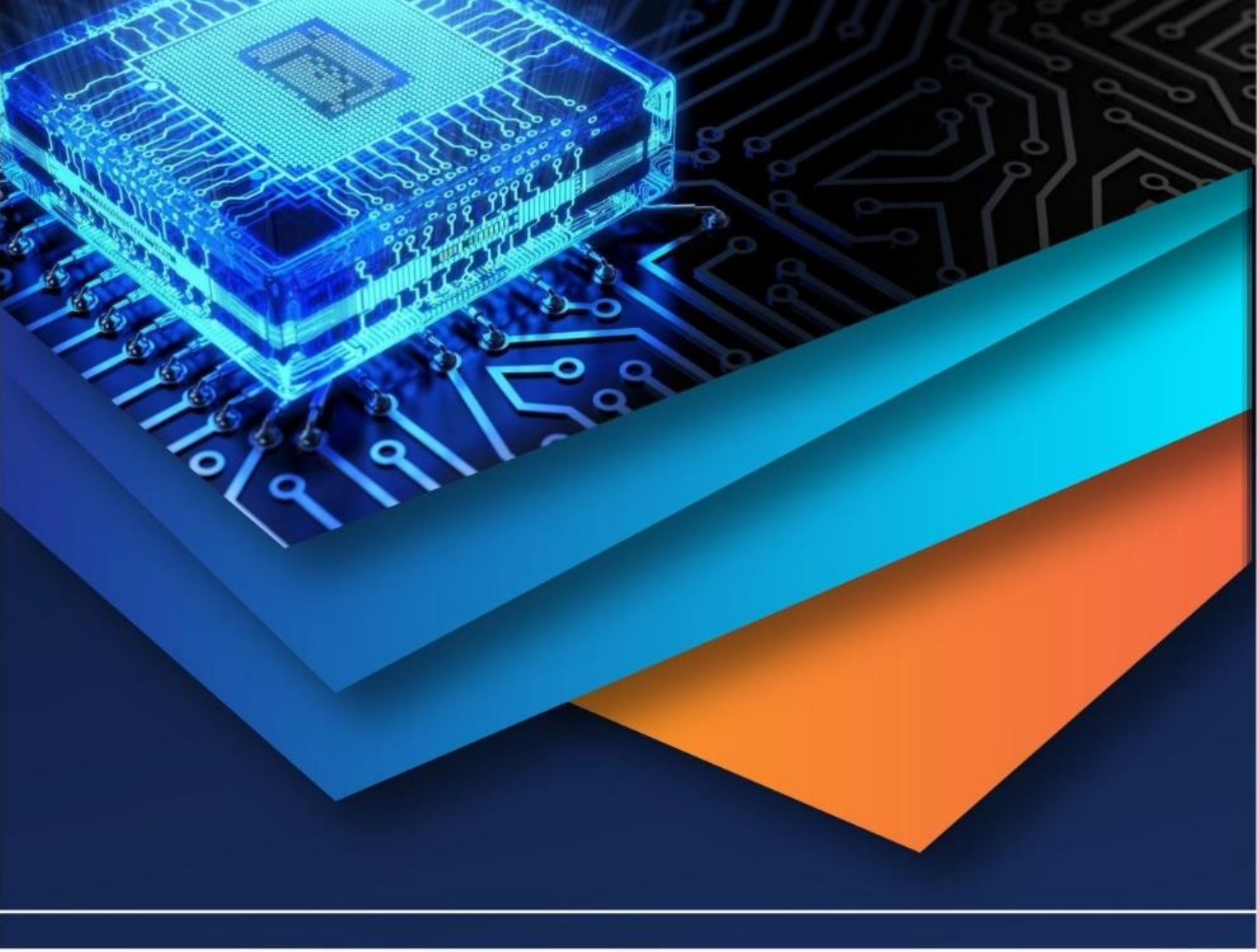
5) General Hints

a) make sure that LVS extraction of layout is clean first (OPEN/SHORT)

b) Power to Ground shorts errors must be fixed before Compare

REFERENCES

[1] ICCII User Guide.
[2] Calibre User Guide.
[3] https://en.wikipedia.org/wiki/Layout_Versus_Schematic
[4] EE5323 VLSI Design – https://www.people.ece.umn.edu
[5] https://www.edn.com/design/integrated-circuit-design/4418390/An-insight-into-layout-versus-schematic



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY