iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 7 **Issue:** X **Month of publication:** October 2019

DOI: http://doi.org/10.22214/ijraset.2019.10040

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue X, Oct 2019- Available at www.ijraset.com

Implementation of Forward Error Correction Encoder for DVB-S2

Ketineni Sravanty[1], Dr. Baswaraj Gadgay[2], Veeresh Pujari[3]
[1]*PG Student Dept. Of VLSI Design & Embedded Systems VTU Centre for PG studies, Kalaburagi, Karnataka, India*
[2]*PG Co-ordinator /Regional Director VTU Centre for PG Studies, Kalaburagi, Karnataka, India*
[3]*Professor VTU Centre for PG Studies Kalaburagi, Karnataka, India*

Abstract: ***The FEC encoder for DVB-S2 systems consist of three blocks, the BCH encoder or the outer encoder, the LDPC encoder or the inner encoder, and the Bit Interleaver. This paper elaborates upon the design and implementation of FEC encoder for DVB-S2 systems. FECFRAMES, i.e., to generate an output of 64,800 bits.***
The design described here implements DVB-S2 frame structure for transport stream, single input with constant code rate of 1/2 and QPSK modulation, with a roll-off of 0.20. A Xilinx Virtex-5 FPGA package XC5VFX130T board is used to implement this design as this FPGA is also available in radiation tolerant version.
Keywords: FEC, LDPC encoder, DVB-S2 System, Xilinx Virtex-5 FPGA, Bit Interleaver.

I. INTRODUCTION

Digital Video Broadcasting – Satellite – Second Generation (DVB-S2), the successor of DVB-S system is a digital television broadcast standard. There are two major changes in DVB-S2 from the previously used DVB-S standard. Firstly, DVB-S2 makes use of a very powerful coding scheme based on a modern LDPC code. To reduce the encoding complexity, the LDPC code has a special structure, called the Irregular Repeat-Accumulate Codes. Secondly, in DVB-S2 systems, Variable Coding and Modulation (VCM) and Adaptive Coding and Modulation (ACM) were added that would dynamically change the transmission parameters to optimize the bandwidth utilization parameters. Error control coding applications have grown rapidly in the past several years in various field of communication and information storage mechanism.

There are number of techniques of error correction based on applied mathematics which correct various types of errors. Still no error correcting code is available which can correct all the random errors and burst errors. When number of errors was increased designed codes turn out to be inefficient. Small error correction codes with desired correction capabilities can be easily developed but with large error correction capability; developing a code is real practical problem. The proposed system utilizes FEC encoders that provide forward error correction of the codes in the receiver itself. The FEC encoder consists of BCH encoder, LDPC encoder followed by the bit interleaver.

II. LITERATURE SURVEY

In [1] DVB-T2 (second generation terrestrial digital video broadcasting) employs LDPC (Low Density Parity Check) codes combined with BCH codes, which has a better performance in comparison to convolutional and Reed-Solomon codes used in other OFDM-based DVB systems. However, the current FEC layer in the DVB-T2standard is still not optimal. In this paper, we propose a novel error correction scheme based on fountain codes for OFDM-based DVB systems. The key element in this new scheme is that only packets are processed by the receiver which has encountered high-energy channels.

In [2] the paper presents typical satellite channel model consistent with the targeted applications of the aforementioned standard is assumed. In particular, non-linear pre-compensation as well as synchronization techniques are described in detail and their performance assessed by means of analysis and computer simulations. The proposed algorithms are shown to provide a good trade-off between complexity and performance and they apply to both the broadcast and the profiles, the latter allowing the exploitation of adaptive coding and modulation (ACM). Finally, end-to-end system performances in term of BER versus the signal-to-noise ratio are shown as a result of extensive computer simulations. The whole communication chain is modelled in these simulations, including the BCH and LDPC coder, the modulator with the pre-distortion techniques, the satellite transponder model with its typical impairments, the downlink chain inclusive of the RF-front-end phase noise, the demodulator with the synchronization sub-system units and finally the LDPC and BCH decoders

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue X, Oct 2019- Available at www.ijraset.com

In [3] The DVB-S2 standard second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications (DVB-S2)) has been conceived for several satellite broadband applications: Television Broadcast Services, Interactive Services including Internet Access by consumers, Professional Applications such as Digital Satellite News Gathering (DSNG) and TV distribution, data trunking. This paper focuses on the profiles supporting interactive type of services, for which Adaptive Coding and Modulation (ACM) has been included in the new generation of the standard. Following the DVB-S2 specifications, a number of modem configurations and tools are made available for implementing ACM in interactive systems. However, the different approaches have important impacts on the design of the system architecture and of the scheduling/resource management algorithms. The aim of the present contribution is providing a first discussion on the critical issues at system and MAC level, which need to be addressed when implementing a DVB-S2 ACM system. A general introduction to ACM is also provided, as well as an illustration of the key elements included in the DVB-S2 standard for supporting physical layer adaptively.

III. PROPOSED DESIGN METHODOLOGY

A. Functional Block Diagram Of Dvb-S2 System

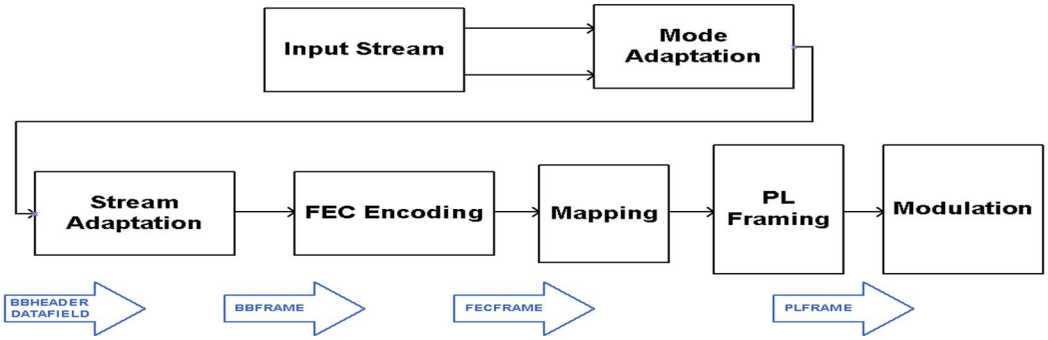


Fig. 1 DVB-S2 SYSTEM

B. Proposed FEC Encoder For Dvb-S2 Systems

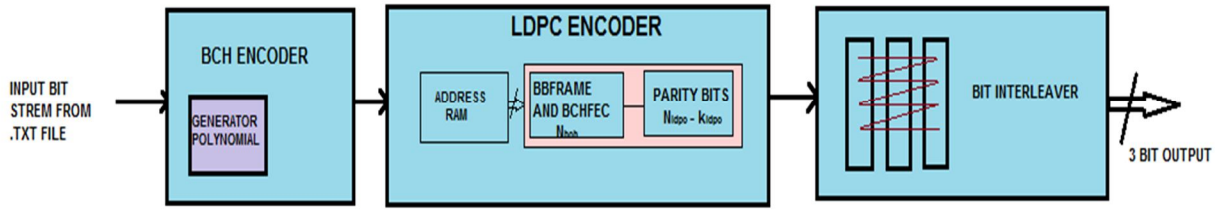


Fig.2 FEC Encoder block for DVB-S2 System for rate ½

FEC is used to control errors during data transmission over noisy or unreliable channels. It uses redundancy to detect and correct errors up to a certain extent. The FEC encoder block for a DVB-S2 system is further divided into three sub-blocks, the BCH encoder or the outer encoder, the LDPC (Low Density Parity Check) encoder or the inner encoder and bit interleaver. The input to the FEC encoder block first goes through the outer or BCH encoder which is a t-error correcting code, i.e., it can correct up to t errors in the message signal.

The BCH encoder generates some parity bits which are appended with the original message signal and is then sent to the LDPC encoder. LDPC encoder again generates another set of parity bits and they are appended with the signal input to the LDPC encoder block. Finally, depending upon the modulation scheme and the rate of LDPC coding, the output of the LDPC encoder is sent to the bit interleaver which generates the final FECFRAME, which is the encoded message signal.

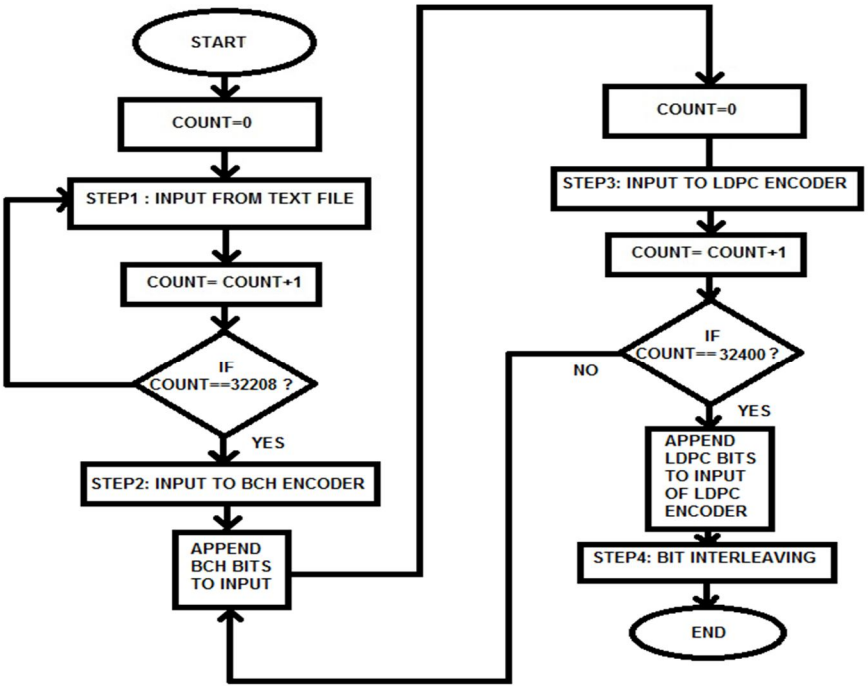


Fig. 3 Flow Chart of FEC Encoder

Implementation of FEC encoder has been done by considering the following values rate = 1/2, K_{bch} = 32208, N_{bch} = K_{ldpc} = 32400, t = 12, N_{ldpc} = 64800 and q = 90. Here q represents the number of row and each row is consists of 360 bits.

To perform FEC encoding of a data, first the data bits are read out from the text file, as seen in the first step of the flowchart. For rate = 1/2, we have 32,208 input bits. So, once all the 32,208 input bits are read out, the entire block of the input data is sent to the BCH encoder where 192 additional BCH bits are generated and appended to the block of input data.

After that, the block of BCH coded data is sent to the LDPC encoder where it generates additional 32,400 bits which are divided into 90 rows and appends them to the block of BCH coded data, thus generating LDPC coded data block. For modulation schemes other than QPSK, the block of LDPC coded data is sent to the bit interleaver as seen in the step 4 for the flow chart. The output of the bit interleaver is the final FEC coded data, i.e., the FECFRAME.

IV. RESULTS

The Simulated result of the proposed Implementation of Forward Error Correction Encoder for DVB-S2 is illustrated here. Xilinx 14.7 is used for synthesis and simulation of the proposed architecture. For implementation purpose Xilinx Virtex-5 FPGA is used. The RTL view of the proposed system is shown in the figure below.

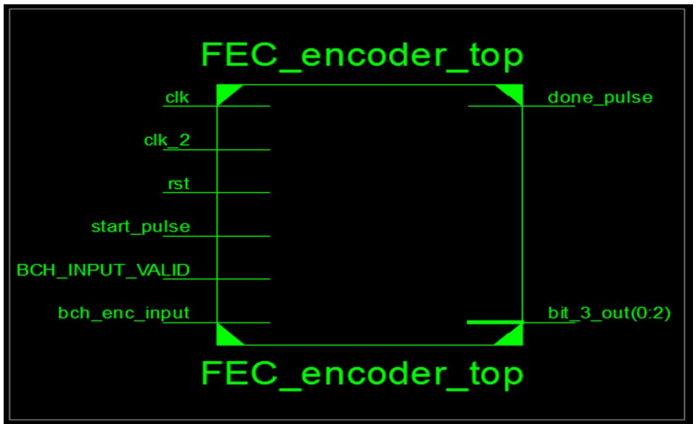


Fig. 4 RTL of FEC encoder top view

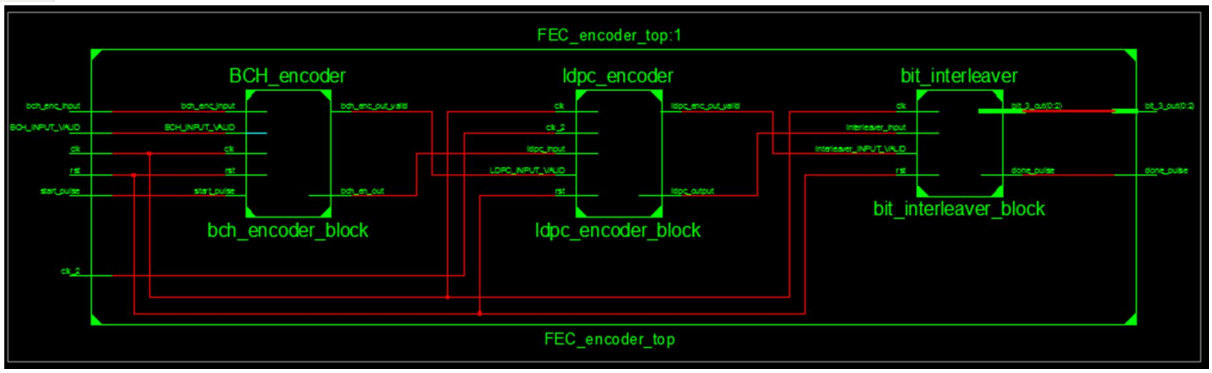


Fig. 5 RTL schematic of proposed FEC encoder

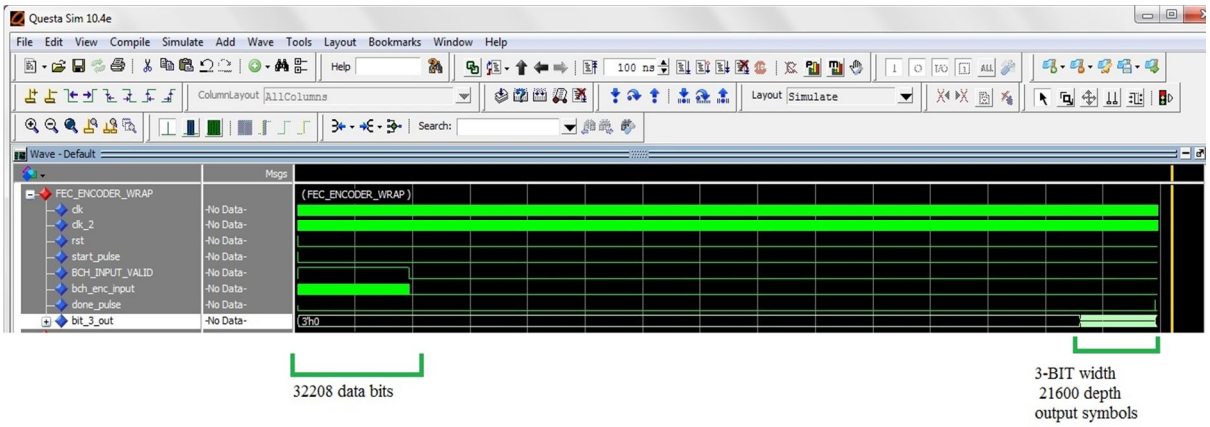


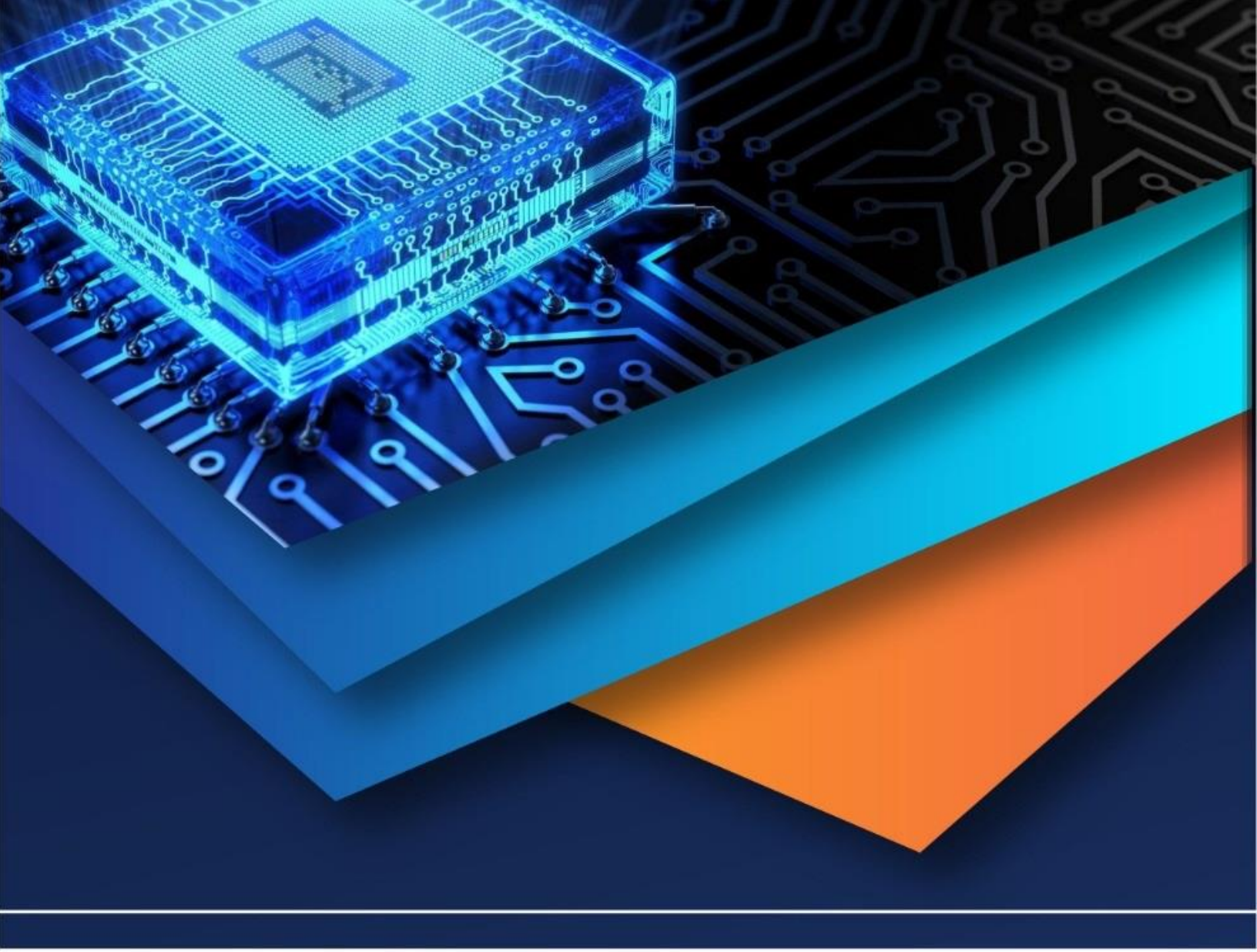
Fig. 6 Simulation Result

V. CONCLUSION

This paper has discussed the strong architecture for Forward Error Correction Encoder for DVB-S2 considering the fault models, intending to provide a good quality product, ease of testing. FEC encoder is used to control errors during data transmission over noisy or unreliable channels.

REFERENCES

[1] Enrico Casini Proceedings of the 20th AIAA Satellite Communication Systems Conference, Montreal, AIAA-paper 2002-1863, May 2002
[2] "Digital Video Broadcasting (DVB): Framing Structure, Channel Coding and Modulation for Digital Terrestrial Television," ETSI EN 300 744, V.1.5.1, European Telecommunications Standards Institute, 2004
[3] Rinaldo "DVB-S2 ACM modes for IP and MPEG unicast applications" international journal of satellite communication and networking, 2004
[4] https://www.google.co.in/search?client=opera&q=bch+coding&sourceid=opera&ie=UTF-8&oe=UTF-8
[5] https://www.google.co.in/search?client=opera&q=fec+encoder&sourceid=opera&ie=UTF-8&oe=UTF-8



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY