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Quadratic based Caches Mapping Technique

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Abstract: ***Cache mapping is a technique used by CPU for storing various copies of data from main memory to the cache memory to minimize the mean time to obtain memory. Distinct cache mapping techniques have various mapping results rely on the cache hit or cache miss ratio changes with respect to corresponding mapping. In this paper, the work is carried on evaluating the combinatorial cache memory through simulation programs and also to discover the best one among the mapping from the obtained evaluation results. Moreover, this work aims to serve the chip designer to find the outcome over a cache memory simulation program. This evaluation work will help us to evaluate different cache mapping methods and will also help us to analyze and find out the pros and cons of mapping scheme.***

Keywords: Cache memory, cache Hit, cache miss, read, write, direct mapping, fully associative mapping, write-through, write back.

I. INTRODUCTION

Cache Mapping is a technique of Central Processing Unit (CPU) that access the main memory fastest then simple access the memory. A cache memory is used to obtain the main memory information speedy then average time. A cache memory is used when a processor want to read a information to main memory then first it will check the information available in cache and not, if the information present in cache then it will read the information fast and it's called cache Hit and if the information is not available in cache memory then it's called cache Miss. Cache mapping used mainly three techniques: - Direct mapping, Associative mapping and set associative.

Direct mapping is a simple mapping technique, in which simply one Tag field, one Data field and one index field. Index field and Tag field contains the address of Data and value that store in main memory. Index field contains $\log_2$ (m) bits and Tag field contains $\log_2$ (n/m) bits and Data field contains m bits.

Index Field	Tag Field	Data Field

Associative mapping is also called as fully associative mapping. In fully associative mapping the main memory and cache memory are divided in to same size of blocks. Associative mapping is speeder than the direct mapping but it is also complex as compare to direct mapping.

Set associative mapping is the merging of direct and fully associative mapping. In this mapping technique the cache memory is split in to one index field and two Tag field and two Data field.

Index field	Tag field	Data field	Tag field	Data field

The execution of cache mapping is depends on cache hit or cache miss. A cache hit if the information available in cache memory and cache miss if the information not found in cache memory. Cache hit or miss we calculate the ratio of cache memory.

Hit Ratio =

$$\frac{\text{Total number of information is available in cache memory}}{\text{Total size of memory access}}$$

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II. CACHE MEMORY

It is faster than main memory.The time taken is less when compared to main memory.The programs which can be executed in a short period of time is stored in cache memory.Cache memory is expensive than RAM and it is very fast.CPU instructions are stored in cache which has a big memory size wheras RAM stores less frequently accessed data.Larger the cache size,the data transfer is faster and CPU performance is good.The performance of PC can be increased by cache memory.The data and information that are frequently requested are stored here so that they can be immediately available to CPU when it is needed.Cache memory is actually CPU memory, the micro processor can access quickly than that of RAM.When micro processor processes the data it first see the data present in the cache memory.

Improving Cache Performance:

We can improve cache performance by following:

1) Reduce the miss rate
2) Reduce the miss penalty
3) Reduce the time to hit in the cache.

III. PROBLEM

The Direct cache mapping technique is convenient to implement and easy to understood. But in this cache mapping technique cache miss tio is more and it is time consuming also. It's taken more time in run. Determine a cache line in a main memory block we use a mapping formula:-

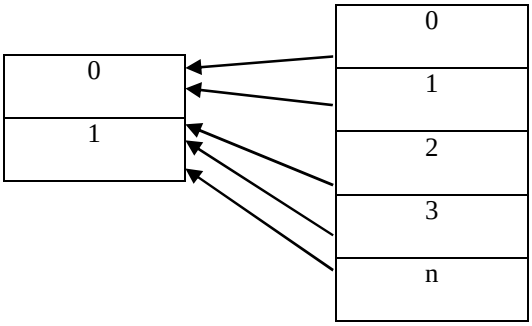
Cache line = (main memory line) MOD (no. of cache lines)

Calculate a cache memory size we took the formula: $\mathbf{2^n}$

Where n = main memory size

For example if main memory size is 16 then cache line are $2^4 = 4$. If we need to calculate the cache line for 6 then it's simply 6 MOD 4 = 2.

The problem in direct mapping is increase the cache miss ratio, that effect the CPU performance and it's taken higher time to execute.



In shown diagram direct mapping between cache memory and main memory.

IV. SOLUTION

In our project we use a Quadratic equation. The general format of Quadratic equation is –

$$\mathbf{a\,x^2 + b\,x + c}$$

Where a, b and c are any integer value.

In our project we did a, b and c value is unique prime number that must be different for each other, and x value will be change according to main memory size start with 0.

For mapping we use a formula –

$y = (a\,x^2 + b\,x + c)$ MOD (Main memory size)

The given formula we use for mapping the cache memory. If the result of y is unique for each memory block then a , b and c value is accepted other vise the merge of a, b and c is incorrect. In this project we use a, b and c value prime and we check it from 0 to 999.

For Replacement of the Page policy use any technique like First in first out (FIFO), Least Recent use (LRU) and Optimal Page Replacement Policy. Using these techniques we remove all unnecessary data or pages from cache memory, simply we use in our project is Optimal page replacement policy, this is we choose because in this page replacement policy minimum page fault.

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V. ALGORITHM

1) *Step 1*- Read the main memory size and check it it's in the form of 2^n, if it is not then read again.
2) *Step 2*- Read Quadratic coefficient a, b and c value.
3) *Step 3*- Check the value of a, b and c must be prime and different. If it is not then go to step 2
4) *Step 4*- Now compute the value of y using the formula. $y = (ax^2+bx+c)$ MOD (memory size)
5) *Step 5*- check the all y value that must be unique or not. If it is different the show a message – a,b and c values are accepted other vise show combination is not accepted.
6) *Step 6*- End the Program.

Below some example are given

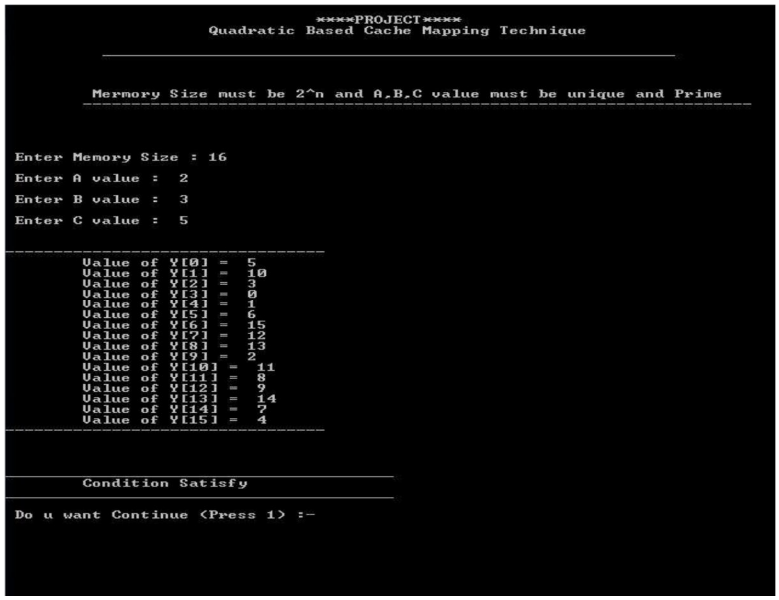
X	a	b	c	Y	Mod
0	5	17	2	2	2
1	5	17	2	24	0
2	5	17	2	56	0
3	5	17	2	98	2
4	5	17	2	150	6
5	5	17	2	212	4
6	5	17	2	284	4
7	5	17	2	366	6

X	a	b	c	Y	Mod
0	19	23	17	17	1
1	19	23	17	59	3
2	19	23	17	139	3
3	19	23	17	257	1
4	19	23	17	413	5
5	19	23	17	607	7
6	19	23	17	839	7
7	19	23	17	1109	5

The main aim for this is to discover the right prime number combination for cache memory.

VI. OUTPUT

A sample output is show bellow. In this first it will ask the memory size, then after its takes values for a, b and c and check that the value must be prime of different. Now it's calculate y value form the formula and check that are unique and different each other, if it is correct then show a message condition is satisfied otherwise show condition not satisfied.



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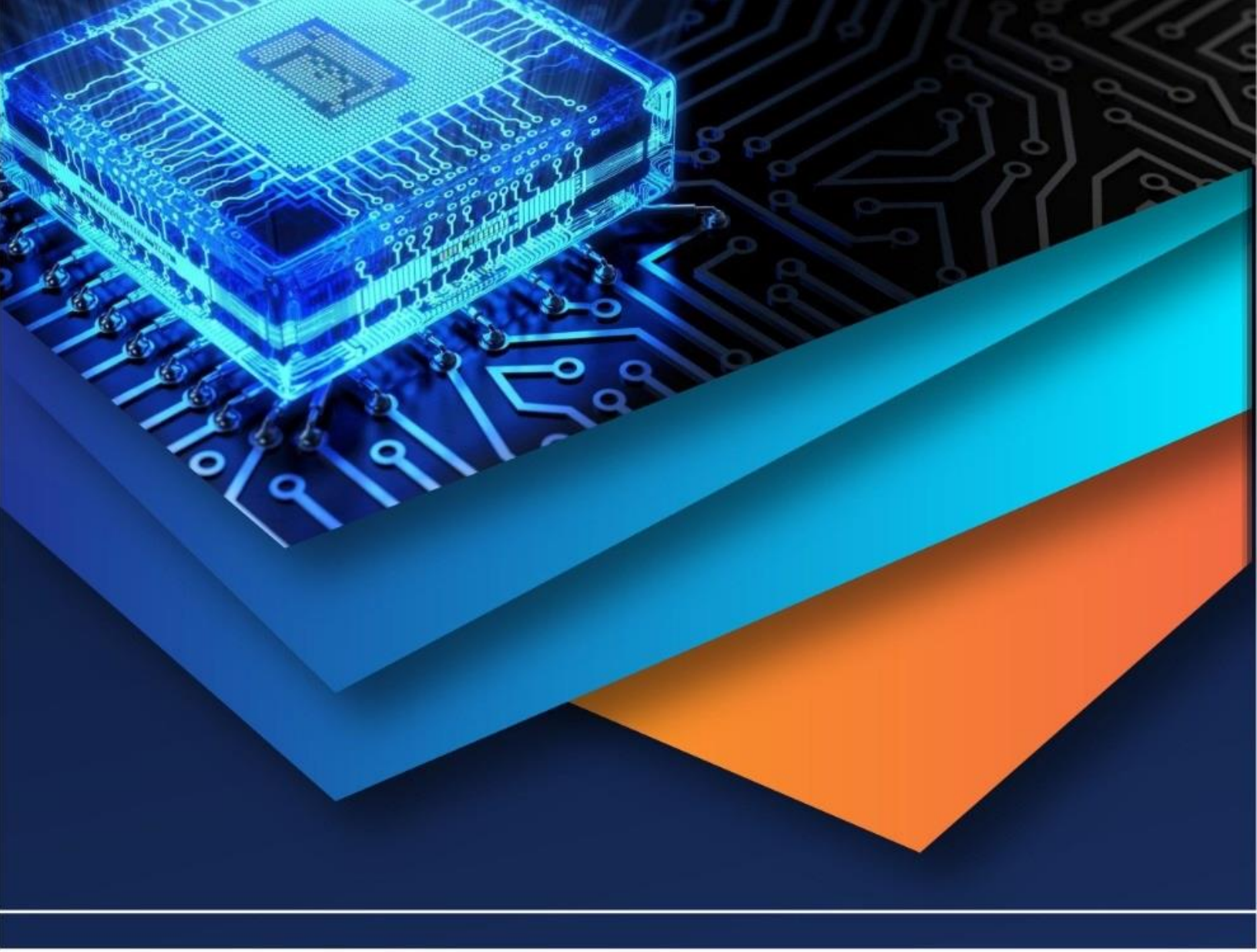
VII. CONCLUSION

The Quadratic based cache mapping is faster than direct mapping or associative mapping. It's easy to implement and easy to understand. In this technique generates unique values so that a better mapping technique is generated. Quadratic based mapping lower miss ratio and higher hit ratio that increase the performance of fetching the data from main memory to cache memory and cache memory to CPU. It decreases the miss ratio and reduces the time taken by processor to fetch the data from memory.

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