iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 3 **Issue:** V **Month of publication:** May 2015

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Sensitivity Analysis of High Speed Sense Amplifier

Jyoti sharma[1], Rajesh Parihar[2]
[1]M.Tech Scholar, [2]Asst. Professor, H.O.D., ECE, CBSGIs, Jhajjar,

Abstract- ***In this paper we have examined the sensitivity Of Current Mirror Sense amplifier at different values of Vdd and W/L ratio.We have verified the results of sensitivity at 180 nano meter technology. In this Paper we will see that when Vdd increases circuit ability to avoid the noise also increases and thus increases the efficiency of circuit. Simulation results shows that efficiency of Sense Amplifier increases with increasing supply voltage and decreases with decrease in W/L ratio.***
Keywords – Sense Amplifier, Sensitivity, efficiency, W/L Ratio.

I. INTRODUCTION

Sense Amplifier is important component of memory design. The choice and design of Sense Amplifier robustness of bit line sensing impacting read speed and power. Due to variety of Sense Amplifiers in semiconductor memories and the impact they have on final specs of memory, the sense amplifiers have become a separate class of circuit.[1]
Since amplifiers play a major role in the functionality Performance and reliability of memory circuits. It is required to read data from memory. Moreover, sense amplifiers are needed to amplify input bit line swing of about 100mv to full digital levels.
In SRAM memory circuits, bit line voltage sometimes reads data incorrectly i.e. read logic 0 instead of reading logic 1. This is due to the small output voltages of SRAM circuit. Sense amplifiers are used to amplify small signals on large capacitive bit lines which can be further used by digital logic. Sense amplifiers use a pair of matched transistors in a positive feedback. A differential input applied to these matched transistors is amplified and resulting logic signals are latched.
For fast and power efficient memory design, both time and signal swing on the bit lines should be minimized.
A differential amplifier with current mirror type of configuration is used to sense correctly. Less delay and power consumption in the circuit involves tradeoff between VDD, Ist Author offset voltage and delays. In particular, they perform the following functions
Amplification- In certain memory structure such as the IT DRAM, amplification is required for proper functionality since the typical circuit swing limited to 100 mill volts
Delay Reduction-The amplifiers compensate for restricted Fan out driving capability of the memory cell by accelerating The bitline transition or by detecting and amplifying small Transition on the bitline to large signal output
Power Reduction- Reducing the signal swing on bit line can eliminates a substantial part of power dissipation related to charging and discharging of bitlines.[2]

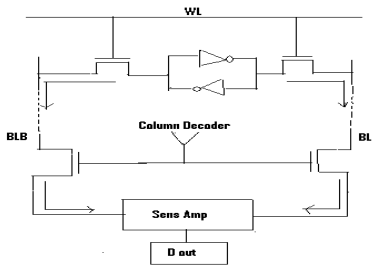


Fig 1. – Block diagram of Sense Amplifier with Memory Circuit[1]

General parameter characterization of a sense amplifier include

Gain- Vout/Vin
Sensitivity- minimum detectable signal
Offset Voltage
CMRR-Common mode rejection ratio
Nosise Marhin- Maximum value of noise of noise tolerated by device.

Simultaneous optimization of above parameter is a difficult task involving balancing the circuit complexity, la- out area ,reliability power speed and environmental tolerances. [1

II. DESIGN METHOLOGY

Essentially the component of sense amplifier NMOS differential pair upon which input are applied which gives higher trans conductance gm. A sense- enable NMOS transistor which basically supply bias current to the differential pair and different active load. Active load are current mirror, which provide higher output resistant with minimum area. The sense amplifier utilize varied load for differential pair, thus achieving diverse gain consequently, different noise margin.[main paper]

III. CURRENT MIRROR SENSE AMPLIFIER

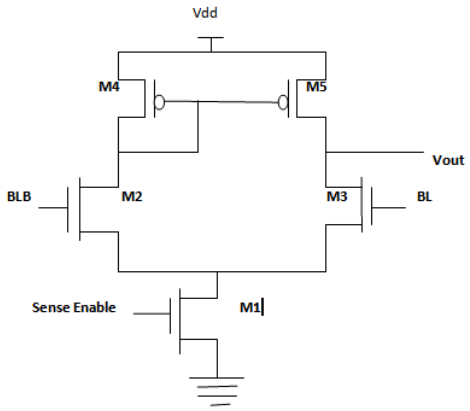


Fig. 2 – Current mirror sense amplifier[2]

The main reason of using this type of sense amplifier for better nose immunity and speed of read circuit.[9]**.** Current Mirror Sense Amplifier takes differential input and amplify them large signal output. The differential approach presents numerous advantage over single ended counter part – one of the most important being common mode rejection. That is such amplifier rejects the noise that is equally injected **at** both input. The signal common at both input suppressed at output of amplifier.[2] e drawback is current mirror sense amplifier that it consume more power than other type due to dc bias current.[ref-3]

IV. PROPOSED CIRCUIT

The current mirror sense amplifier eventually amplifies correct read data once the developed sensing margin overwhelms the input offset voltage of sense amplifier. As a result it can avoid sensing failure much better. Nevertheless such current mirror sense amplifier consume more power than other type due to d.c. biasing current [9] so it compensated by the gain. Since gain is proportional to the transconductance. The transconductance of the device can increased by widening of devices or by increased by bias current.
Although we have some area penalty it compensated by the gain.

Volume 3 Issue V, May 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

V. SIMULATION OF SENSE AMPLIFIER

Sense amplifier enable when minimum detectable signal 50 mV. BL maintain at 1.80 V and BLB maintain at 1.75 V. Speed of sense amplifier are increases when corresponding Vdd are increases but corresponding power dissipation are also increases. When we increases threshold voltage of input transistors corresponding delay are also increases. The main reason of power consumption during high Vdd is time window of transition region are large so there device found more time to short between Vdd and ground. It also computed from the formula $P= CV^2F$.Offset voltage of sense amplifiers arise from unavoidable mismatch in the differential mismatch at differential stage caused by mismatches in transistor pair , drain current drain resistance .In the case of sensitivity when we increases the threshold, corresponding sensitivity increase because it take more time to sense the signal. In the case of CMRR for any amplifier it value should be high .Same applicable or sense amplifier also. Speed of sense amplifier increases when CMRR increases the reason behind that better CMRR helps to suppressed common mode signal.

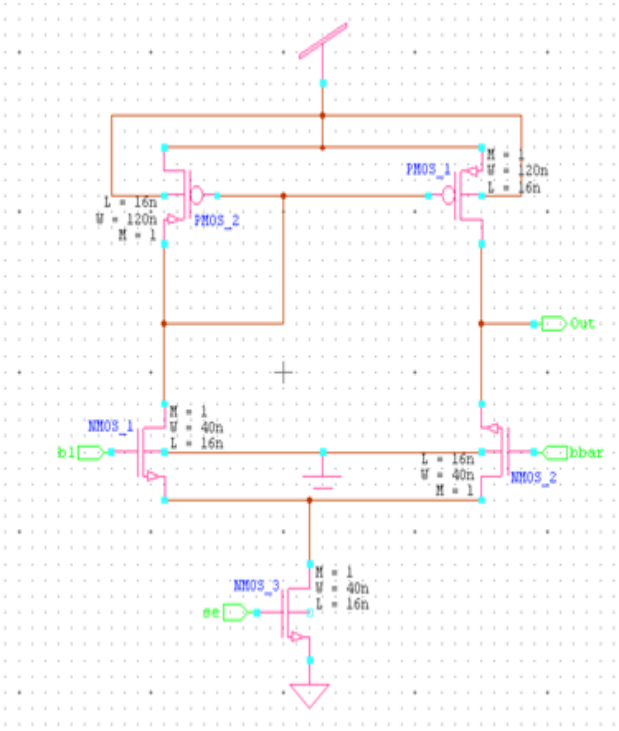


Fig.3 – Schematic of Current Mirror sense amplifier

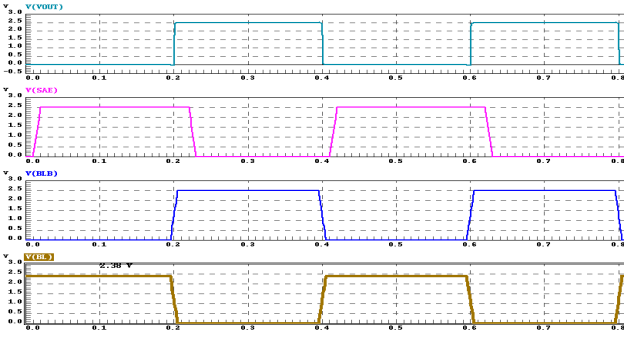


Fig.4 – Simulated Waveform of Current Mirror sense amplifier

Volume 3 Issue V, May 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

VI. RESULT AND ANALYSIS

Table 1.1 V_{DD} versus Sensitivity of CLSA

S.No.	V_{DD} (V)	Sensitivity (V)
1.	5	0.41V
2.	4	0.30V
3.	3	0.19V
4.	2	0.05V

Its clear from the table 1.1 when Vdd increases sensitivity also increases.

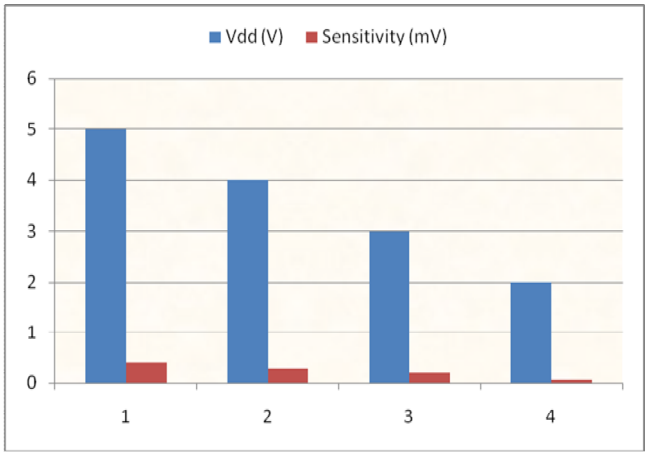


Table 1.2 W/L Ratio versus Sensitivity of CLSA

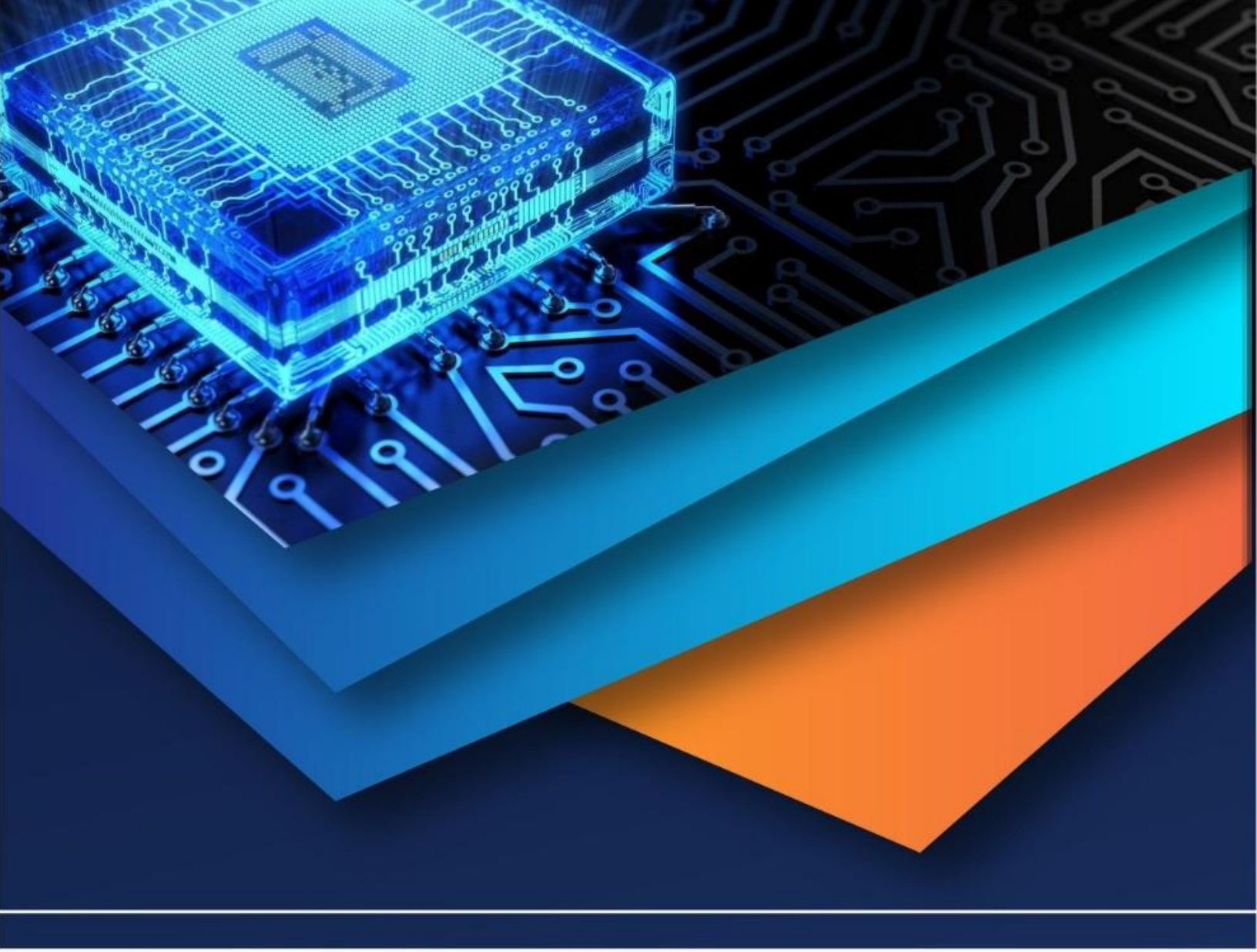
W/L Ratio (µW)	Sensitivity (V)
900/180	0.7
720/180	0.54
540/180	0.48
360/180	0.3
180/180	0.13

VII. CONCLUSION

From the above graphs and tables we conclude that the sensitivity of sense amplifier increases with increase in supply voltage and decreases with decrease in W/L ratio. Thus from these results we conclude that sense amplifier can avoid noise and provides efficient output at higher value of supply voltage.

REFERENCES

[1] Andrei Pavlov & Manoj Sachdev. "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies".spriger Publication. 2004
[2] Janm Rabaey, Anantha Chandakasan, Borivoje Nikolic."Digital Integrated Circuits", Second Edition, PHI Publication 2008.
[3] Behzad Razavi "Design of Analog CMOS Integrated Circuit " TATA Mc Graw Hill Publication 2008.
[4] Tuli Dake and Erhan Ozaleveli " A Precision High- Voltage Current Sensing Circuit' IEEE Transaction on CIRCUIT and SYSTEM Vol-55 pp: 1197-1202 ; JUNE 2008.
[5] Sherwin Paul R. Almazan , Zarsuela , Anastacia P. Ballesil, Louis P. Alarcon " A Study on Effect of Varying Voltage Supply on the Performance of voltage Sense Amplifier for 1 T DRAM Memories. IEEE pp: 108-112 , ICSE 2008.
[6] Antonino Conte, Gianbattista Lo Giudice P alumbo, Alfredo " A High Performance Very Low Voltage current sense amplifier for Nonvolatile Memories" IEEE JOURNAL of SOLID STATE CIRCUIT. Vol -42 No 2 pp: 507-514, Feb. 2005.
[7] Tang Young , Feng Quan Yuan Piotor Nasalski " A New Flash Memory Sense Amplifier In 0.18µm CMOS Technology " IEEE SYMPOSIUM of QUALITY ELECTRONIC DESIGN pp : 138 –141 2005.
[8] Joseph F.Ryan and Benton H .Calhoun "Minimizing Offset for Latching Voltage –Mode Sense Amplifier for Sub-threshold Operation " 9 th International Symposium on Quality Electronic Design pp: 127-132, 2008.
[9] Sreerama Reddy G M, P. Chandrasekhara Reddy "Design and Implementation of 8k-bit low Power SRAM in 180-nm Technology" Proceedings of the International MultiConference of Engineers and Computer Scientists 2009 Vol II IMECS 2009, March 18-20, 2009, Hong Kong.
[10] Ya –Chun Lai and Shi-Yu Huang "Resilient and Power Efficient Automatic –Power Down Sense Amplifier for SRAM Design" IEEE Transactions on Circuits and Systems, Vol 55, No.10, October 2008.
[11] Anantha P. Chndrakasan and Robert W.Brodersen,"Minimizing Power Consumption in Digital CMOS Circuit" IEEE Vol 83, No 4, pp: 498-521, April 1995
[12] Bao Nguyen and W.David Smith "Nulling Input Offset Voltage of Operational Amplifiers" Mixed signal Products, Texas Instruments, pp:1-14, August 2000.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY