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Design and Analysis of Low Power High Speed Current Latch Sense Amplifier

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Abstract- This paper is about the comparison of the conventional CLSA and a current latch sense amplifier with body bias controlled CLSA. In late, used for speed up of the precharging time of Sense Amplifier. The CLSA is capable of high-speed pre-charging with little increase in transistors counts. We will also verify the various result like Power consumption, Offset Voltage and noise margin at 180 nano meter technology. Here in this Paper we will see that when Vdd increases circuit the ability to avoid the noise increases but power consumption are increases. Simulation result shows that speed of Sense Amplifier are increased by 11% at same time the power dissipation reduced by 80%.
Keywords – Sense Amplifier (SA), CLSA, BB-CLSA, Offset voltage, Sensitivity.

I. INTRODUCTION

Static random access memory (SRAM) that occupies a large area in a digital LSI system is an indispensable building block for digital signal processing. Data stored in an SRAM cell are read by a sense amplifier circuit. The sense amplifier amplifies the voltage or current difference between two bit lines, BL and BLB, connected to the SRAM cells. So the sense amplifier (SA) is the most important peripheral circuits in memory devices. The choice and design of Sense Amplifier robustness of bit line sensing impacting read speed and power [1]. Due to variety of Sense Amplifiers in semiconductor memories and the impact they have on final specs of memory, the sense amplifiers have become a separate class of circuit. Sub threshold operation of MOSFETs has been attracting much attention as an alternative to conventional low-power techniques [1].

The LSIs that operate in the sub threshold region of MOSFETs can achieve ultra-low power dissipation compared to conventional circuit design. Sub threshold operation, however, degrades the speed of digital circuits due to the extremely low drive-current of less than microampere. Sub threshold logic also provides extremely low power consumption since the power supplies are kept below the threshold voltage and the small sub-threshold current of MOS transistors is used as drive current. But in most of the implementations using sub threshold MOS circuits, body effect i.e. dependence of sub-threshold current on potential difference between body or substrate and source terminal (V_{SB}) is either neglected or it has not been taken into account using simplified equation. In deep submicron technology, body effect cannot be neglected. Body effect degrades the linearity of the circuit due to nonlinear behaviour of transconductance of MOS transistor with respect to input. So amplifiers play a major role in the functionality Performance and reliability of memory circuits. In a sense amplifier, precharging of the sense amplifier is required for correct sensing and amplifying. The pre-charge time generally determines the speed of the sense amplifiers.

Therefore, a sense amplifier circuit with a high-speed pre-charge is strongly required. In particular, the sense amplifier performs the following functions namely.

A. Amplification

In certain memory structure such as the DRAM, amplification is required for proper functionality since the typical circuit swing limited to 100 millivolts

B. Delay Reduction

The amplifiers compensate for restricted Fan out driving capability of the memory cell by accelerating The bitline transition or by detecting and amplifying small Transition on the bitline to large signal output

C. Power Reduction

Reducing the signal swing on bit line can eliminates a substantial part of power dissipation related to charging and discharging of bit

lines [6, 7].

General parameter characterizations of a sense amplifier are

Gain- Vout/Vin

Sensitivity- Minimum detectable Difference signal.

Offset Voltage- Minimum difference between bit lines voltage at which sense amplifier gives altered outputs.

CMRR-Common mode rejection ratio

Simultaneous optimization of above parameter is a difficult task involving balancing the circuit complexity, lay out area, reliability power speed and environmental tolerances.

II. CONV ENTIONAL SENSE AMPLIFIER

Figure 1 shows a schematic of a conventional CLSA [4], [5]. This CLSA consists of nine transistors. Transistors MP1, MP2, MN1, and MN2 form a cross-coupled complementary structure, and two bit lines, BL and BLB, are connected to the gate nodes of transistors MN3 and MN4. Unlike the Voltage sense Amplifier, the CLSA has its outputs isolated from the inputs.

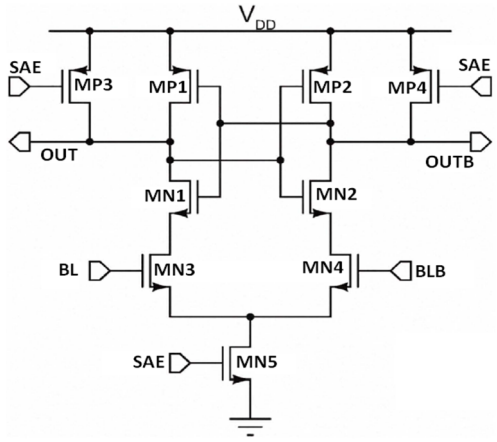

Fig 1: Schematic of conventional CLSA.

When a pre-charge control signal (SAE) is low, pre-charge transistors MP3 and MP4 turn On. Output nodes V_{OUT} and V_{OUTB} are then charged to the supply voltage (V_{DD}) through MP3 and MP4. When SAE is high, pre-charge transistors MP3 and MP4 turn off and transistor MN5 in on state. When the bit lines are connected to gate of transistors MN3 and MN4 by column selector circuit. Due to this an activated SRAM cell induces the small voltage difference between BL and BLB depending on the data stored in the cell, the cross-coupled complementary structure of the sense amplifier amplifies the voltage difference to a full swing voltage when control signal SAE kept high. Sensing must be performed after output nodes V_{OUT} and V_{OUTB} are pre-charged. So, the time for pre-charge determines the speed of the sense amplifiers. Therefore, a sense amplifier circuit capable of high-speed pre-charging is required.

III. BODY BIAS TECHNIQUE

One of the most promising ways to attain both high speed and low stand-by power consumption at low supply voltage is to modulate the threshold voltage of MOS (V_T) transistor electrically by applying source-to-body voltage (V_{SB}) at body terminal. A MOS transistor can be operated at a lower threshold voltage or higher threshold voltage by using body relation given by following equation biasing techniques. In this V_T is modulated by V_{SB}.

$$V_T = V_{TO} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

Where V_{TO} is the threshold voltage at V_{SB}= 0V and depends on the manufacturing process. V_T is threshold voltage other than 0 of V_{SB}, γ is the body effect coefficient, Φ_F is the surface potential at threshold and finally V_{SB} is the source to body voltage of MOS transistor.

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IV. CLSA WITH BODY BIAS TECHNIQUE

To achieve high-speed pre-charging of a sense amplifier, we developed a current latch sense amplifier with using a body bias control technique with a conventional CLSA. Because the precharging of the conventional CLSA shown in Fig. 1 is done with transistors MP3 and MP4, it can be accelerated by increasing the drive ability of transistors MP3 and MP4 with a forward body bias control. Therefore, we compare the results of conventional CLSA and body biased CLSA, a new circuit configuration with using extra two inverters for controlling of body bias of precharge transistors. The details of the circuit are discussed in implementation section.

V. IMPLEMENTATION AND RESULT

Figure 2 shows a schematic of our CLSA with body bias control. Two CMOS inverters consisting of four transistors (MP5, MP6, MN6, and MN7) are added to the conventional CLSA (Fig. 1). The source node of transistors MN6 and MN7
connected to the output and output node of the inverters are connected to body terminal of the pre-charge transistors. The SAEB, which is an inverted signal of SAE, is applied to the input of the inverters. When the SA is in sensing mode, SAE and SAEB are high and low, respectively.

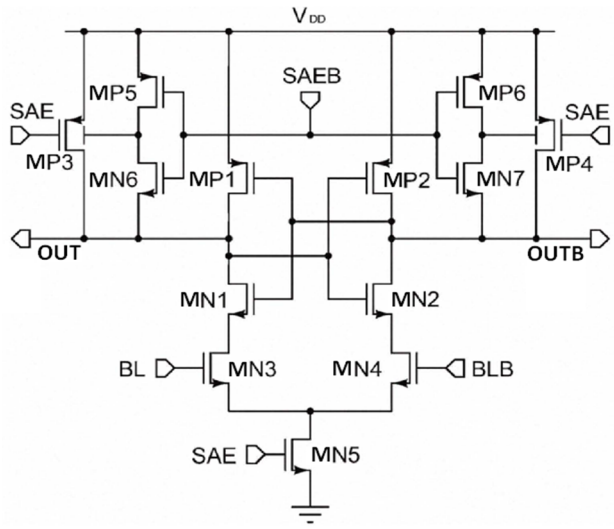

Fig.2. Schematic of body bias controlled CLSA.

At this time, both the output voltages of the inverters become high. Because the body nodes are kept at VDD, the CMOS inverters do not affect pre-charge transistors MP3 and MP4. On the other hand, when the CLSA is in pre-charge mode, SAE and SAEB are low and high, respectively. At this time, both the output voltages of the inverters connected to output of sense amplifier. Therefore, the voltage of one of the body nodes decreases to 0 V so a forward body bias voltage is applied. Then, the threshold voltage of the forward body biased pre-charge transistor decreases and the drivability of the pre-charge transistor increases. As the output node voltage increases, the gate-source voltage of MN6 or MN7 decreases. Thus, the body node is disconnected from the output sense amplifier and the forward body bias control keeps on being applied to the pre-charge transistor. Therefore, the pre-charging time reduced significantly.

The main reason of using this type of sense amplifier is to improve the nose immunity and speed of read circuit.[8]. Current latch Sense Amplifier takes differential input voltage and amplify them large signal output. The differential approach presents numerous advantage over single ended counter part – one of the most important being common mode rejection. That is such amplifier rejects the noise that is equally injected **at** both input. The signal common at both input suppressed at output of amplifier.

The performance of the sense amplifier was evaluated using T-SPICE with 180 nm technology standard CMOS parameters. To simulate a condition where a SRAM cell is connected to one column, 150 fF capacitances were connected to the bit lines. The size W/L ratio of transistors is kept in following manner MN1, MN2, MN6, MN7 all equal to540/180; MN3, MN4 are equal to720/180 ; MP1,MP2 are equal to 360/180,MP5 MP6 are equal to 1620/180; MP3,MP4 are equal to 900/180. MN5 is kept at 900/180 nm/nm A. Simulated circuit, Waveforms and Power dissipation We conducted transient analysis to evaluate the pre-charge performance and

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the power dissipation of the sense amplifiers.

In the simulations, the bit lines were first discharged with a SRAM cell and the sense amplifiers amplified the voltage difference. Pre-charging was then evaluated. Sense amplifier enable when minimum detectable signal 50 mV. Sense amplifier' Speed are increased when corresponding Vdd are increases but corresponding power dissipation are also increases.

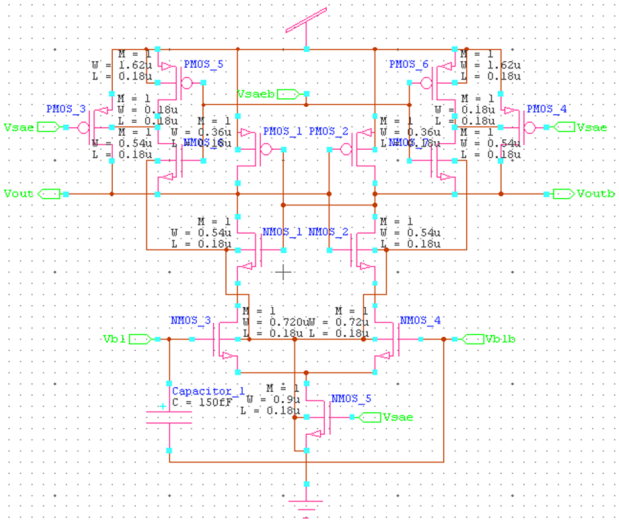

Fig.3. Implementation of body bias controlled CLSA

Pre-charging was then evaluated. Sense amplifier enable when minimum detectable signal 50 mV. Sense amplifier' Speed are increased when corresponding Vdd are increases but corresponding power dissipation are also increases. When we increases threshold voltage of input transistors corresponding delay are also increases. The main reason of power consumption during high Vdd is time window of transition region are large so there device found more time to short between Vdd and ground.

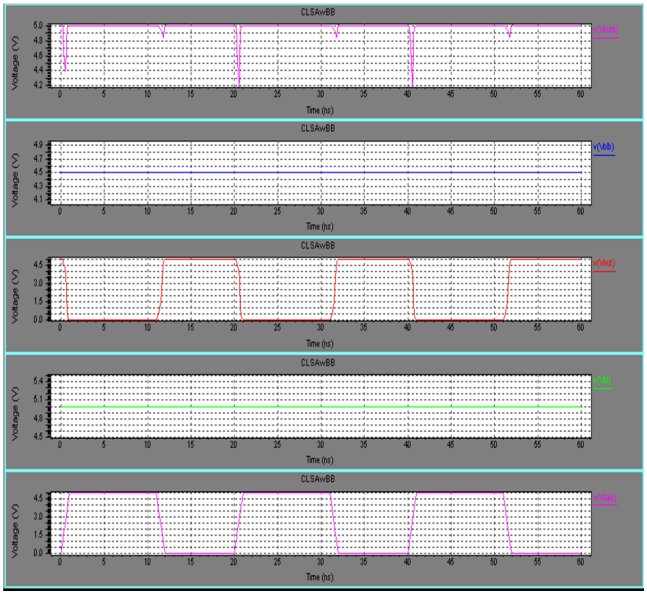

Fig.4: Simulated Waveform of sense amplifier

It also computed from the formula P= CV^2F.Offset voltage of sense amplifiers arise from unavoidable mismatch in the differential mismatch at differential stage caused by mismatches in transistor pair , drain current drain resistance .In the case of sensitivity when we increases the threshold, corresponding sensitivity increase because it take more time to sense the signal. In the case of CMRR for any amplifier it value should be high .Same applicable or sense amplifier also. Speed of sense amplifier increases when CMRR

increases the reason behind that better CMRR helps to suppressed common mode signal.

VI. RESULT AND ANALYSIS

Analysis and comparison of various parameters of CLSA & BB-CLSA is shown in this section

Table 1: Delay and Power dissipation with varying supply voltage

VDD (V)	CLSA		Body Biased CLSA	
	Delay (pS)	Power dissipation (µW)	Delay (pS)	Power dissipation (µW)
5	199.43	227.585	179	120.505
4	202.48	232.025	211.13	74.045
3	219.98	16.635	221.98	28.13
2	297.84	24.225	241.04	12.695
1	480.43	3.54	467.59	5.25

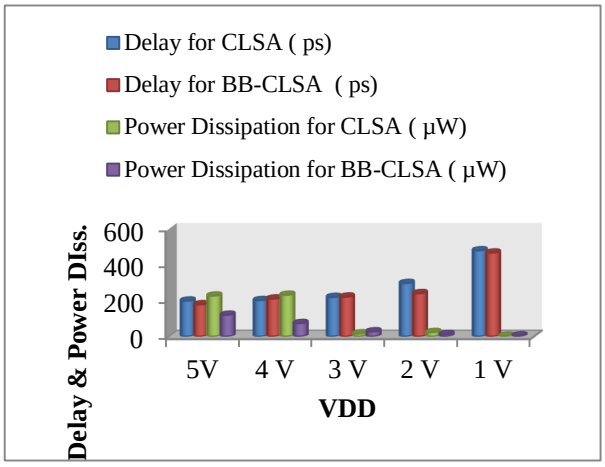

Fig 5: Graph b/w Delay and power with varying supply voltage

VII. CONCLUSION

We Compare the results of CLSA and body bias controlled -CLSA sense amplifier with using a technique called body bias controlled technique for improving high-speed pre-charging. The pre- harge time decreased by 11% and power dissipation decreased by only 80% compared to the conventional CLSA.

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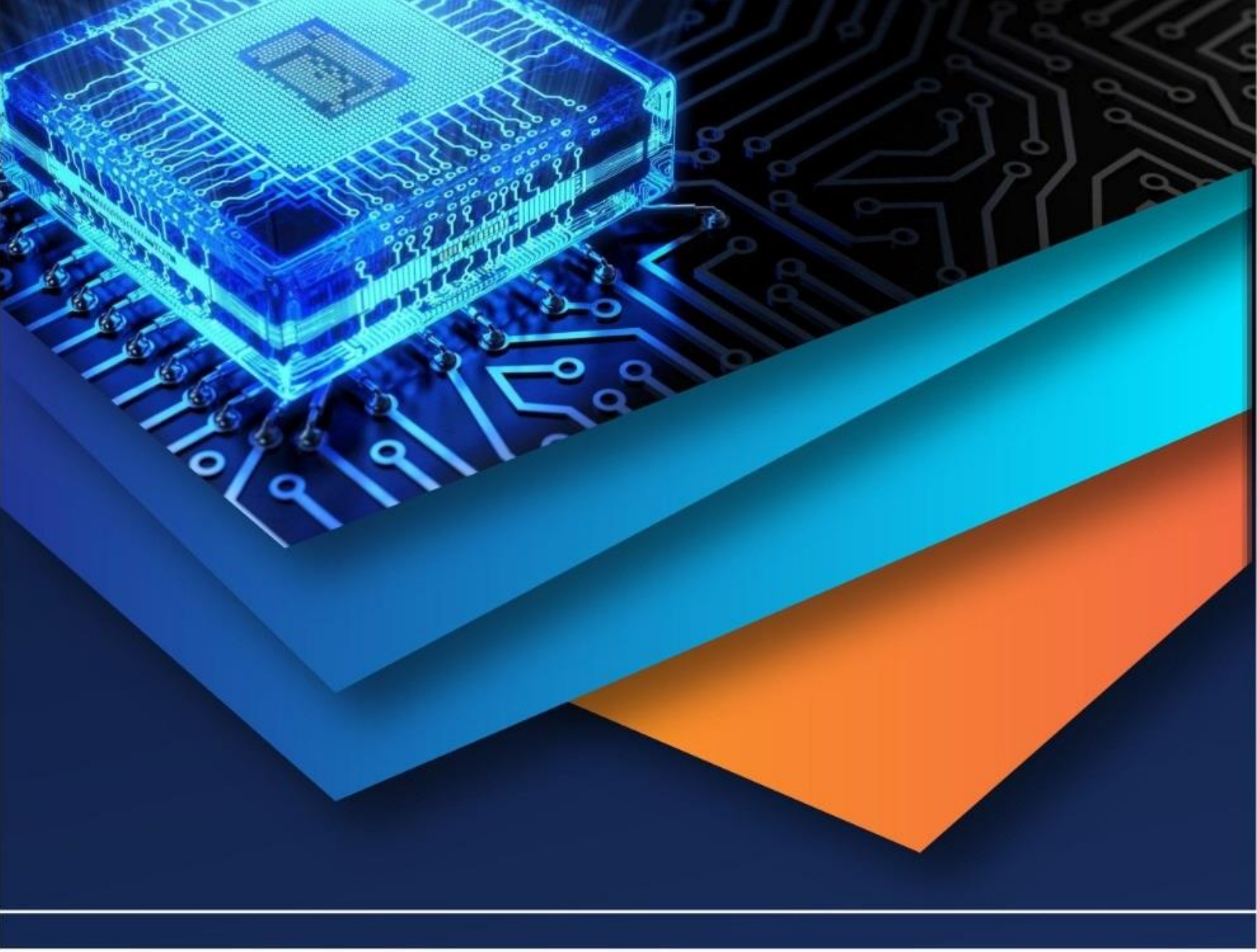

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