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An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator

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I. INTRODUCTION

Modern consumer electronics make extensive use of Digital Signal Processing (DSP) providing custom accelerators for the domains of multimedia, communications etc. Typical DSP applications carry out a large number of arithmetic operations as their implementation is based on computationally intensive kernels, such as Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), Finite Impulse Response (FIR) filters and signals' convolution. As expected, the performance1 of DSP systems is inherently affected by decisions on their design regarding the allocation and the architecture of arithmetic units.

II. SCOPE OF THE PROJECT

Complex arithmetic operations are widely used in Digital Signal Processing (DSP) applications. In this work, we focus on optimizing the design of the fused Add-Multiply (FAM) operator for increasing performance. We investigate techniques to implement the direct recoding of the sum of two numbers in its Modified Booth (MB) form. We introduce a structured and efficient recoding technique and explore three different schemes by incorporating them in FAM designs.

III. LITERATURE SURVEY

Title: Design Issues and Implementations for Floating-Point Divide–Add Fused
Author:Alexandru Amaricai, Mircea Vladutiu, and Oana Boncalo,
This brief presents a dedicated unit for the combined operation of floating-point (FP) division followed by addition/subtraction—the divide–add fused (DAF). The goal of this unit is to increase the performance and the accuracy of applications where this combined operation is frequent, such as the interval Newton's method or the polynomial approximation. The proposed DAF unit presents a similar architecture to the FP multiply-accumulate units. The main difference is represented by the divider, which is implemented using digit-recurrence algorithms.
An important design tradeoff regarding DAF is represented by the number of required quotient bits. We present the impact of the adopted number of quotient bits on accuracy, cost, and performance. Consequently, two implementations are proposed: one pro-accuracy and one pro-performance. We show that the proposed implementations have better accuracy with respect to the solution based on two distinct units: an FP divider and an FP adder. The implementation suitable for lower latency presents the best cost-performance tradeoff.

Title: FFT Implementation with Fused Floating-Point Operations
Author:Earl E. Swartzlander Jr., and Hani H.M. Saleh.
This paper describes two fused floating-point operations and applies them to the implementation of fast Fourier transform (FFT) processors. The fused operations are a two-term dot product and an add-subtract unit. The FFT processors use "butterfly" operations that consist of multiplications, additions, and subtractions of complex valued data. Both radix-2 and radix-4 butterflies are implemented efficiently with the two fused floating-point operations. When placed
and routed using a high performance standard cell technology, the fused FFT butterflies are about 15 percent faster and 30 percent smaller than a conventional implementation. Also the numerical results of the fused implementations are slightly more accurate, since they use fewer rounding operations.

Title: Estimation of Signal Transition Activity in FIR Filters Implemented by a MAC Architecture

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Author: S. Nikolaidis, E. Karaolis, and E. D. Kyriakis-Bitzaros

A novel method for the accurate calculation of the transition activity at the nodes of a multiplier-accumulator (MAC) architecture implementing finite impulse response filters is proposed in this paper. The method is developed for input signals, which can be described by a stationary Gaussian process. The transition activity per bit of a signal word is modeled according to the dual-bit-type (DBT) model and it is described as a function of the signal statistics. An efficient analytical method has been developed for the determination of the signal statistics at each node of the MAC architecture. It is based on the mathematical formulation of the multiplexing in time of signal sequences with known statistics. The effect of the multiplexing mechanism on the breakpoints of the DBT model, which influences significantly the accuracy of the method, is also determined. Several experiments both with synthetic and real data have been conducted. The numerical results produced by the proposed models are in very good agreement with the measured values of the transition activity.

Title: A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm

Author: Young-Ho Seo, and Dong-Wook Kim.

In this paper, we proposed a new architecture of multiplier-and-accumulator (MAC) for high-speed arithmetic. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was elevated. The proposed CSA tree uses 1's-complement-based radix-2 modified Booth's algorithm (MBA) and has the modified array for the sign extension in order to increase the bit density of the operands. The CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to decrease the number of the input bits of the final adder. Also, the proposed MAC accumulates the intermediate results in the type of sum and carry bits instead of the output of the final adder, which made it possible to optimize the pipeline scheme to improve the performance. The proposed architecture was synthesized with 250, 180 and 130 m, and 90 nm standard CMOS library. Based on the theoretical and experimental estimation, we analyzed the results such as the amount of hardware resources, delay, and pipelining scheme. We used Sakurai's alpha power law for the delay modeling. The proposed MAC showed the superior properties to the standard design in many ways and performance twice as much as the previous research in the similar clock frequency. We expect that the proposed MAC can be adapted to various fields requiring high performance such as the signal processing areas.

A. MODULES Description

1) *S-MB1 recoding scheme for even and odd number of bits: S-MB1 Recoding Scheme:* The first scheme of the proposed recoding technique is referred as *S-MB*1 and is illustrated for both even bit-width of input numbers. As can be seen in the sum of A and B is given by the next relation:

$$Y = A + B = \mathbf{y}_k \cdot 2^{2k} + \sum_{j=0}^{k-1} \mathbf{y}_j^{MB} \cdot 2^{2j}$$

$$\text{where} \quad \mathbf{y}_j^{MB} = -2s_{2j+1} + s_{2j} + c_{2j}.$$

When we form the most significant digit (MSD) of the *S-MB*1 recoding scheme, we distinguish two cases: In the first case, the bit-width of A and B is even, while in the second case, both A and B comprise of odd number of bits. In the first case, the MSD $y_{k,even}$ is a signed digit and is given by the next algebraic equation:

$$y_{k,even=-a2k-1+c2k}$$

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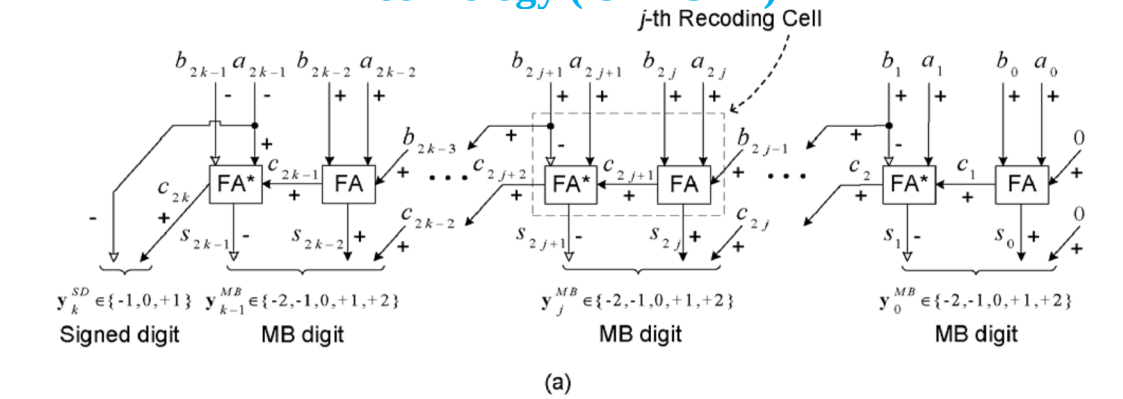

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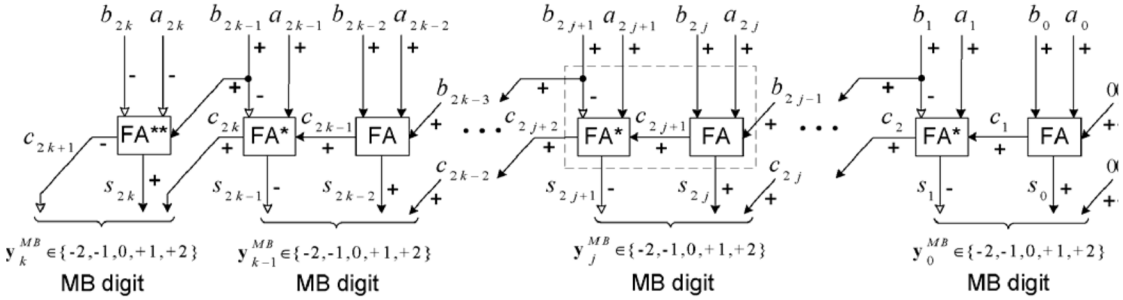

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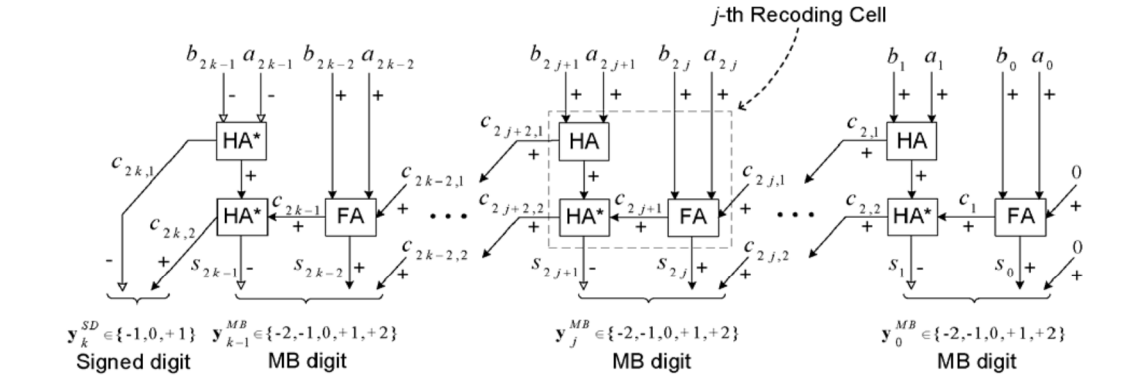
2) S-MB2 recoding scheme for even and odd number of bits



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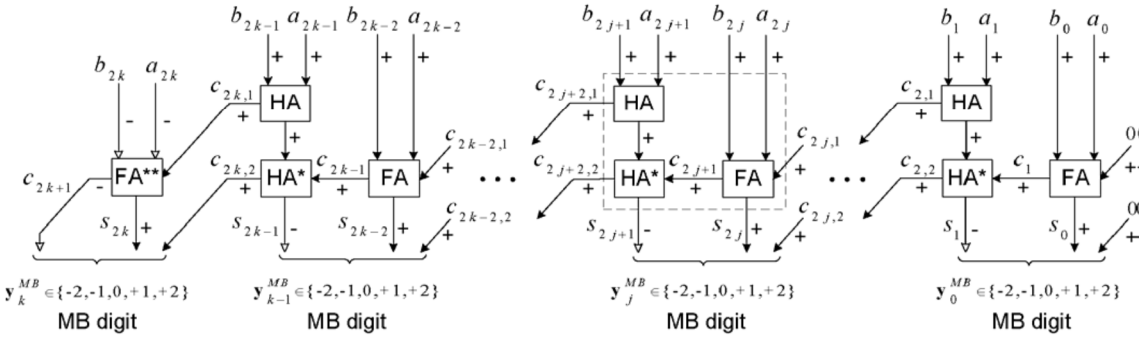

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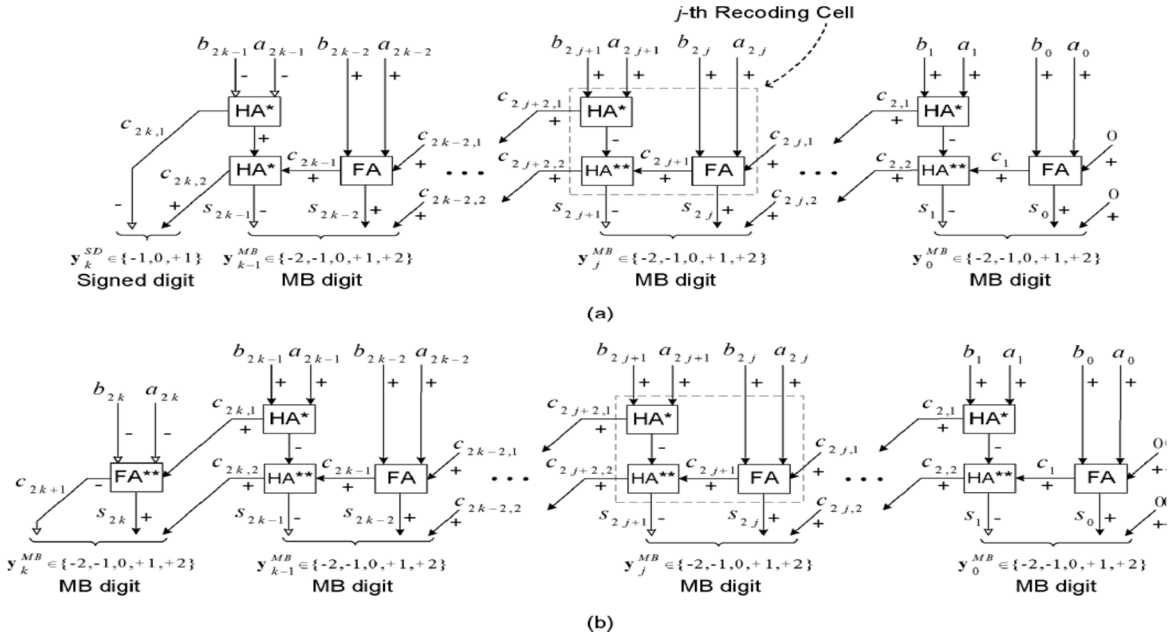
3) S-MB3 recoding scheme for even and odd number of bits



B. Proposed System Algorithm

In *S-MB* recoding technique, we recode the sum of two consecutive bits of the input A with two consecutive bits of the input B into one MB digit . As we observe from (2), three bits are included in forming a MB digit $y_{j,MB}$. The most significant of them is negatively weighted while the two least significant of them have positive weight. Consequently, in order to transform the two aforementioned pairs of bits in MB form we need to use signed-bit arithmetic. For this purpose, we develop a set of bit-level signed Half Adders (HA) and Full Adders (FA) considering their inputs and outputs to be signed.

C. Software Requirement

1) *MODELSIM 6.4C:* ModelSim is a simulation tool for hardware design which provides behavioral simulation of a number of languages, i.e., Verilog, VHDL, and System C. Verilog HDL is an industry standard language used to create analog, digital, and mixed-signal circuits. HDL's are languages which are used to describe the functionality of a piece of hardware as opposed to the execution of sequential instructions like that in a regular software application.
2) *XILINX 9.1/13.2:* Xilinx Tools is a synthesize tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA). Digital designs can be entered in various ways using the above CAD tools: using a schematic entry tool, using a hardware description language (HDL) – Verilog or VHDL or a combination of both.

D. Hardware requirement

1) *FPGA: Field Programmable Gate Arrays (FPGAs)* are programmable semiconductor devices that are based around a matrix of Configurable Logic Blocks (CLBs) connected through programmable interconnects. As opposed to Application Specific Integrated Circuits (ASICs), where the device is custom built for the particular design, FPGAs can be programmed to the desired application or functionality requirements and One-Time Programmable (OTP) FPGAs are available. In our project we are using Spartan 3 FPGA kit.
2) *SPARTAN 3:* The Spartan 3 trainer xc3s400 pq208 is useful to realize and verify digital designs. User can construct Verilog/VHDL code and verify the results by implementing physically into the target device (FPGA). With the help of this kit user can simulate/observe various input and output conditions to verify the implemented design.
3) *SPARTAN 3 AN:* The Spartan 3AN trainer xc3s50AN tq144 is useful to realize and verify digital designs. User can construct Verilog/VHDL code and verify the results by implementing physically into the target device (FPGA). With the help of this kit user can simulate/observe various input and output conditions to verify the implemented design

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E. Future Enhancement

We will modify the proposed system by increasing the input bit size of A and B and will get a multiplier output with efficient area and low delay.

F. Advantages

1) High-Throughput.
2) Less area &delay.
3) Reduces the system complexity**.**

G. Application

1) Digital signal processing (DSP).
2) Finite impulse response (FIR) filter.

IV. CONCLUSION

This paper focuses on optimizing the design of the Fused-Add Multiply (FAM) operator. We propose a structured technique for the direct recoding of the sum of two numbers to its MB form. We explore three alternative designs of the proposed *S-MB* recoder and compare them to the existing . The proposed recoding schemes, when they are incorporated in FAM designs, yield considerable performance improvements in comparison with the most efficient recoding schemes found in literature.

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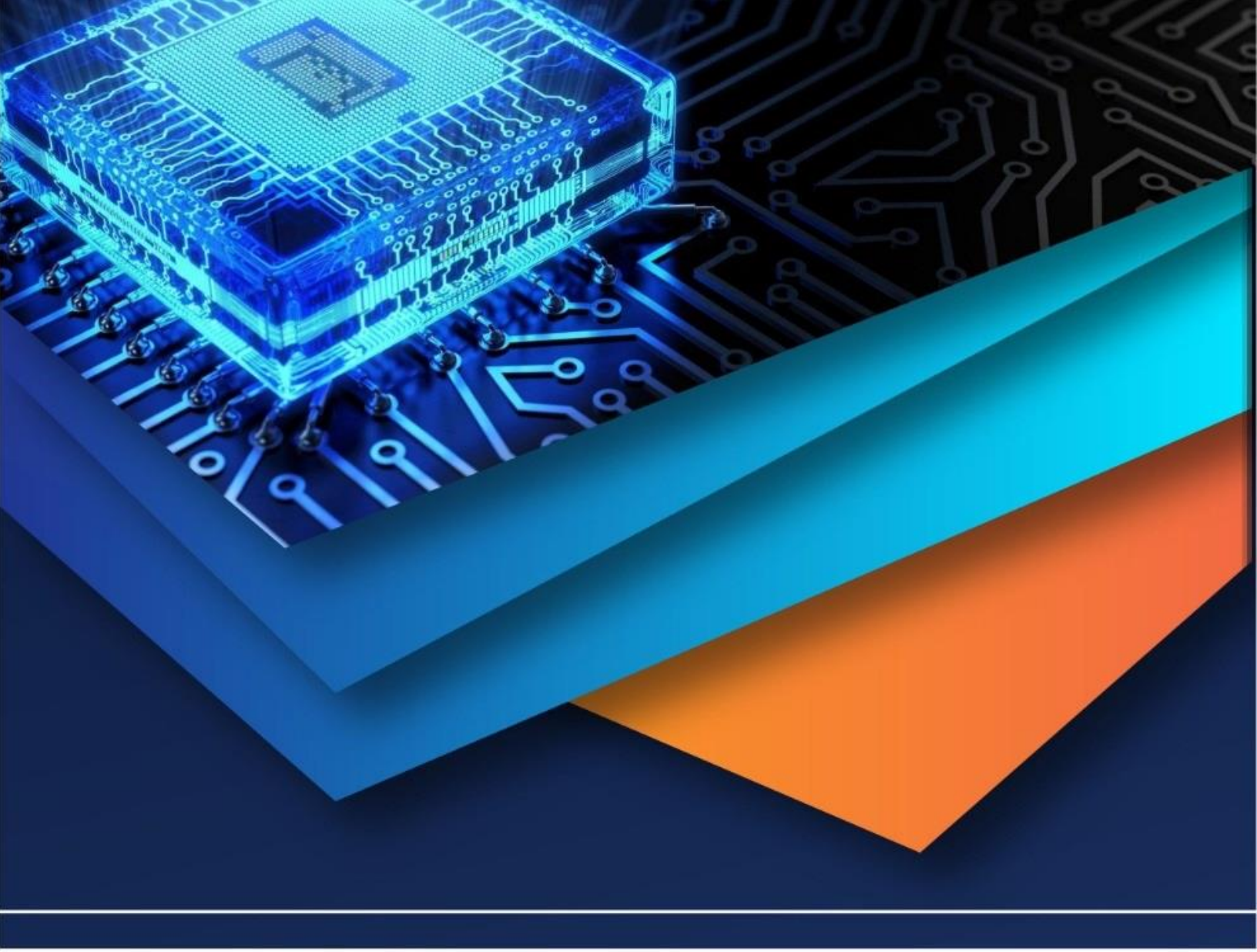

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