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Estimation of Mathematical Function by Stochastic Logic

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Abstract: ***Recent application demand high speed and robustness with small area and low power consumptions. Much pupation in nanometer scale technology in VLSI dimension of transistors goes on reducing. On the other hand increasing number of transistors leads to leakage current so Circuit becomes unreliable. Additionally, if transistors are replacing by other devices it does not yield satisfied result. Owning to these complications an alternative method for computing technique called stochastic logic. This paper described a stochastic implementation for various mathematical functions which analyses the area, power consumption, delay, efficiency. Logic implementations overcome the disadvantages of conventional methods.***
Keywords: Stochastic logic, mathematical function, AlteraDE2 board, VHDL.

I. INTRODUCTION

Fundamental concept of probabilistic logic was first introduced by John von Neumann in 1960.Later up to 1980 it is converted in stochastic logic by Gaines introducing definitions and constructions of bit stream and in 1990 advancement in conventional technique which is probabilistic in nature used in digital circuits. From 1990 and onwards based on specific applications, as increasing demand on digital circuits it is used in decoding of error correcting codes. The techniques that collectively constitute continuous values by streams of random bits .The stochastic computing is a interesting blending of analog and digital concepts. It is probabilistic nature technique which is less cost design and more tolerant to soft errors. So logical interpretation for stochastic computation becomes an attractive solution for many applications. It is so called stochastic because it computes with analog probabilities but represents them by digital bit stream and processes them with logic circuits. Basic arithmetic operations can be tackled with very simple digital logic circuits with stochastic encoding scheme. General computing has some specific and deterministic path to estimate the functions whereas stochastic bit stream are randomly occurring. When probabilistic laws are applied to digital clocks, it results into stochastic computing. Output information is shown by 0 and 1's which are random in nature. They are represented by stochastic sequence. The strength of stochastic computing is that enables the implementation of complex arithmetic functions by means of standard

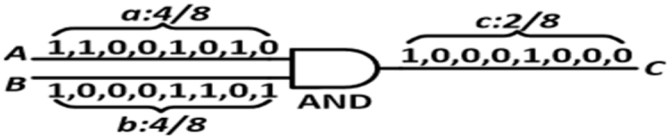


Figure1: Multiplication of stochastic logic (Reff no:2)

Suppose multiplication of two numbers can be implemented by simple AND logic gate function. So that it offers less area for arithmetic function. Recently it regains sufficiently great attention due to its fault tolerance and extremely low cost arithmetic units .Stochastic field has been utilize in the field of image processing, neural network, data mining, error correction and detection coding applications. It is also applied to the design of IIR, FIR and Gabor filter. Stochastic computing is a collection of techniques that represent continuous values by stream of random bits. Complex computations can be computed by simple bit wise operations on the streams along with low cost designs with minimum hardware complexity. This logic implementation overcomes the conventional methods such as implementation using Bernstein polynomial and implementation using FSM. Most circuit's presents in this computation are feed forward logic thus it can be pipelined at gate level for low power applications using threshold techniques. By using SC technique, minimum time is required for computation with small hardware system. Additionally, it is vigorous against noise, if a few bits in a stream are flipped, those errors will have no significant impact on the solution. It provides n estimate of solution that grows more accurate as we extend the bit stream. This property of SC is called progressive precision. This property introduces low discrepancy (LD) sequence, in which 0's and 1's are equally spaced between each other, so that it do not suffer from random fluctuations and fast converges and less error. Low Discrepancy sequence provides excellent progressive precision.

II. STOCHASTIC LOGIC APPROACH

First of all conversion of a binary number into its corresponding stochastic number is compulsory process and vice versa. This conversion is proceed by two blocks they are binary to pulse converter and pulse converter to binary. It consists of linear feedback shift register (LFSR), random number generator and comparator. Random number source usually a linear feedback shift registers which produces pseudo random bit stream. The processing flow generates output equal to 1 at each clock cycle when binary number is greater than generated random number. The sequence of random number 0's and 1's is manipulated by blocks over finite period of time called evaluations time period. Pulse to binary block consist of simple counter which count the number of 1's in stochastic signal. Pseudo random bit stream which is given by Random number source usually a linear feedback shift registers. We also focus on SNG for decreasing the power consumed, gain high accuracy, decreasing the number of random fluctuations and reducing the execution time. It is a digital approach to arithmetic computation. Inputs are determined by random bit stream. Implementation of hardware by arithmetic is very difficult so development of VLSI technology by FPGA has high integration and high performance. Random number generator and LFSR are described at each micro cycle, here random number is produced and contrast with binary which is arranged in registers. Random numbers are generated in the sequence of numbers and symbols. It is mainly designed for cryptographically secure computation base method. It is a seed secrete for sender and receiver which generate same set of numbers that automatically used as key. For the purpose of security, the RNG generate the number that attackers can't use the same number. There are two random numbers true random number and pseudo random number. True random number generally used to predict the pure randomness from the universe. Pseudo random number is seed value for computer and respective coded value. LFSR is the linearly function of existing state. The initial value of LFSR is represented as seed because the operation of registers is deterministic and it is used to develop an arrangement of bits that appear randomly.

Here input is taken as real value number, where it is in form of fractional part. Firstly, all inputs are converted into binary sequence. Then this binary form of input is arranged for stochastic operations. Stochastic output is send to ALU design for logical operations like AND, OR, NAND etc and arithmetic operation addition, subtraction. Finally output of stochastic ALU design again converted to binary form of respective value. These values of ALU are simulated by VHDL or Verilog programming and synthesis in qutertus2 and modelSim.

Generally, it is three stage operations. Initially LD sequences are generated in parallel depending on degree of parallelism. A counter which leads a specific sequence of counting, are used to implement the SNGs in parallel. In second stage comparator play very important role. These generated sequences are sending to comparator units where are compared with input probability to produce stochastic bit stream. It follows the condition that comparator produce 1 if the random number is less than binary number and otherwise 0. Third stage basically gives the binary output. It is generated by stochastic to binary conversion unit, which comprises of counters that counts number of ones in stochastic bit stream. Various softwares was used for simulation and synthesis of VHDL coding that are required in stochastic logic such as modelSim and quatus2.Also Altera DE2 board is used for hardware interfacing. ModelSim support both VHDL and Verilog designs. Quatus2 design software provides a complete multiple way and various options that easily adapt to vendor need.

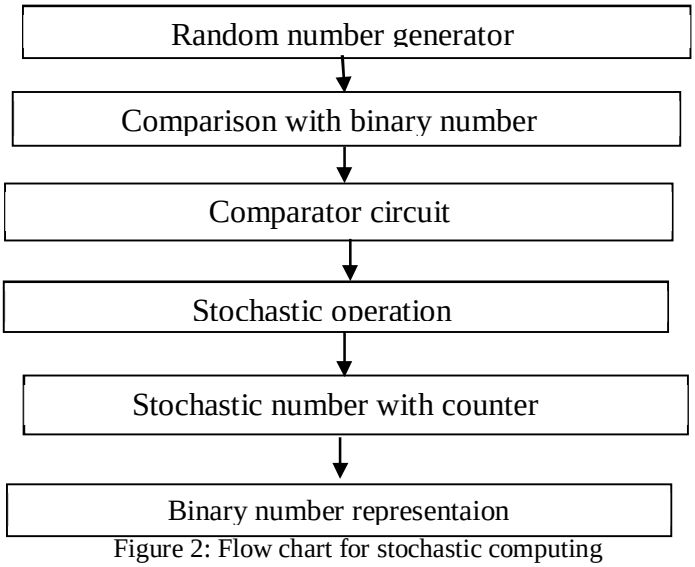


Figure 2: Flow chart for stochastic computing

III. LITERATURE REVIEW

Weifang Qian et al [1] present methodology for preparation of stochastic logic which is based on probabilistic bit stream. This paper also looks over the low economy and sources and fault. Also study the value of the architecture on a collection of benchmark for digital image processing. Stochastic computing required small area and more tolerate to soft fault than deterministic implementations.

Peng Li et al [2] this paper investigate Computation performed on stochastic bit streams is less efficient than that based on a binary radix because of its long computation process. However, for certain complicated arithmetic operations, computation on stochastic bit streams can ease less energy and tolerate more soft faults. In addition, the latency issue could be solved by using a faster clock frequency or additionally with a parallel processing approach. To take advantage of this computing technique, previous work proposed combinational logic-based rearrange architecture to perform complicated arithmetic operations on stochastic streams of bits. This method improves rearrange architecture using sequential logic compared to the previous approach, the proposed rearrange architecture takes less hardware area and consumes little energy, while achieving the same performance in terms of processing time and fault-tolerance.

Peng Li et al [3] this paper proposes a new finite-state machine (FSM) topology for complicated arithmetic computation on stochastic bit streams. It explained a general methodology for synthesizing such FSMs. Analysis show that these FSM-based implementations are more tolerant to faults and less costly in terms of the area-time product that conventional implementations. This paper will focus on study of synthesis techniques for general purpose computation. Their future work is completely focused on stochastic design of a microprocessor.

Armin Alaghi et al [4] this paper surveys the key concepts of stochastic number representation and circuit structure. It gives examples of the potential applications of SC and showed some practical problems that are yet to be solved. The role of randomness and correlation in stochastic number representation and generation remains poorly understood. As we have seen here, judicious use of pseudorandom numbers leads to more accurate results than purely random ones. Although individual SC operations like multiplication can now be implemented with high precision, the problem of efficiently maintaining such precision across multiple operations and circuits is difficult and largely unexplored. Stochastic number generators continue to be among the costliest components of stochastic circuits. The problems of designing and deploying cost-effective SNGs that ensure a desired, system-wide level of accuracy or precision is far from solved.

Armin Alaghi et al [5] this paper present novel methods for SN generation which give accuracy and run time trade off- (PP) which allows computational accuracy to grow systematically. Also Monte Carlo method, show that SC performance can be greatly achieved by low discrepancy (LD) sequences that are predictably progressive instead of the usual pseudo-random number sources. At the end LD stochastic numbers in SC, much faster and more accurate results than existing stochastic designs.

Armin Alaghi et al [6] it gives introduction about stochastic logic. Stochastic computing (SC) employ conventional logic circuits to implement analog-style arithmetic functions acting on digital bit streams. It exploits the advantages of analog computation powerful basic operations, high operating speed, and fault tolerance in important applications such as sensory image processing and neuromorphic systems. At the same time, SC exhibits the analog drawbacks of low precision and complicated underlying behavior. Although studied since the 1960s, many of SC's fundamental properties are not well known or well understood. This paper presents, in a uniform manner and notation, what is known about the relations between the logical and stochastic behavior of stochastic circuits. It also considers how correlation among input bit-streams and the presence of memory elements influences stochastic behavior. Some related research challenges posed by SC are also discussed.

Yin Liu et al [7] this paper addresses computing complicated functions using unipolar stochastic logic. Stochastic computing requires simple logic gates and is inherently fault-tolerant. Thus, these structures are well suited for nanoscale CMOS technologies. Implementations of complex functions cost extremely low hardware complexity compared to traditional two's complement implementation. In this paper an approach based on polynomial factorization is proposed to compute functions in unipolar stochastic logic. In this approach, functions are expressed using polynomials, which are derived from Taylor expansion or Lagrange interpolation. Polynomials are implemented in stochastic logic by using factorization. Experimental results in terms of accuracy and hardware complexity are presented to compare the proposed designs of complicated functions with previous implementations using Bernstein polynomials.

Keshab K. Parhi et al [8] stochastic logic based implementations of complicated arithmetic functions using truncated Maclaurin series polynomials have been presented in this paper. This technique based on Horner's rule, factorization and format conversion are proposed. The generalized methods for stochastic unipolar implementations of tanhax and sigmoid (ax) for arbitrary a > 0 have also been presented. However, the proposed approach for tanhax and sigmoid (ax), where a is greater than 1, requires more hardware and

leads to more fault than FSM based implementations. Future work will be directed towards stochastic logic implementations of different types of machine learning classifiers.

Rosima Akhtar et al [9] this paper described the key concept of stochastic computing, its variants, conversion process and stochastic circuits. It also address main challenges related with stochastic computing and their possible solutions are also highlighted in this paper.

IV. SUMMARIZED WORKDONE

Table1. Shows the study of various methods used in the stochastic logic and compares the various parameters such that area, delay, cost, hardware units, power consumptions etc., which play very vital role for working of design efficiently.

Table. Summary of methods used

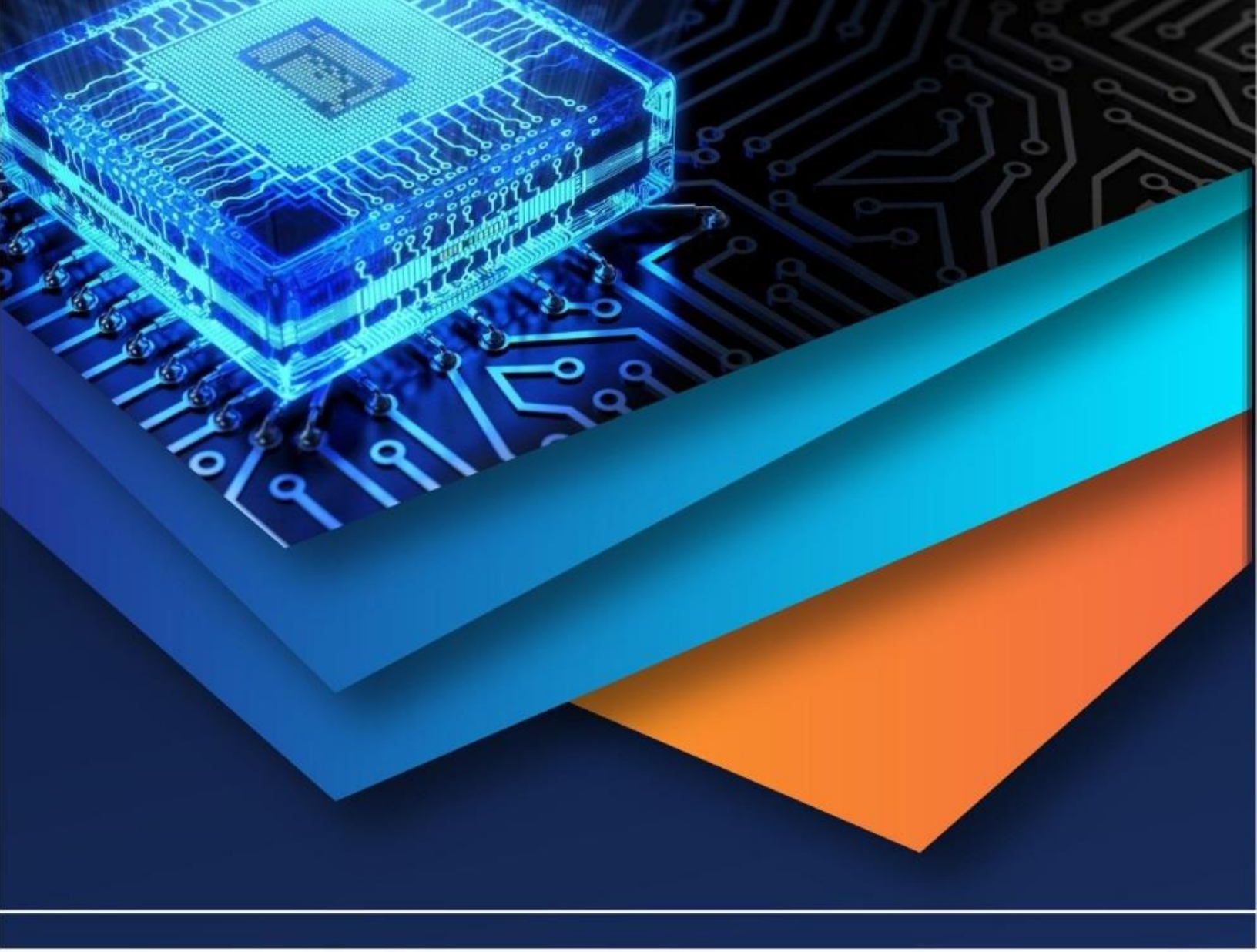
Reff no.	Methodology	Result
1.	Method with serial bit stream for synthesizing stochastic logic for arithmetic operation and reconfigurable architecture	Less area than conventional hardware and observed error below 20%with less noise level of 10%
2.	Reconfigurable architecture using finite state machine	Less area small delay product compared to ReSC architecture based on binary radix
5.	Stochastic number generation technique, LD sequence with progressive prison property	area consumption for non-stochastic method is12214, for stochastic without PP is 35 and with PP is 35in µm^2 leading fast and highly accurate circuit
6.	Stochastic logic by combinational circuit	Not affected by autocorrelation like sequential circuit
7.	Computing complex function using factorization in unipolar stochastic logic and compared with Bernstein polynomial	Computational error reduce more than 50%and area is reduced by 88%
8.	Computing arithmetic function using stochastic logic by series expansion	Propose system reduced large area, order, delay

V. CONCLUSIONS

The various methods and techniques used for the stochastic logic computation and generation of the stochastic numbers are described in this paper. Paper presents comparisons between various parameters which are necessary for efficient architecture of any function by using stochastic logic implementation. But there is need to improve the precision in all parameters such as less area, accuracy, fast computation with less error and low power consumption.

REFERENCES

[1] Weikang Qian, Xin Li, Marc D. Riedel, Kia Bazargan, David J. Lilia "An Architecture for Fault Tolerant Computations with Stochastic Logic, " IEEE transactions on computers 2011.
[2] Peng Li, Weikang Qian, David J. Lilia "A Stochastic Reconfiguration Architecture for Fault Tolerant Computation with Sequential Logic," International Conference on Computer Design 2012.
[3] Peng Li, David J. Lilja, Weikang Qian, Kia Bazargan and Marc Riedel "The Synthesis of Complex Artihmetic Computation on Stochastic Bit Stream Using Sequential Logic," International Conference on Computer Aided Design 2012.
[4] Vincent Canals, Antoni Morro, Antoni Oliver, Miquel L. Alomar, and Josep L. Rossello "A New Stochastic Computing Methodology for Efficient Neural Network Implementation," IEEE Transactions On Neural Networks And Learning Systems, Vol. 27, NO. 3, March 2016
[5] Armin Alaghi, John P. Hayes "Fast and Accurate Computation using Stochastic Circuits" Design Automation and Test in Europe Conference and Exibition 2014.
[6] Naoya Onizawa, Daisaku Katagiri, Kazumichi Matsumiya, Warren J. Gross and Takahiro Hanyu "Gabor Filter Based on Stochastic Computation," IEEE Signal Processing Letters Vol.22, 2015.
[7] Armin Alaghi, John P. Hayes "On the Functions Realized by Stochastic Computing Circuits," Great lakes Symposium on VLSI 2015.
[8] Yin Liu, Keshab K. Parhi "Computing Complex Functions using Factorization in Unipolar Stochastic Logic," Great Lakes symposium on VLSI 2016.
[9] Romisa Akhktar, Farooq A. Khanday "Stochastic Computing System : Applications, Challenges and Solutions," Proceeding of the International Conference on Communication and Electronic System 2018
[10] Keshab K. Parhi and Yin Liu "Computing Arithmetic Functions Using Stochastic Logic by Series Expansion," IEEE TRANSACTIONS ON EMERGING TOPICS IN COMPUTING 2019.



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