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Analysis of CNTFET Based Circuit Performance over CMOS in Inverter and OPAMP

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Abstract*— Carbon nanotubes (CNTs) exhibit high current handling capability, higher thermal and electrical conductivity and higher transport properties, presently the Carbon nanotube technology are be the best competitor and alternative of conventionally used Complementary metal oxide semiconductor technology(CMOS). In this paper, CNT based field effect transistors known as CNTFET is compared with the conventionally used silicon based technology MOSFETs on the basis of circuit level performance. Those two technologies are compared with simulation work performed on logic families such as inverter and non inverting OPAMP on different predefined parameters such as power delay product, power dissipation, input output resistance, gain, phase margin, slew rate and power delay. We used minimum gate length of 32nm for both MOSFET and CNTFET. The results of simulation conclude that in CNTFET based logic gates, power consumption and delay is about 10times lower, leakage is reduced to 100% compared to the MOSFET based devices such as inverter. These excellent performances characteristics with different variations are also exhibit excellent robustness.
***Keywords*— Carbon Nanotubes, MOSFET, CNTFET, SWNTs, VTC**

I. INTRODUCTION

The CMOS technology may posses some limitations, to overcome these limitations we introduce the new technology carbon nano tube technology. It have many numbers of single walled nanotube that posses outstanding transport capability in low voltage bias, less power consumption, power delay and power leakage etc [1][2]. CNTFET based devices posses these fundamental characteristics to replace silicon based MOSFET devices. Many drawbacks are encountered in CNTFET, these drawbacks arise under manufacturing process like misaligned CNTs, contact resistance and diameter problem. Now many researches have successfully executed to supersede these drawbacks by using accurate modeling for simulation work. CNTs is a carbon allotrope that consist hollow cylinder structure that provides a novel superior material for optimize the electronic transport in various dimension. In modern era of invention of micro fabrication techniques are available for reduced the size and increase the performance of the device. In various techniques of fabrication has pushed the microstructure to the limit of 10 nm conviction. In other side VLSI technology will applied for Carbon nano tube SWNTs have a diameter below 1 nm and it is a 1D conductor. That reduces the many transverse modes in compare to the VLSI technology. Carbon nanotubes are metallic or semiconducting based on its chirality's and its lattice structure gives ballistic transport properties in room temperature. All aspects to reduce power consumption are achieved by lowered the numbers of transistor but that circuit is suitable only for minimum sized devices only. Digital and analog circuits are possibly operated in the ultra low voltage levels less than 0.4volt. This is known is threshold region and the performance are lowered in this region due to small energy fulfillment that will cause poor circuit performance of standard circuits. That shows optimal reduced energy level circuits exhibit minimum size devices. By this paper, introduced the new better preformed robust technology in the form of CNTFET. In this assessment, simulation work is done by using the predictive technology model for a silicon based MOSFET and HSPICE based model which is used for the simulation of CNTFET [3][4][5]. Channel length of 32nm is commonly used for both technologies for the evaluation of the better performance characteristics in different predefined parameters. Circuit modeling used for evaluation is discussed below for the perfect design to encountered best performing characteristics in different variations. First we understand the structure of MOSFET like CNTFET.

II. MOSFET LIKE STRUCTURE OF CNTFET

CNTs are sheets of graphene rolled into tubes. The single-walled CNT can be either metallic or semiconducting just depending on its

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chirality. However, the direction in which the graphene sheet is rolled. Semiconducting nanotubes have attracted the widespread attention of circuit designers as an alternative channel implementation for high performance transistors [6][7]. CNTs can be used to develop Carbon Nanotube Field Effect Transistors (CNFETs) in which their conducting channel is made by carbon nanotubes these are reduced in size and gives extra ordinary electrical transfer capability with less power loss and low power disipation. CNFETs posses less power and intrinsic delay (CV/I), which shows higher electron mobility compared with bulk silicon power leakage are also less and they provide greater energy-delay product [3]. CMOS circuit blocks are also easily replaced by them because their operation principle is similar, so CNFET are the best candidature to replace CMOS**.**

The thin films of SWNTs can potentially decrease the device to device variations which are occurred in single tube transistors by the statistical averaging.

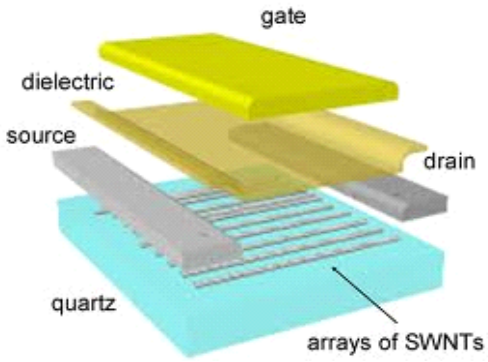


Fig. 1 Top view of CNTFET with multiple SWNTs. On the other hand transistor which active conducting channel is aligned arrays of SWNTs are retain the high mobility as in a SWNT transistor.

The structure of CNTFET is almost the same like silicon MOSFET except the CNT is attached in the transistor and acts as the channel. CNTFET operates on the same principle of MOSFET. The electrons travel from the source terminal to the drain terminal. In this paper, we focus on MOSFET-like CNTFET structure as shown in Fig 1, which illustrates the CNTFET with multiple SWNTs. However, transistor which active conducting channel is aligned arrays of SWNTs are retain the high mobility as in a SWNT transistor [8][9].

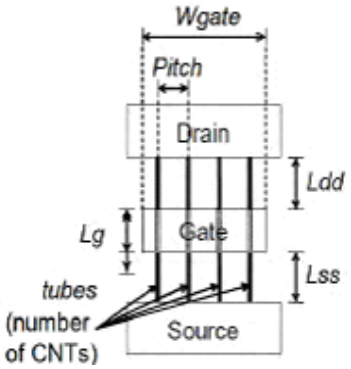


Fig.2 CNFET Schematic using SWNTs in channel region

A structure of CNTFET illustrates in Fig 2. This is structured like MOSFET. The source and drain is heavily doped and CNTs channel region remains undoped which exhibits substantially improved performance by work as interconnects between devices. In the undoped region gate will control the conductance. However; MOSFET-like CNTFET operates on the principle of modulating the barrier height by applying gate voltage. The drain current is controlled by the number of charge that is induced in the channel by gate potential [3][8][9].

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III. PERFORMANCE ANALYSIS

By modeling and design rules inverter and OPAMP are design with channel length of 32nm for both MOSFET and CNTFET. Comparison work is done to evaluate the better performance characteristics in different variations. By the fig. 3 & 4 is the inverters performance at various threshold voltages DC curves get steeper and steeper when it reaches to 0 Dc curve is no longer work as inverter because gain is below to 1. In that current flow through diffusion when it reaches to 0 inverters works off but in reality it is not turns off immediately, it turns off gradually.

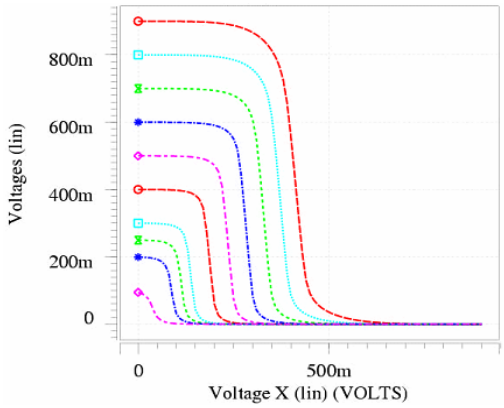


Fig.3 MOSFET Inverter at various threshold voltages.

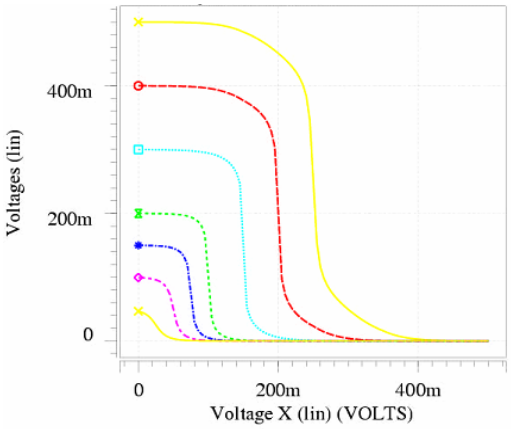


Fig.4 CNTFET Inverter at various threshold voltage.

By the fig.5 shows that CNTFET has similar curve in the threshold voltage as MOSFET. But CNTFET posses smaller current compared to MOSFET. At the trasition region CNTFET posses steeper curve because of the higher gain. This improved the noise margin under low power consumption [3].

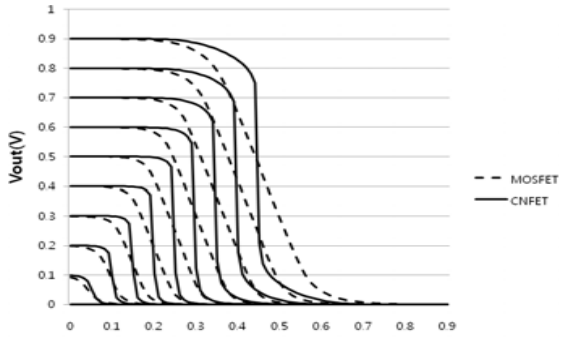


Fig.5 Voltage transfer characteristics of CNTFET and MOFET inverters in various power supplies.

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TABLE I
Comparison of Si based MOSFET and CNTFET inverter (32nm) in various parameters like Power, Delay and maximum power leakage.

Parameter	MOSFET	CNTFET	Unit	Comments
Delay	17.66	2.42	per sec	Lower by 10 times
Leakage	10.52	0.14	nW	Reduced by 100%
Power Consumption	1.39	0.11	Micro W	Lower by 12Times

TABLE II
Comparison of Si based MOSFET and CNTFET OPAMP.

Parameter	MOSFET	CNTFET	Unit	Comments
Input Resistance	1E20	1E12	Ohm	Decreased
Output Resistance	52.12	6.85	Ohm	Reduced by 600%
Settling Time	4.5us	387ns	Sec.	Faster by a factor of 10
DC gain	1.909	1.90	-	Equal
Phase Margin	-73.6	-60.1	Degrees	Reduced
Power Dissipation	289.4	67.74	uW/M ohm	Reduced by 327.22%
Slew Rate(Rise) {10% to 90%}	2.0147	9.66	V/uS	Faster by 390%
Slew Rate(Fall) {10% to 90%}	-2.23	-8.94	V/uS	Faster by 283.2%

IV. CONCLUSIONS

Finally we can conclude from the fig.5 CNT inverter posses higher gain because in the transition region, it has steeper curve. They also exhibit small amount of current in the circuit. So by this noise margin is improved about 22.5% under low supply of power

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voltage. By table I and II obtained from the simulations illustrates that carbon nanotube technology is far superior as compared to silicon based CMOS technology. In future, nanotubes will eventually replace silicon and even the simplest; the smallest of technologies will have nanotube as its basic block. The limitation of fabrication is the only obstacle that is obstructing the growth of the carbon nanotube industry. Eventually commercialization of carbon nanotube will come to pass. But with a compromise in directivity proving that this method is efficient with much reduction in computation time and complexity.

In future, the extension of the study would be to physically examine the logic gates and understand the competence of carbon nanotube compared to the traditional CMOS technology and the influence of the environment on nanotube's performance. A physical performance observation of carbon nanotube will confirm our study to a commercial basis and will prove that Moore's law can still be valid.

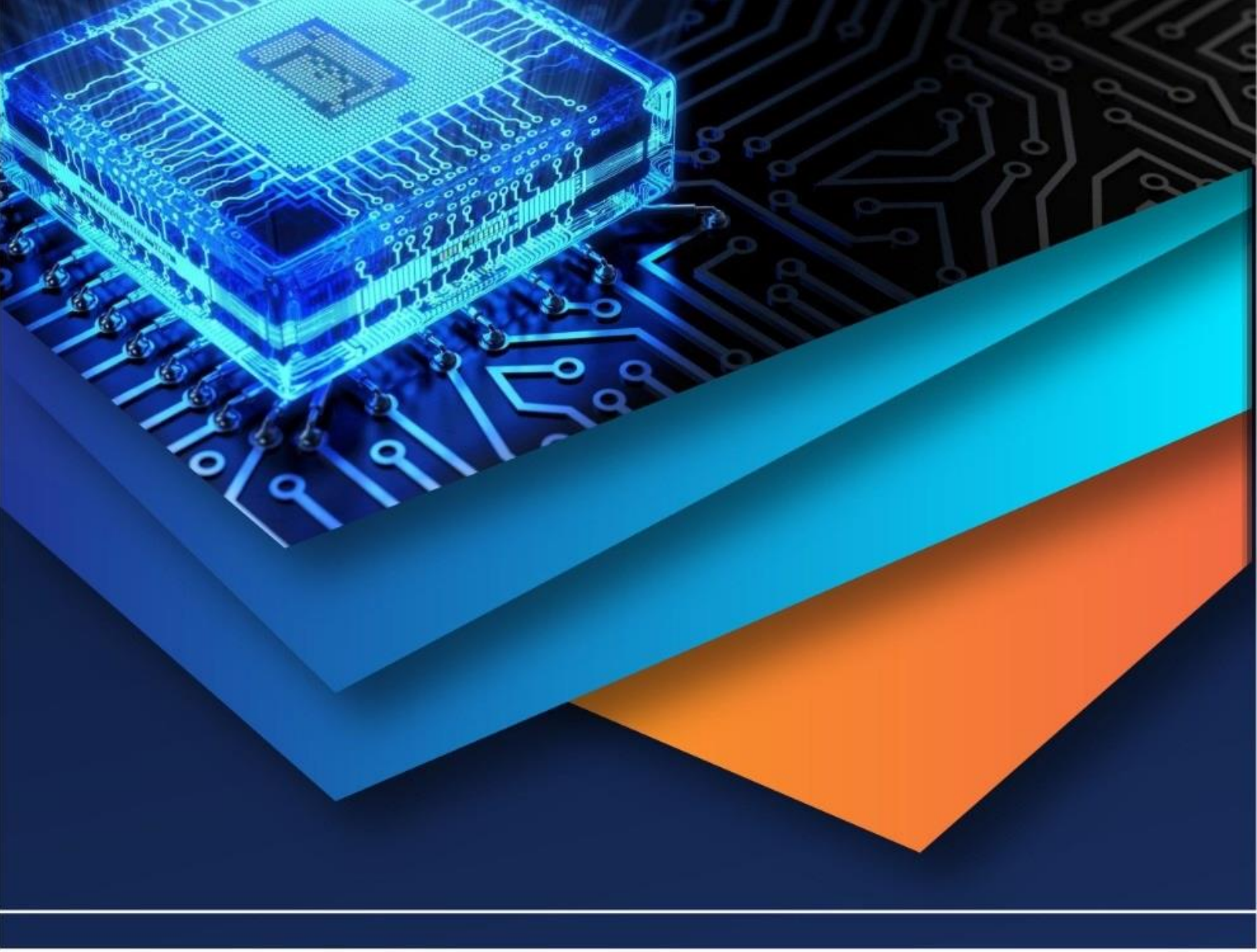
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