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Analysis of Five Level Diode Clamped in Comparison with Cascaded H Bridge Multilevel Inverter

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Abstract: ***The DC control is changed over to AC control by a power hardware gadget at a dimension of the ideal yield voltage and recurrence level portrayed as inverter. The dimensions of a yield voltage or current is delivered by the inverters having voltage sources and those sources might be either 0 or +Ve Vdc or –Ve Vdc which is essentially known as two level inverters. These ordinary two dimension inverters have certain points of confinement in working at high frequencies for the most part because of exchanging misfortunes and requirements in device rating. The issue is settled by methods for multilevel inverters, that utilization frequencies having lower exchanging and produce high voltages with improved total harmonic distortion (THD) without the utilization of channel (filter). In a power electronic circuit, the activity of multilevel happens both in inverter and rectifier mode. For the powerful uses of staggered inverters, the choices of new assortment of intensity converter have risen and these aides in the decrease of the substance of harmonics. In this postulation, a model of five level Diode braced and Cascaded inverter has been created utilizing MOSFETS. The structuring comparators produce the gating beats. So as to keep up the various dimensions of voltage at specific timeframe, the beat width of gating beats is kept up by the conduction timespans of MOSFETS. The re-enactment models dependent on five level have been created and THD in the sum total of what cases have been discovered.***

Keywords: Total Harmonic Distortion (THD), Diode Clamped Multilevel Inverter (DCMI) , Pulse Width Modulation (PWM), Cascaded H Bridge, Fast Fourier Transform (FFT)

I. INTRODUCTION

At the point when there is a need of DC to AC, inverter gives this facility of change when required. This is essentially done by two level inverters, yet one of the most transcendent downside of two level inverter is its output results in higher THD. When we talk about THD control, multilevel inverter plays an very important role of lessening the THD in the AC yield. Power semiconductor switches and capacitor voltage sources are properly arranged which is collectively considered as 'multilevel inverter', which produces voltage of stepped waveform. At the point when the switches are appropriately commutated expansion of capacitor voltages happens, which results in large voltage at the output side while the semiconductor switches have to handle diminished voltage. Nabae et al [7] introduces the term multilevel for three level inverter. Different topology of multilevel inverters are: Diode-clamped [7], Capacitor clamped [5] and Cascaded multicell with separate dc source. Recently, some new multilevel topologies have been developed. It includes asymmetric or hybrid inverters [26]. In asymmetric unequal dc sources are used. Hybrid inverters are developed using different topologies.

II. MULTILEVEL INVERTERS

The multilevel inverter topologies are of various type such as [7]:

A. Diode Clamped Multilevel Inverter

The 'Diode clamped inverter' is the most normally utilized multilevel topology, in this the diode is utilized as the bracing device to clamp the dc bus voltage in order to accomplish ventured waveform in the output voltage. The neutral - point converter proposed by Nabae, Takahashi, and Akagi in 1981 was basically a three-level diode-clamped inverter [7]. A three-level diode clamped inverter comprises of two sets of switches and two diodes. Each switch sets works in integral mode and the diodes used to give access to mid-point voltage. . In a three-level inverter every one of the three periods of the inverter shares a typical dc bus, which has been subdivided by two capacitors into three levels. The DC bus voltage is divided into three voltage levels by utilizing two arrangement associations of DC capacitors, C1 and C2. In a three-level diode clamped inverter, there are three various conceivable exchanging states which apply the stair case voltage on output voltage identifying with DC interface capacitor voltage rate. For a three-level inverter, a set of two switches is on at some random time and in a five-level inverter, a group of four switches is on at some random time, etc.

In a ***m*** level diode clamped multilevel inverter:
Number of switches = *2(m-1)*
Number of diodes = *(m-1) * (m-2)*
Number of capacitors = *(m-1)*

B. Cascaded H Bridge Multilevel Inverter

The essential thought behind Cascaded multilevel inverter is arrangement association of single-stage inverters with discrete dc sources. This three-level cascaded converter is the fundamental cell that is utilized to fabricate multilevel converters. A multilevel converter is effectively manufactured interfacing essential three-level cells in arrangement [5], [13]. Notice that every essential cell needs a free voltage source and this is one of the most significant disadvantages of this multilevel converter topology.

In a 3-level cascaded inverter each single-stage full-connect inverter creates three voltages at the yield: +Vdc, 0, - Vdc (positive dc voltage, zero and negative dc voltage). This is made conceivable by interfacing the capacitors consecutively to the ac side through the power switches. The subsequent yield ac voltage swings from - Vdc to +Vdc with three levels, - 2Vdc to +2Vdc with five level and - 3Vdc to +3Vdc with seven level.

1) Features

a) Various non-conventional energy sources can also be used with CHB such as PV cell, biomass, fuel cell and each cell of CHB needs independent dc sources.

b) For *n* cell connected in CHB there are *2n + 1* output voltage level.

c) DC sources cannot be connected in back-to-back fashion because it will introduce short circuit, if not synchronised properly.

C. Flying Capacitor Multilevel Inverter

The Flying Capacitor inverter on the other hand known as capacitor-clamped. It was proposed by Meynard and Foch in 1992 [8]. The structure of this inverter is like that of the diode braced inverter aside from that as opposed to utilizing clamping diodes, the inverter utilizes capacitors in their place. The flying capacitor includes arrangement association of capacitor clamped exchanging cells. This topology has a stepping stool structure of dc side capacitors, where the voltage on every capacitor contrasts from that of the following capacitor. The voltage increase between two contiguous capacitor legs gives the size of the voltage ventures in the yield waveform.

1) Features: The major issue in this inverter is the essential of innumerable capacitors. Given that the voltage rating of each capacitor used is equal to that of the rule control switch, a m-level converter will require a total of (m - 1) * (m - 2)/2 aide capacitors for each stage leg not withstanding (m - 1) essential dc transport capacitors.

III.CONTROL TECHNIQUES FOR MULTILEVEL INVERTER

A. Fundamental Switching Frequency

1) Space Vector Control

2) Selective Harmonic Elimination

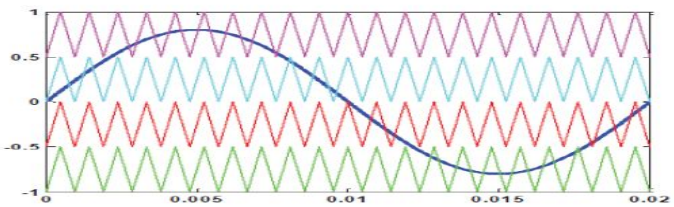
B. High Switching Frequency PWM

1) Space vector PWM

2) Sinusoidal PWM

C. Sinusoidal Pulse width Modulation [2] [14] [23]

1) Phase Disposition: Regular technology is shown in Figure 3.2, under the multi-stage SPWM technology. The idea of steering is to compare different carriers with basic signal.m-1 carriers for the m level phase converter and the reference signal and frequency (50 Hz) is required .



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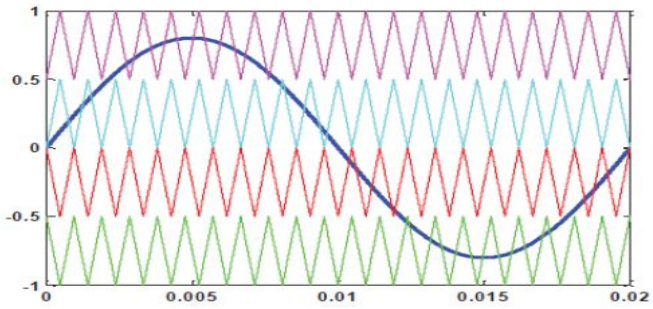
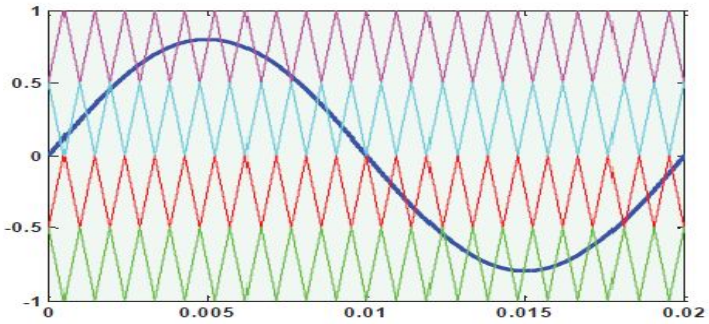
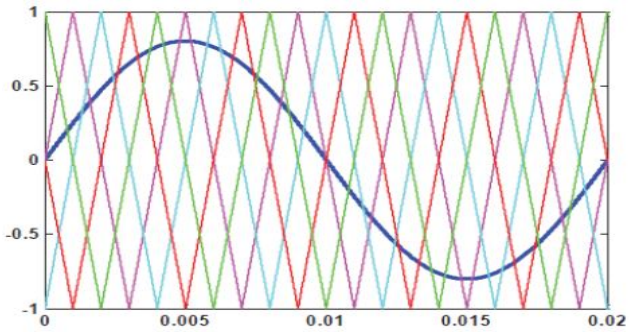
2) *Phase Opposition Disposition:* In 'Phase opposition disposition method' above two carrier wave are in phase. The carrier waveforms below zero reference value are also in phase but 180- degree phase shifted from above two carrier waveforms



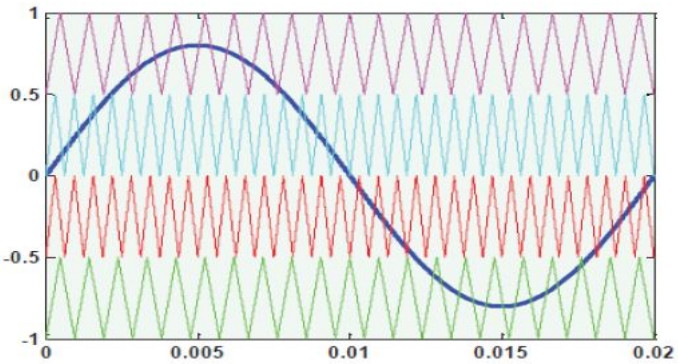
3) *Alternative Phase Opposition Disposition:* One reference signal and m-1 carrier waveforms are required for m level and there is phase difference of 180 degree between all carriers.



4) *Phase Shifted:* 'Phase shifted technique' also needs m-1 carrier waveforms and a reference signal to produce m level inverter. In phase shifted carriers are shifted horizontally by 180/m degree where m is the level of inverter.



5) *Variable Frequency Carrier Wave:* In all previous methods such as PD, APOD, POD and PS the numbers of the switching in upper and lower switches is more than middle switches. In this method, carrier frequency of middle switches vary with two others, in order to balance the number of the switching.



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IV. SIMULATION MODEL OF FIVE LEVEL INVERTER

The proposed multilevel inverters are designed and simulated in the MATLAB/Simulink. We have made the Diode Clamped multilevel inverter and Cascaded H bridge multilevel inverter of five level. The parameters used for these model are : For DCMI source voltage = 400V, Reference wave of 5 V, Carrier Wave of 2.5 V, Capacitor of 2200µF and for CHB inverter source voltage of 100 V.LC filter of L =2mH and C=2200µF .

A. Diode Clamped Five level Inverter

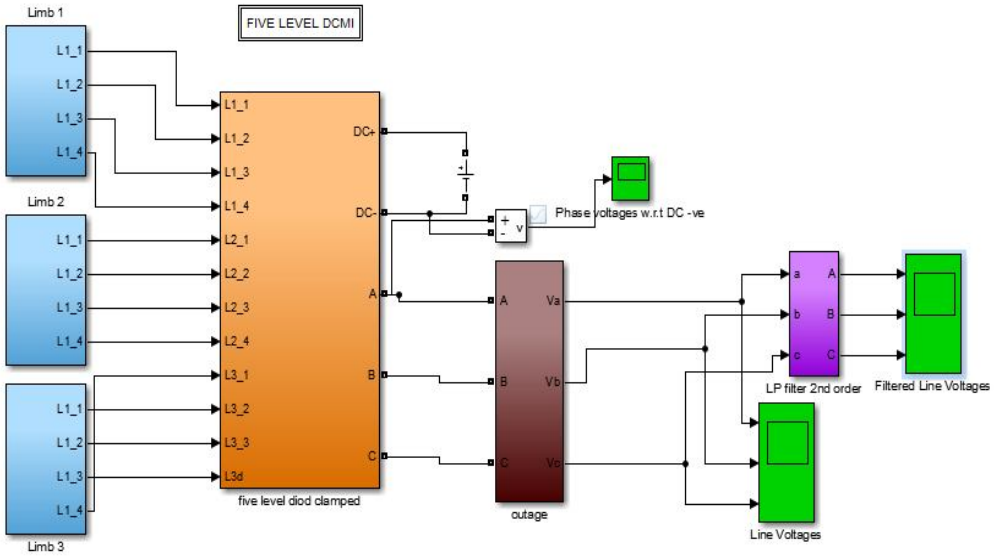

Fig.2(a) Simulation model of diode clamped multilevel inverter for 5-level

Five level DCMI is modelled based on the theoretical concepts explained above. Here the sub system for pulse generator is modelled where one reference wave (sine wave) and four carrier waves (triangular wave) are taken. First two triangular waves are applied across the positive half cycle of the sine wave and next two triangular wave is applied across negative half cycle of the sine wave. Based on the concepts explained in modulation techniques, eight pulses are generated. These pulses are given to the switches in one phase leg of a five-level inverter. Similarly, the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120 degrees.

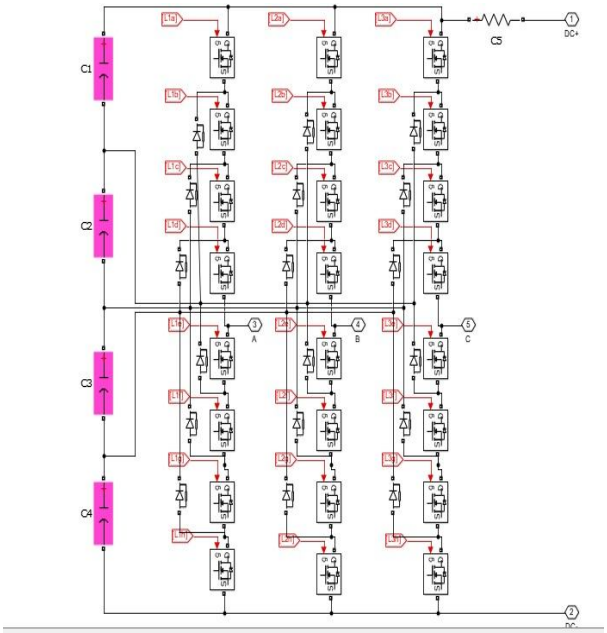

Fig. 2(b) DCMI Simulink circuit

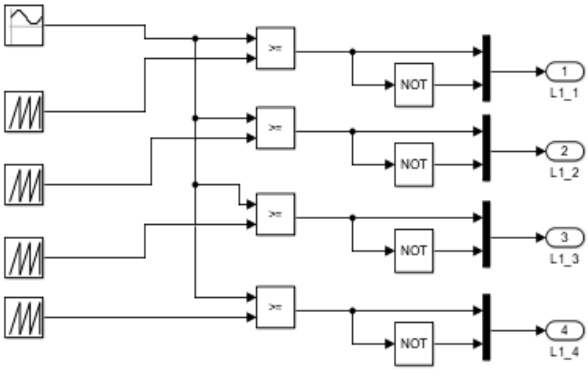

Fig.2(c) Carrier modulation signal circuit

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B. Cascaded H Bridge Five level Inverter

Five level Cascaded H Bridge multilevel inverter can be modelled based on literature given above. Fig 3(a) shows the one phase of five level CHB multilevel inverter in this two cells are connected in series in order to increase the number of levels. Fig 3(b) shows the complete simulation model of five level CHB multilevel inverter.

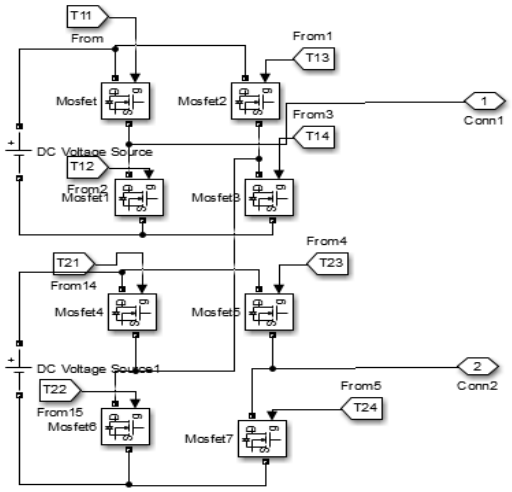

Fig.3(a) One phase of Five level CHB multilevel inverter

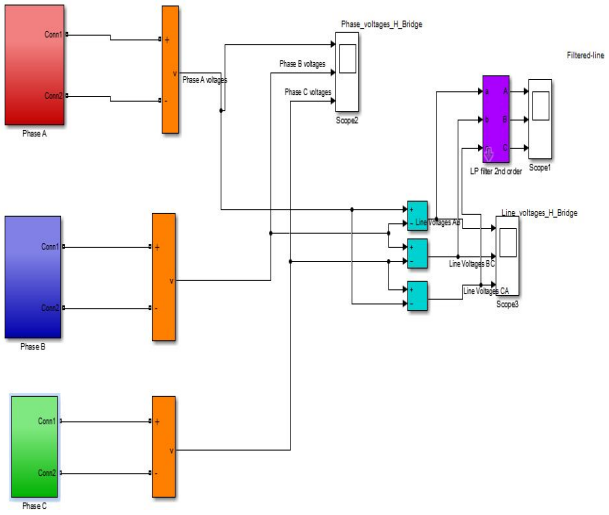

Fig.3(b) Simulation model of Five level CHB inverter

V. RESULT ANALYSIS

The Simulink model of DCMI and CHB multilevel inverter is shown in figures 2(a) and 3(a) respectively.We have obtained several line voltages and phase voltages.

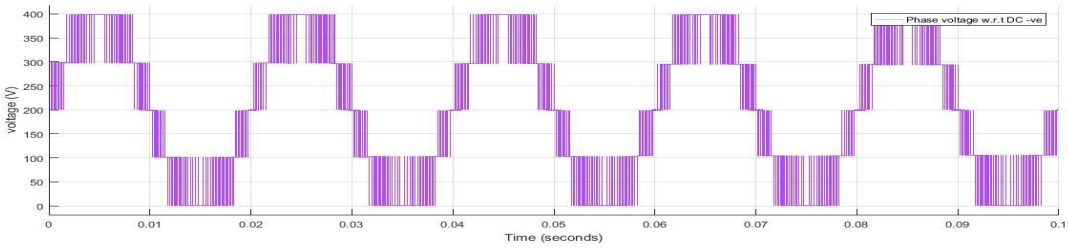

Fig.4(a) Phase Voltage waveform w.r.t DC negative terminal of DCMI

Figure 4(a) shows the phase voltage waveform w.r.t negative terminal of the voltage source, it is obtained in order to verify the level of the multilevel DCMI, as in waveform there are 5 steps so the multilevel inverter is of five level.

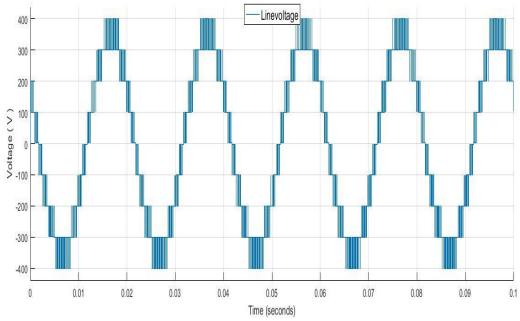

Fig.4(b) Phase to Phase voltage waveform of DCMI

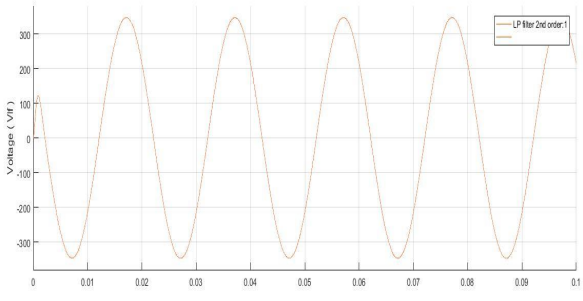

Fig.4(c) Filtered phase to phase voltage waveform of DCMI

Figure 4(b) illustrates the Let the number of level is denoted by *m.* Line voltage waveform is shown which is having the number of steps S such that S= (2*m-1), as the numbers of steps increases harmonic distortion get lower.

Figure 4(c) shows that by using filter output voltage may become more smoother and more nearly to sinusoidal and hence harmonic can be reduced or eliminated.

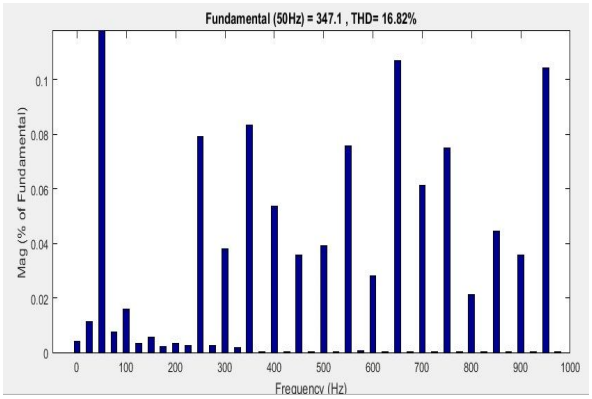

Fig.4(d) THD of Phase to phase voltage of DCMI

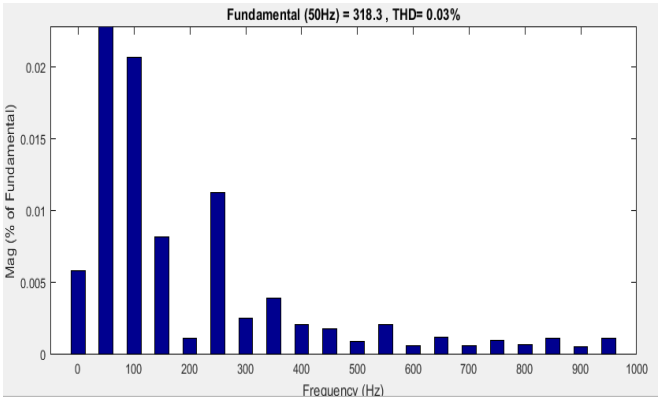

Fig.4(e) THD of filtered phase to phase voltage of DCMI

From FFT analysis shown in figure 4(d) and figure 4(e) shows that THD has been reduced to 0.03 % from 16.82 % of without filtered waveform.

Now let us see the different voltages waveform and THD of CHB multilevel inverters. As output of five level CHB varies from $2V_{dc}$ to $-2V_{dc}$, output voltages are more than input voltage.

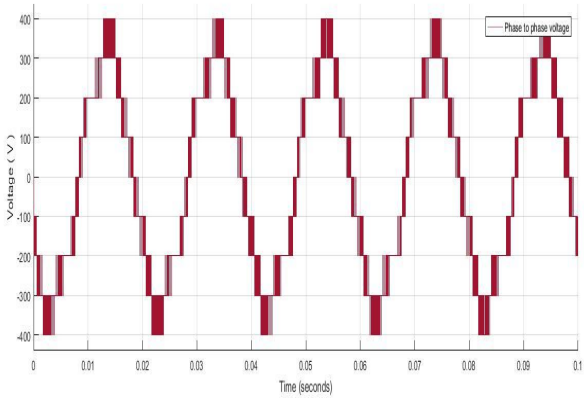

Fig.4(f) Phase to phase voltage of CHB

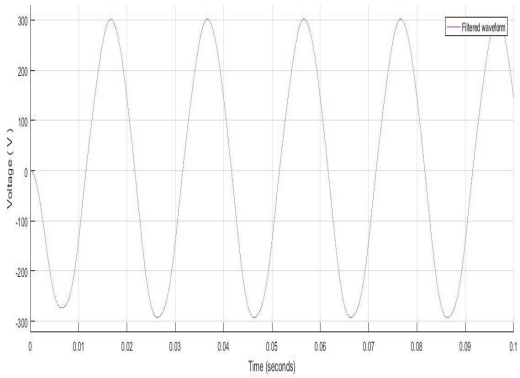

Fig.4(g) Filtered phase to phase voltage of CHB

In figure 4(f) again we can see that for phase to phase voltage number of steps increases and waveform become smoother than phase to neutral voltage and hence harmonic distortion in the output decreases.

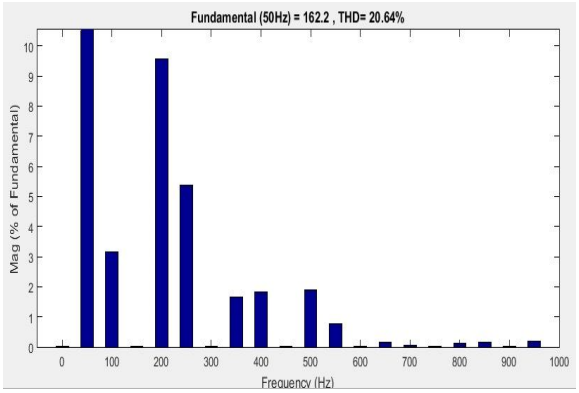

Fig.4(h) THD of phase to phase voltage of CHB

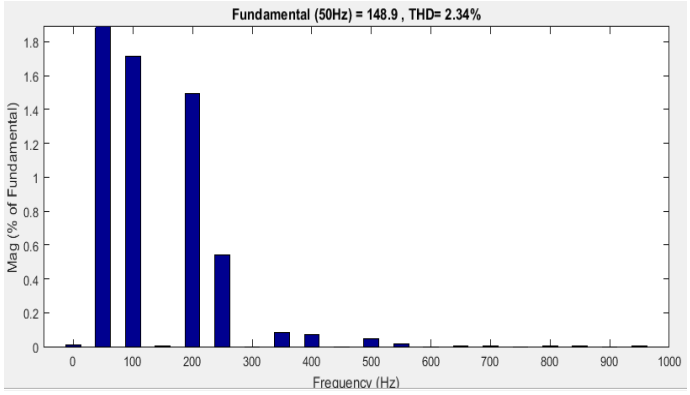

Fig.4(i) THD of filtered phase to phase voltage of CHB

From the THD analysis of different voltages we see that THD for Diode clamped multilevel inverter is 16.82% and that of Cascaded H Bridge multilevel inverter is 20.63 %. After filtering THD reduces to 0.03% for Diode clamped and 2.34% for Cascaded multilevel inverter.

The above discussion can be summarised in tabular form as shown in table 1.

Table 1. Comparison of THD of DCMI And CHBMI

S.No.	Inverters	THD of output voltage in %	THD of filtered output voltage in %
1.	Diode clamped multilevel inverter	16.82	0.03
2.	Cascaded H Bridge multilevel inverter	20.63	2.34

VI. CONCLUSION

The different kinds of topologies of 5-level staggered inverter were considered, reenacted, broke down and the ideal yields were acquired in the MATLAB/Simulink Environment. Particularly, an overall investigation of fell inverter and diode clamped inverter alongside and without sifted line voltage utilizing FFT examination is discovered . It was discovered that the relating THD esteems with and without filter was similarly low for diode clamped staggered inverter when contrasted with H bridge staggered inverter.

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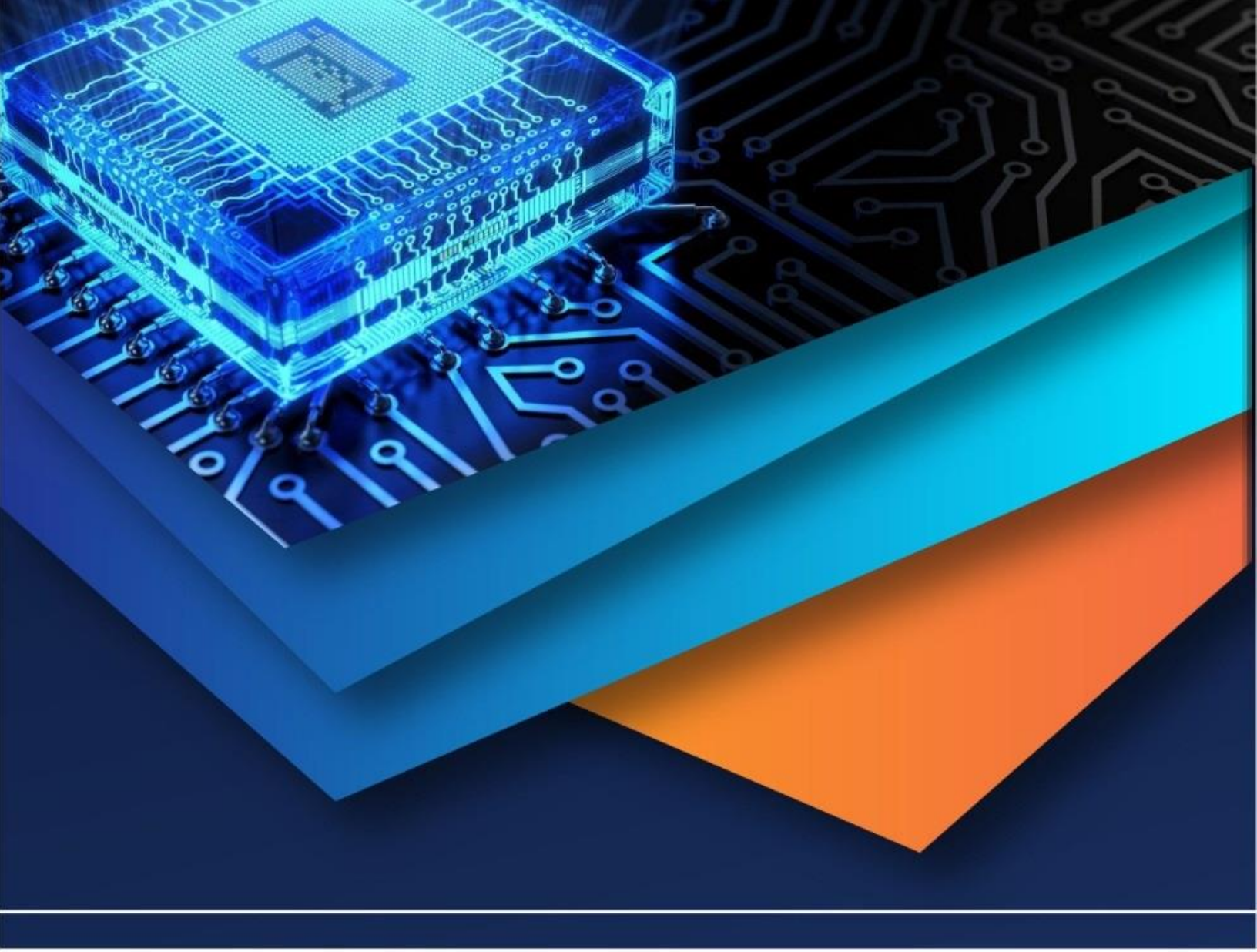

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