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Modeling Heat Transport in Thermal Interface Materials Enhanced with MEMS-based Microinterconnects

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Abstract: ***Thermal management of device-level packaging continues to present many technical challenges in the electronics industry. In a device/heat sink assembly, the highest resistance to heat flow typically comes from the thermal interface material (TIM). The thermal conductivities of TIMs remain in the range of 1–4 W/mK due to the properties and structure of small dispersed solids in polymer matrices. As a result of the rising design power and heat flux at the silicon die, new ways to improve the effective in situ thermal conductivity of interface materials are required. This paper analyzes a unique TIM enhanced with ultrahigh- density wafer-level thin film-compliant interconnects referred to as smart three axis compliant (STAC) interconnects. MEMS technology is used to directly fabricate STAC interconnects onto a silicon wafer and embed them into the TIM to provide an enhanced conductive path between the die/package and the heat sink. Here, results from a theoretical analysis of the thermal conduction in a TIM embedded with STAC interconnects are reported. The objective of the study is to provide comprehensive design strategies for effective implementation of this type of TIM for specific applications. Parametric studies are performed to ex- amine the thermal resistance of the microinterconnect-enhanced TIM for varying materials, configurations, and geometry of the microinterconnects. A periodic element model of a chip–TIM configuration with top heat sink is used to evaluate the conductive effect of the microinterconnects. In addition, an investigation of the conductive transport in a more complicated chip stack is considered. A 3-D thermal analysis is conducted for a multi- chip stack package with and without through-silicon vias. The numerical results show that the microinterconnects significantly improve the thermal performance of the TIM. Finally, further steps toward achieving a chip-level design optimization and fabrication process using a STAC microinterconnect structured TIM is proposed.***

Keywords: MEMS, numerical modeling, STAC intercon- nect, thermal interface material, thermal management.

I. INTRODUCTION

The Performance requirements of today's multi- function and high-performance electronic devices impose ever-increasing demands on thermal management. The International Electronics Manufacturing Initiative (INEMI) report for 2006 [1] states that the power dissipation at the chip level with 2 cm^2 area is projected to exceed 250 W for high-performance applications in the next few years. Heat flux on the order of 125 W/cm^2 requires new strategies for adequate heat removal.

In a representative device/heat sink configuration, the largest thermal resistance is generally associated with thermal inter- face materials (TIMs). These thin layers play an important role in the overall thermal path from the silicon die to the heat dissipation system, such as an air- or liquid-cooled heat sink. Many commonly used TIMs are heterogeneous mixtures of conducting solids in polymer matrices. These types of TIMs typically have thermal conductivities in the range 1–4 W/mK [2]. A considerable amount of research remains focused on the development of more effective TIM performance [3]. Currently, many new and novel types of TIMs are under investigation, for example, grease, solder, or phase-change materials [4]–[8], and polymer–metal composite [9], [10]. As stated above, conventional TIMs typically consist of a matrix (i.e., polymer, grease, phase-change material, silicone, etc.) with micrometer-sized highly conductive particles to produce a material with low to moderate thermal conductivity. This approach works well when the distances between conduc- tive particles are minimized (i.e., larger particle volume frac- tions). At lower volume fractions, conduction of heat within the lower conductivity matrix material dominates, leading to higher thermal resistance. The use of carbon nanotubes (CNTs) as the conductive material in a TIM, which are reported to have a very large thermal conductivity value (more than 3000 W/mK), has been the focus of recent research [11]–[13]. Highly conductive CNT-based TIMs can only be achieved by properly aligning and placing CNTs in the material matrix, thus providing the lowest heat resistance path through the TIM. However, currently it is hard to control the overall height and orientation of the CNTs that is required for this application. In this paper, a novel TIM enhanced with smart three axis compliant (STAC) interconnects is presented. The STAC interconnect was developed by all [14], [15]. A STAC array consists of highly dense titanium–tungsten

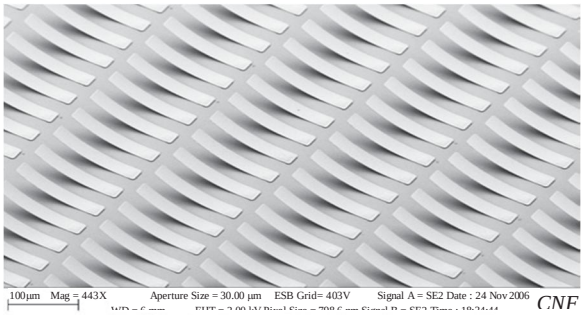

Fig. 1. Highly compliant titanium-tungsten fabricated STAC interconnects. The beam thickness is 0.8 μm and the intrinsic stress range between the two TiW layers is approximately 1.7 GPa. The scale bar shown represents 100 μm.

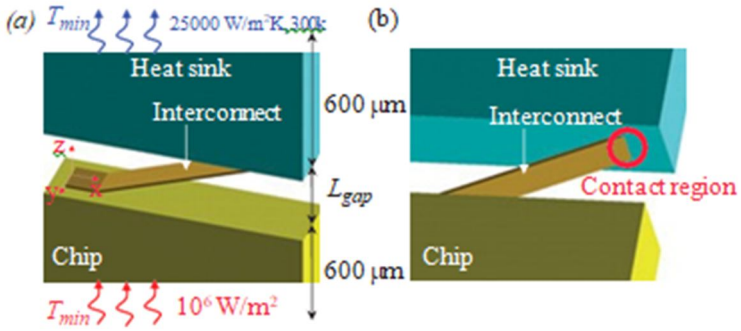

Fig. 2. (a) Configuration of the unit cell and (b) Contact region between the interconnect and the heat sink shown in the rotated view. The heat flux input and the convection boundary condition are loaded on the bottom surface of the chip and the top surface of the heat sink, respectively. *Lgap* is also defined in (a).

(TiW) bi-stressed thin film z-axis interconnects that are directly formed onto copper (Cu) through-silicon vias (TSVs). This approach is novel in that it employs MEMS fabrication technology to provide a well-ordered conductive path by creating dense arrays of microsprings. In theory, the springs will have very good thermal contact with the substrate. In addition, this methodology integrates well with 3-D packaging technology. When utilized with TSV technology, the STAC interconnect arrays yield an effective packaging approach for complex multi-chip stacking configurations. This packaging approach could help minimize the signal transmission path [16], [17] and, as an offshoot, provide for better package thermal performance. Potentially, the integration of MEMS technology into back-end wafer processing provides an eco- nomical manufacturing method.

Fig. 1 shows a successfully fabricated STAC interconnect array. For each STAC interconnect ("spring" or "beam") the total beam length is 150 μm, with 25 μm of its length fixed to the substrate, and the beam width is 25 μm. For this array, each interconnect is spaced 50 μm widthwise and 175 μm lengthwise, bringing the total number of STAC interconnects on a 1-cm^2 chip to 11 200. The total number of I/O exceeds the long-term requirement of the International Technology Roadmap for Semiconductors (ITRS) [18]. Since these interconnects were defined with photolithography and dry-etch chemistry, the same individual spring shown in Fig. 1 can potentially be spaced at a 30 μm (laterally) by 155 μm (longitudinally) pitch with a new mask, bringing the total number of compliant interconnects on a 1 cm^2 chip to beyond 21 000. Detailed fabrication and characterization of STAC interconnects can be found in [19].

To evaluate the thermal characteristics of the STAC inter- connect array, a periodic element model of a chip with top heat spreader (heat sink) is developed. Using numerical and ana- lytical modeling, maximum temperatures, thermal resistances, and interfacial resistance behavior are predicted for different geometries and materials properties. In addition, to investigate the thermal management in a chip stack, a 3-D thermal analysis is conducted on a two-stack package with and without TSV. This thermal analysis of a TIM comprised of STAC interconnects is the first step in assessing the effectiveness and feasibility of this new type of TIM design.

II. THERMAL ANALYSIS

Here, the numerical modeling of a thermal interface material enhanced with STAC interconnects is comprised of three parts. The first part of the analysis consists of a parametric study to evaluate the thermal conductivity of the interconnect- enhanced TIM for a chip–TIM–heat sink configuration, for varying materials and geometries of the interconnects. A 3-D unit element for this configuration was devised and is used to assess the effectiveness of an interconnect array due to essentially 1-D conduction. In the second part, an investigation of the conductive transport in a more complicated chip stack is performed. A 3-D thermal analysis is conducted for a multichip stack package with and without TSVs. The third part of the paper considers the influence of nonideal contact between an interconnect and the heat sink. The 3-D conduction computations were performed using the commercial finite element software package ANSYS [20].

A. Basic Unit Cell Analysis

For the first part of the computational study, a unit, pe- riodic element model is used to analyze the conduction heat transfer from a power dissipating device through an individual interconnect (with either insulated sides or surrounded by a polymer matrix) and out through a heat spreader. The unit cell model geometry is shown in Fig. 2. The width and height of the heat sink and device remain fixed and were chosen to be 50 and 600 μm, respectively. The 25 μm wide beam is centered across the 50 μm width of the cell. The length of the individual interconnect beam determines the global interconnect density. Since the STAC interconnect is stress-engineered, the lift height or the intrinsic stress can be controlled during the deposition process. The parameter L_{gap} represents the distance between the heat sink and the device (silicon). Here, the gap heights 50 and 90 μm are considered based on two different interconnect lift heights. The beam length and the gap height determine the overall length of the unit cell.

In the model, the curvature of the interconnect is neglected. Some assumptions must be made concerning the contact area between the top of the interconnect and the bottom of the heat sink. In an actual device the contact area is dependent upon the curvature and the contact pressure of the interconnect. For the computational model, it is assumed that the beam contacts the heat sink with the cross-sectional area of the beam corresponding to the beam thickness and the angle the beam makes with the heat sink surface (i.e., it depends on beam length and gap height). For the first part of the analysis, perfect contact between the beam and surface is assumed and three different unit cell configurations are compared and discussed. The first case models a unit cell in which only a STAC interconnect is included to form a thermal conductive path between heat sink and silicon, as shown in Fig. 2. The second case corresponds to a conventional TIM, wherein the unit cell system consists of a heat sink, a layer of solid material (polymer) with the same thickness as the gap height (with no interconnect), and a silicon chip. The second case models the performance of a conventional TIM. The third case consists of the STAC interconnect surrounded by the polymer matrix material used in the second case to produce a low resistance path through the interface material. For the numerical modeling work, the 3-D steady-state heat conduction equation [21] is solved in order to determine the temperature T in the unit cell configuration. In Cartesian coordinates the steady-state conduction equation, neglecting volumetric generation, is written as follows:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)=0. \qquad (1)$$

Here k is the thermal conductivity of the material (in SI units W/mK). The above form is general in that it allows for variable thermal conductivity. For the work presented here, only constant conductivity values are considered.

The boundary conditions applied on the unit cell are as follows. A uniform, constant heat flux q_d (W/m^2) is applied at the lower boundary to simulate the power dissipation. For the coordinate system definition used here (shown in Fig. 2), this boundary condition is written as

$$k_z\frac{\partial T}{\partial z}=-q_d \qquad (2)$$

where h is the convective heat transfer coefficient. The thermal conductivity of aluminum is assumed for the heat sink (k_{hs}). All the remaining exposed surfaces on the unit cell model are taken to be adiabatic. The model dimensions and thermal conductivity values used for the computations are listed in Table I. Different thermal conductivities of the STAC interconnects and the polymer matrix are considered. In all the simulations, the heat flux input at the bottom is q_d = 100 W/cm^2, except where specified, and the convective coefficient h is set to be 25000 W/m^{2}K, representing a highly effective liquid-cooled heat sink. The ambient temperature T_a is taken as 300 K.

TABLE I
DIMENSIONS (μm) AND CONDUCTIVITY VALUES (W/mK)

Parameter	Chip	STAC Interconnect	Polymer	Heat sink
Length (L)	10^4	100, 125 150, 175	10^4	— —
Width (W)	10^4	25	10^4	—
Thickness (t)	50 or 600	2 or 5	50 or 90	600
Conductivity (k)	148	200 or 398	1 or 3	235

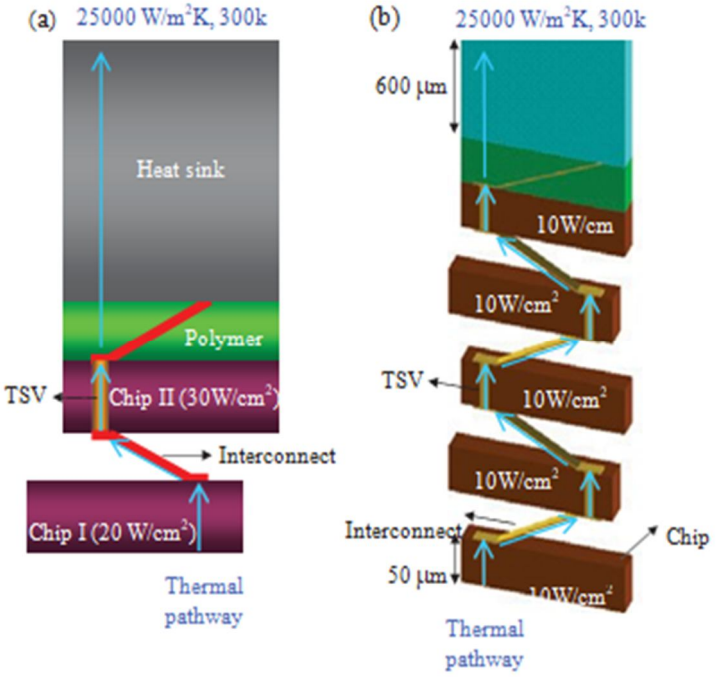

Fig. 3. (a) Two-chip stack unit cell and (b) Five-chip stack. The blue arrow shows the thermal pathway. In the unit cell model shown in (a), two chips with nonuniform power and the top heat sink are connected by two STAC interconnects. The embedded Cu-filled TSV connects two STAC interconnects. Polymer is injected into the space between Chip II and the top heat sink. The model in (b) shows the five-chip application with uniform power. Four Cu-filled TSVs are utilized along the thermal pathway.

B. Multi-Chip Stack Modeling

The stacking of multiple chips offers several advantages as a packaging methodology. Essential to 3-D packaging is the use of TSV technology. A two-chip stack unit cell model is shown in Fig. 3(a), which incorporates two 50-μm-thick device layers. Each chip in this stack is modeled with different power dissipation. For simplicity, power input is applied at the bottom of each layer representing a device. The device referred to as Chip I is represented by a heat flux of 20 W/cm^2, while the heat flux for Chip II is 30 W/cm^2. Chip II has a 10-μm- diameter Cu-filled TSV to facilitate z-direction heat flow from Chip I to the STAC interconnect-enhanced TIM. Two modeled

STAC interconnect beams anchor to the exposed Cu column. Again, a convective heat transfer coefficient of 25 000 W/m^{2}K is assumed at the top of the heat sink. The STAC interconnect is assumed to have the thermal conductivity of copper in this case.

For the five-chip stack model considered in this paper [see Fig. 3(b)], each device is assumed to input a heat flux of 10 W/cm^2 and the same top heat sink condition as used in the previous cases is imposed. For all but the lowest die, a 10-μm- diameter Cu-filled TSV lies beneath each STAC interconnect. For this model, the STAC interconnect has the dimensions of 150 μm X 25 μm X 2 μm. For the TIM between the top most die and the heat sink, a polymer matrix surrounding a STAC interconnect is used.

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C. Interface Resistance Model

In practice, the pressure distribution and the lift height of interconnects may not be controlled precisely, so that some released interconnects may not have ideal contact with the bottom surface of the heat sink. Hence it is important to analyze the effect of a gap at the interconnect–heat sink interface. To represent this effect a contact conductance (or resistance) between the interconnect and the heat sink can be introduced as follows:

$$q = h_c O T_g \qquad (4)$$

where q is the heat flux, h_c is the thermal contact conductance for the small gap between the end of the interconnect and the heat sink, and OT_g is the temperature jump across this small gap. In this type of model, if the temperature jump is zero (i.e., no contact resistance), then the contact conductance is infinite in order to maintain a finite heat flux. For the present application, the conductance of the interconnect tip gap can be defined in the following manner as a function of the gap height δ_g

$$h_c = \frac{k_g}{\delta_g} \qquad (5)$$

where k_g is the thermal conductivity of the gap (1 W/mK is assumed).

Here the influence of varied contact conductance on the thermal performance of the interconnect enhanced TIM is investigated. For this part of the study, the interconnect di- mension is set to 150 μm X 25 μm X 2 μm. In addition to investigating the effect of an interconnect gap alone, results are presented including a matrix material as well with thermal conductivity equal to 3 W/mK.

Once the effect of nonideal contact is established, a final case is considered to better understand the effect of change in beam curvature due to applied pressure during heat sink assembly on the overall thermal performance of the TIM enhanced with STAC interconnects. For this case, the inter- connect dimension considered is 150 μm X 25 μm X 5 μm, and the interconnect thermal conductivity is set to 398 W/mK. For model simplification purposes, the beam curvature vari- ation is represented by the change in beam lift height. The overall beam lift height variation considered in this analysis is between 50 and 90 μm. Furthermore, for the computations, ideal contact between the beam and the heat sink is assumed.

III. RESULTS AND DISCUSSION

Following the organization of the previous section, the computational results will be presented in three mains parts:

The thermal characterization of the interconnect alone, for varying materials and geometries of the interconnect. B) Mod- eling results for the 3-D thermal analysis of a multichip stack package with and without TSVs. C) Results corresponding to the influence of nonideal contact between an interconnect and the heat sink.

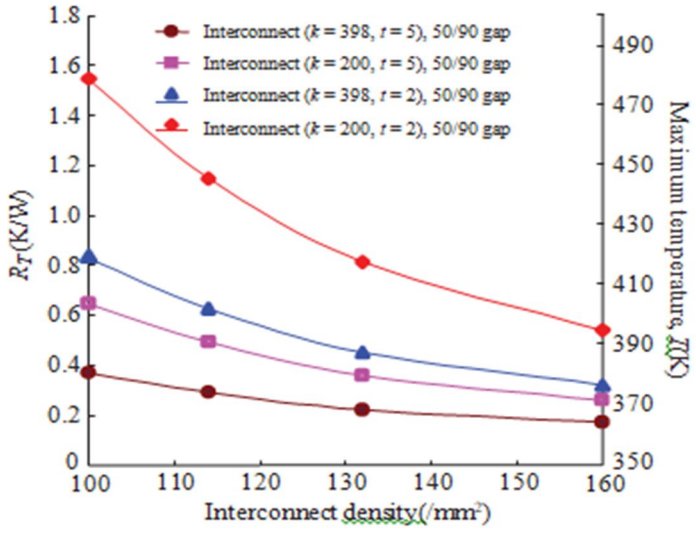

Fig. 4. Thermal performance results under various interconnect densities (/mm^2), thermal conductivity (k, W/mK) and thickness (t , μm). The gap height is defined as the distance between the top surface of the chip and the bottom surface of the heat sink.

A. Chip-TIM With Top Heat Sink

Simulation results are presented for the performance of the microinterconnect array-based TIM. For the microinter- connects three design parameters, i.e., the geometry of each interconnect, the thermal conductivity, and the gap height, are investigated. Both conduction through the interconnects alone and conduction through the interconnects surrounded by a polymer matrix are considered.

1) *Interconnect Configuration:* Table I summarizes the four different interconnect sizes, two different interconnect thick- nesses, and two different interconnect thermal conductivity values used to determine the thermal performance of the STAC interconnect via the unit cell configuration. Starting from a simple thermal resistance analog calculation, it is straightforward to show that most of the temperature drop in the overall configuration results from the TIM. A convenient way to compare the thermal performance for the various cases is to define a thermal resistance between the location of the power source and the top of the heat sink where the minimum temperature is attained. Here, the total chip-to-heat sink resistance is defined as

$$R_T = \frac{T_{\max} - T_{\min}}{P} \qquad (6)$$

where $T_{\max}$ is the maximum temperature at the bottom of the chip, $T_{\min}$ is the minimum temperature at the top surface of the heat sink, and P is the power dissipation of the chip represented by the applied constant heat flux.

The conduction computations are performed for the unit cell, but the results are interpreted for a 1-cm^2 region. Intercon- nect density is studied from 100 to 160/mm^2, corresponding to a single interconnect length ranging from 175 to 100/mm^2. The density of 160/mm^2 corresponds to interconnects with the minimum length (i.e., 100 μm). Two gap heights L_{gap} are investigated: 50 and 90 μm, as defined in Fig. 2(a). Note that the shortest interconnect length cannot be used with the larger gap height. Fig. 4 is a plot of the total resistance versus the interconnect density (maximum absolute temperature values are presented as well). It is found that by increasing the interconnect density from 100 to 160/mm^2, the global thermal resistance decreases in all four cases considered: two differ- ent beam thicknesses and two different thermal conductivity values for the interconnects. With only the interconnects for conduction across the gap, the results do not depend on the gap height L_{gap}.

The lower thermal conductivity value corresponds to TiW, while the higher value represents Cu. For the 100 μm intercon- nect length (160/mm^2 density) with low thermal conductivity (200 W/mK) and small thickness (2 μm) the total resistance is about 0.6 K/W. This value corresponds to a configuration close to the best that has been fabricated to date. The results indicate the extent to which better performance can be obtained for a thicker interconnect with higher thermal conductivity. For example, an interconnect of 5 μm thickness and 398 W/Mk reduces the total resistance significantly. However, for the interconnect with same thermal conductivity, the thickness of the interconnect does not significantly reduce the overall chip-to-heat sink resistance (or maximum temperature) as the interconnect density increases, i.e., the thickness of the interconnect plays an important role only at lower densities. Similar to the thickness of the material, as the density of the interconnect increases, the thermal conductivity of the interconnect material does not play a significant role in reduc- ing the overall chip-to-heat sink resistance. Another important observation is that for a thick (5 μm) and high thermally conductive interconnect increasing the interconnect density does not play a significant role in reducing the overall chip- to-heat sink resistance (or maximum temperature). Thicker interconnects can be realized by selectively electroplating Cu to the TiW-based STAC interconnect, since TiW films can be fabricated with a smaller thickness (approx. 200–400 nm) than Cu. For simplification in the numerical model, the conductivity of Cu alone is used to obtain an estimate of the best case performance. Overall, the data presented in Fig. 4 summarizes the impact of the various design factors.

2) *Polymer Matrix:* The thermal conductivity of polymer- based TIMs is typically in the range of 1–4 W/mK. In practice it is more likely that the interconnect array would be encapsulated with a polymer matrix. In this part of the study, the thermal performance with the addition of a polymer matrix around the interconnects is investigated. The conductivity values 1 and 3 W/mK are used. With a filled gap, the gap height now impacts the results, so calculations are presented for both 50 and 90 μm gap height. The maximum temperature rise (or thermal resistance) can be determined analytically for a polymer-filled gap in the unit cell (the analytical values were used to verify the computational model as well). For a purely polymer-filled TIM, the maximum temperature rise of the system for a 50-μm-thick gap is 57 K with a 1 W/mK conductivity, and 23 K for a 3 W/mK conductivity. For 1 and 3 W/mK conductivity values, the corresponding thermal resistances are 0.57 and 0.23 K/W, respectively. For a 90 μm gap, the temperature rise is 97 K for 1 W/mK and 36 K for 3 W/mK, with corresponding thermal resistance values of 0.97 and 0.36 K/W, respectively. These values serve as reference points for comparison with the results for a TIM consisting of a polymer matrix and a STAC interconnect array.

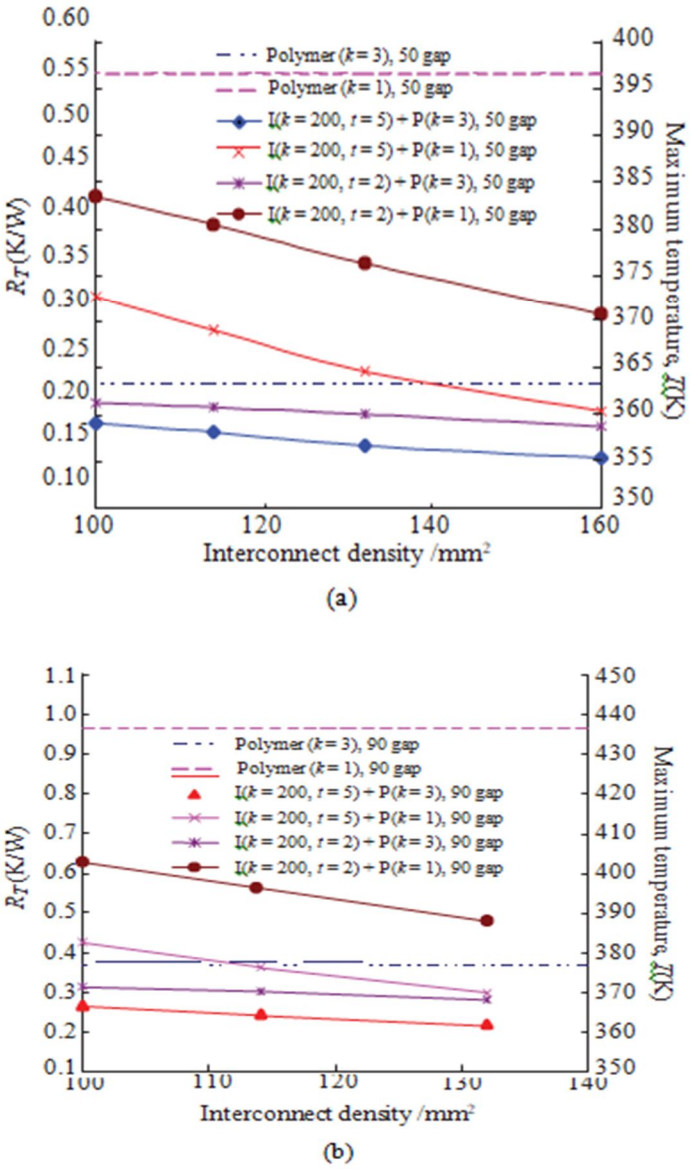

Fig. 5. Total thermal resistance and maximum temperature versus intercon- nect density for interconnect conductivity of 200 W/mK: (a) 50 μm TIM gap height; (b) 90 μm TIM gap height. I refers to interconnect, P refers to the polymer matrix. The gap height is defined as the distance between the top surface of the chip and the bottom surface of the heat sink.

3) *Polymer/STAC Interconnect Configuration:* While the interconnects are made of higher conductivity materials, they have small cross-sectional area. If the interconnects alone are used, then the air surrounding them will result in high thermal resistance values across the gap. In addition, using the interconnects alone may not provide sufficient mechanical support to the heat spreader. Thus, there are benefits for using some type of solid material (typically a polymer) to fill the gap (e.g., structural behavior, moisture barrier, etc). As a result, the thermal performance of the interconnects with the gap region filled by a polymer matrix was investigated. Figs. 5 and 6 show the computed results in terms of total thermal resistance (and maximum temperature) as a function of interconnect density for the various configurations described previously. The values for the purely polymer-filled gap are shown by the marked horizontal lines. The modeling results indicate that the presence of the interconnects can have a significant impact on the thermal performance. The figures show the effect of the interconnect dimensions and conductivity values. A summary of the results is presented in Table II, where the reduction in thermal resistance for the range of cases is summarized.

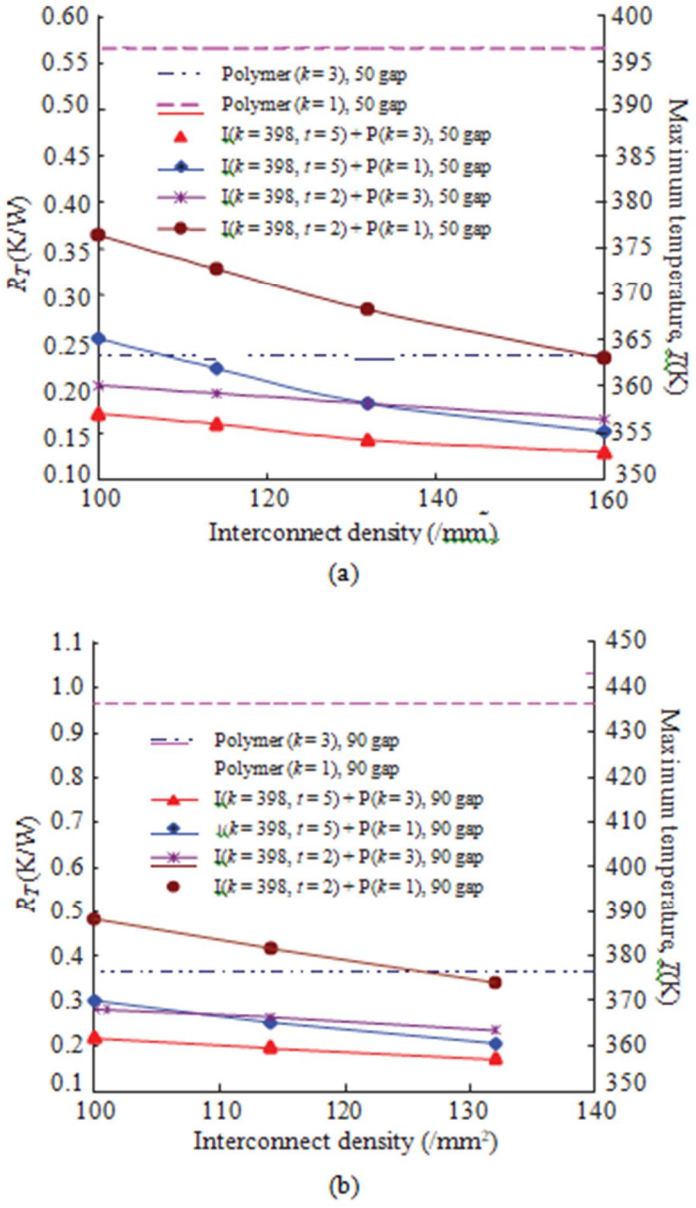

Fig. 6. Total thermal resistance and maximum temperature versus intercon- nect density for interconnect conductivity of 398 W/mK: (a) 50 μm TIM gap height; (b) 90 μm TIM gap height. I refers to interconnect, P refers to the polymer matrix. The gap height is defined as the distance between the top surface of the chip and the bottom surface of the heat sink.

4) *Multi-Chip Stack With TSV:* The periodic element for the two-chip stack described previously and shown in Fig. 3(a) was also analyzed using a 3-D finite element computational model. Fig. 7 shows the temperature profile along the length of the structure. Results are presented for the cases with the high and low conductivity values for the interconnect and the matrix material. Also included is the curve corresponding to the lower interconnect conductivity and higher matrix conductivity. For this model configuration, a heat flux corresponding to 20-W dissipation is specified at the bottom of chip I and an additional heat flux corresponding to 30-W dissipation is added for chip II. The higher thermal conductivity combination results in a significantly lower temperature for the lower silicon region (I). Between regions I and II, the interconnect is the only conductive path. In the second silicon region (II), the effect of the Cu column on the temperature is relatively small if the higher conductivity matrix material surrounds the interconnect in the gap.

TABLE II
PERCENTAGE REDUCTION IN THERMAL RESISTANCE FOR THE POLYMER/INTERCONNECT CONFIGURATION COMPARED TO THE POLYMER ALONE. LENGTH, THICKNESS AND AP HEIGHT (L_{gap}) ARE IN μm; THERMAL CONDUCTIVITY (k) IS IN W/mK

Interconnect Length 150 Thickness 2	P (k = 1) I (k = 398, t = 2) versus P (k = 1)	P (k = 3) I (k = 398, t = 2) versus P (k = 3)
L_{gap} = 50 L_{gap} = 90	42% 56%	17% 28%
Interconnect Length 100 Thickness 2	P (k = 1) I (k = 398, t = 2) versus P (k = 1)	P (k = 3) I (k = 398, t = 2) versus P (k = 3)
L_{gap} = 50 L_{gap} = 90	60% 65%	30% 33%

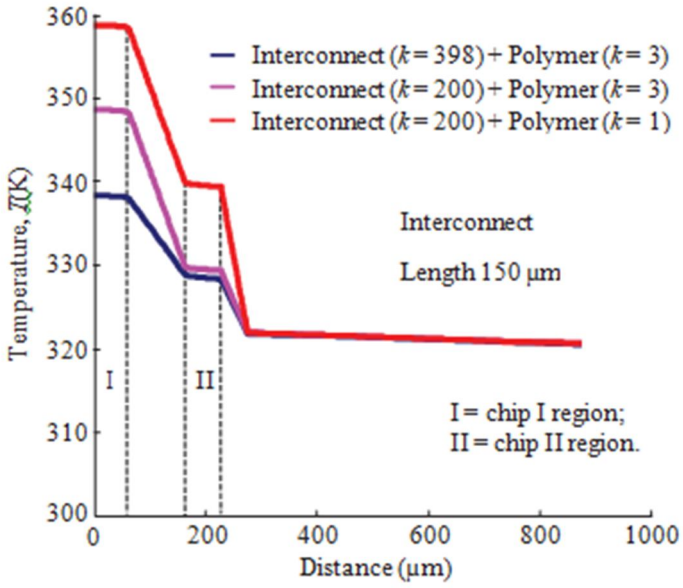

Fig. 7. Overall temperature profile as a function of thermal pathway for the two-chip stack model [see Fig. 3(a)] for three combinations of conductivity. I = first chip region; II = upper chip region.

In Fig. 8, the heat flux along the length of the unit cell with and without the Cu column is plotted. At the bottom STAC interconnect after region I, there is a sudden jump in the heat flux due to the cross-sectional area change. The interesting result is that along the Cu column in the second device (II) a higher nonuniform heat flux is obtained.

To explore the benefit of the thermal path provided by the interconnects, a five-chip stack package is modeled. The dimensions of the devices comprising the stack, the STAC interconnects, and the Cu TSV are the same as in the previous two-chip stack. For the highest conductivity values, i.e., higher thermal conductivity for the matrix and the higher value for the interconnects, the maximum temperature is approximately 60 K lower than the low conductivity case, as shown in Fig. 9. Keeping the thermal conductivity of the polymer fixed at the higher value while changing the thermal conductivity of the microinterconnect from 398 to 200 W/mK leads to a 50 K higher maximum temperature. However, by keeping the ther- mal conductivity of the interconnect fixed while changing the thermal conductivity of the polymer has a much smaller impact on the maximum temperature. These results clearly show the effect of the conduction path provided by the interconnects.

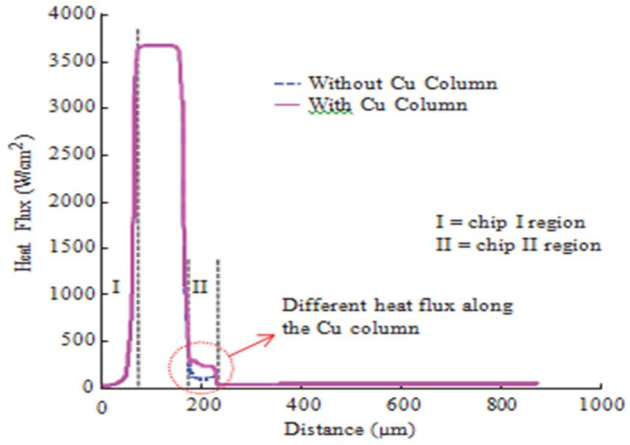

Fig. 8. Heat flux as a function of thermal pathway for the two-chip stack model shown in Fig. 3(a). I = first chip region; II = upper chip region. For these results, the thermal conductivity of polymer matrix is 3 W/mK.

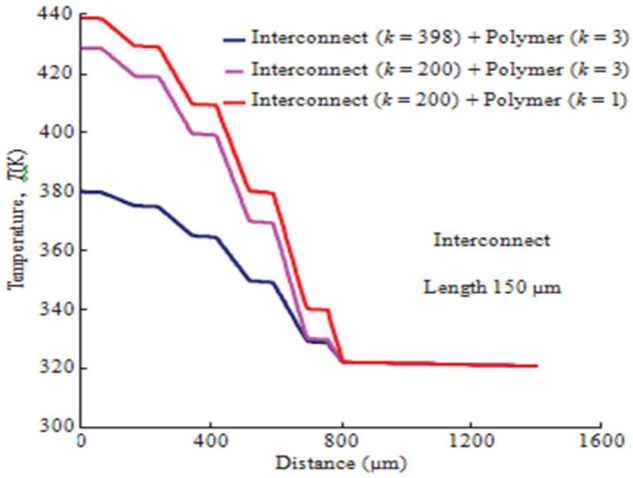

Fig. 9. Overall temperature profile as a function of thermal pathway for the five-chip stack [see Fig. 3(b)] for three different conductivity combinations.

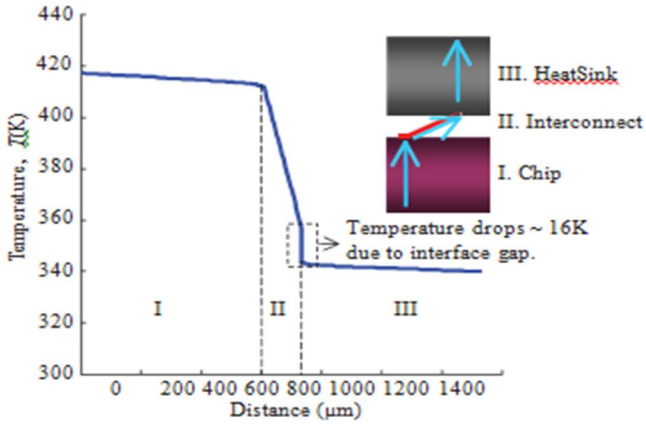

Fig. 10. Temperature as a function of length for the interconnect interface gap model, with δg 0.2 μm, which is located at the interface between the interconnect tip and the bottom of the heat sink. The figure shows the large temperature drop when the gap is present. The total length and thickness of the interconnect used here are 150 and 2 μm, respectively. I = chip region; II = interconnect region; III = heat sink region. No polymer is involved in this model.

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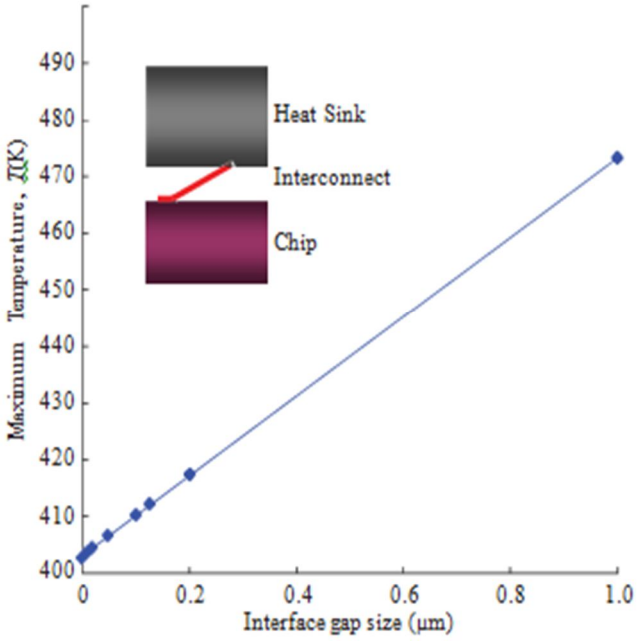

Fig. 11. Maximum temperature as a function of the interface gap (δg) between the interconnect tip and bottom of heat sink. The total length and thickness of the interconnect used here are 150 and 2 μm, respectively. No polymer is involved in this model.

B. Interface Resistance Model

To study the effect of the contact between the intercon- nect and the heat spreader, a common modeling approach (described in Section II-C) is used to account for an interface resistance at the end of the interconnect in the unit cell. For the results presented here, the gap conductance h_c is varied from 10^6 to 10^{15} W/m^2 K (corresponding to gaps from 1μm to essentially 0). The temperature profile is used to assess the effect for an interconnect with dimensions of 150 μm X 25μm X 2μm. The heat flux input and the convective cooling at the top of the heat spreader are the same as the original case considered (Fig. 2). For a single interconnect, Fig. 10 shows the temperature as a function of thermal pathway distance across the model configuration for a 0.2μm interconnect gap.

A significant temperature jump $\sim$ 16 K occurs because of the reduced conductance in the primary heat transfer path. The 0.2μm interface gap causes the maximum temperature in the system to reach 418 K, while the maximum temperature predicted by the ideal contact model is about 400 K as shown in Fig. 4. Therefore, as would be expected, for an interconnect alone the contact condition can be a significant factor affecting the system thermal performance.

Fig. 11 shows the maximum temperature in the unit cell for various interface gap sizes ranging from 0 to 1 μm. As the interface gap size is increased, there is a linear increase in unit cell maximum temperature. The data shown in Fig. 11 suggests that the imperfect contact between the interconnect and the heat sink would be an important consideration if the interconnect is surrounded by air. If a matrix with thermal conductivity 3 W/mK is used to fill the gap, the impact of the interconnect gap is alleviated. Fig. 12 is included as verification that the gap between the interconnect and heat sink does not affect the maximum temperature once the intercon- nect is embedded in a matrix material. In the actual assembly, the contact condition of each interconnect is not identical, i.e., some interconnects may have ideal contact but some may not. The unit cell interface resistance model presented in this section corresponds to the worst case contact condition. The result clearly indicates that the special manufacturing needs to ensure identical lift height for all interconnects in the STAC array can be alleviated by embedding the interconnect in a polymer matrix. In addition to this aspect, encapsulation with a matrix material is beneficial from a structural standpoint and for efficiency in manufacturing.

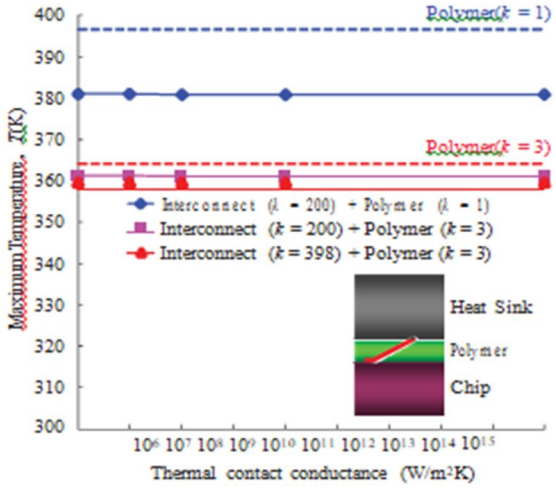

Fig. 12. Maximum temperature as a function of the thermal contact conductance (*hc)* between interconnect tip and bottom of heat sink. Polymer is involved between the chip and the top heat sink. *hc* is varied from 10^6 to 10^{15} W/m^2 K corresponding to gaps from 1 μm to essentially 0. The total length and thickness of the interconnect used here are 150 and 2 μm, respectively.

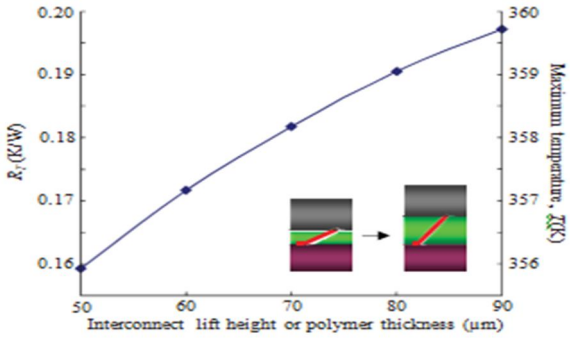

Fig. 13. Total thermal resistance and maximum temperature versus poly- mer thickness ranging from 50 to 90 μm for interconnect conductivity of 398 W/mK, length of 150 μm, and thickness of 5 μm; the ideal contact is assumed between the interconnect tip and the heat sink bottom.

The effect of interconnect curvature on the thermal per- formance of the system was also addressed. Results for five interconnect lift heights are shown in Fig. 13. The polymer thickness is assumed to be the same as the interconnect lift height, and zero thermal contact resistance is assumed at the interface of the interconnect and the heat sink. As the interconnect lift height decreases, there is a reduction in the overall thermal resistance due to the reduction of the polymer thickness. This translates to a 3.8 K decrease in the maximum temperature when the overall interconnect lift height is varied from 90 to 50 μm. The results clearly indicate that when a heat sink is placed on the TIM, the pressure applied to the interconnects ensures good contact between the TIM and the bottom surface of the heat sink. The change in interconnect curvature due to applied pressure does not hamper the overall thermal performance of the TIM.

IV. CONCLUSION

An extensive thermal analysis of a novel TIM comprised of STAC interconnects was conducted using a finite element com- putational model and 1-D analytical conduction calculations. A unit cell model consisting of a silicon device, TIM, and heat spreader assembly was used to determine the total thermal resistance and the maximum temperature (or temperature rise). In order to analyze the potential of using a STAC array as a TIM, three different cases were investigated. First, heat transfer through the unit cell with the microinterconnect alone acting as the conduction path was analyzed. For the second case, a polymer matrix was added to the TIM region to encapsulate the interconnect. The third case considered the effect of a small gap between the end of the interconnect and the bottom surface of the heat spreader. The computational results show that a TIM comprised of a

microinterconnect array encased in a matrix material can significantly improve the thermal performance over the matrix material alone, when the interconnects have a higher conductivity than the matrix material. STAC interconnects with larger cross-sectional area, higher thermal conductivity, and high array density yield the best thermal performance. By using the highest array density and a matrix with higher conductivity, the STAC interconnect- based TIM can improve the thermal performance up to 33% depending on the gap height (TIM thickness). The thermal modeling presented here provides a guide for the design of a STAC array-based TIM. Performance estimates for a range of design parameters are provided. The impact of a gap between the end of the interconnect and the bottom of the heat spreader was found to be negligible as long as a matrix material is used in combination with the microinterconnect array. Furthermore, it was also found that a change in interconnect curvature due to applied pressure during heat sink assembly does not affect the overall thermal performance of the TIM. Since this technology is well suited for 3-D packaging, two additional multiple-stack configurations were modeled, which include the effect of TSVs. The 3-D package model results show that STAC microinterconnect array-based TIMs may be particularly useful for providing enhanced cooling in hotspot regions. In addition, the STAC interconnects can play a dual role for both electrical and thermal conduction, thus making it a multifunctional interconnect approach for addressing specific application needs at the wafer level.

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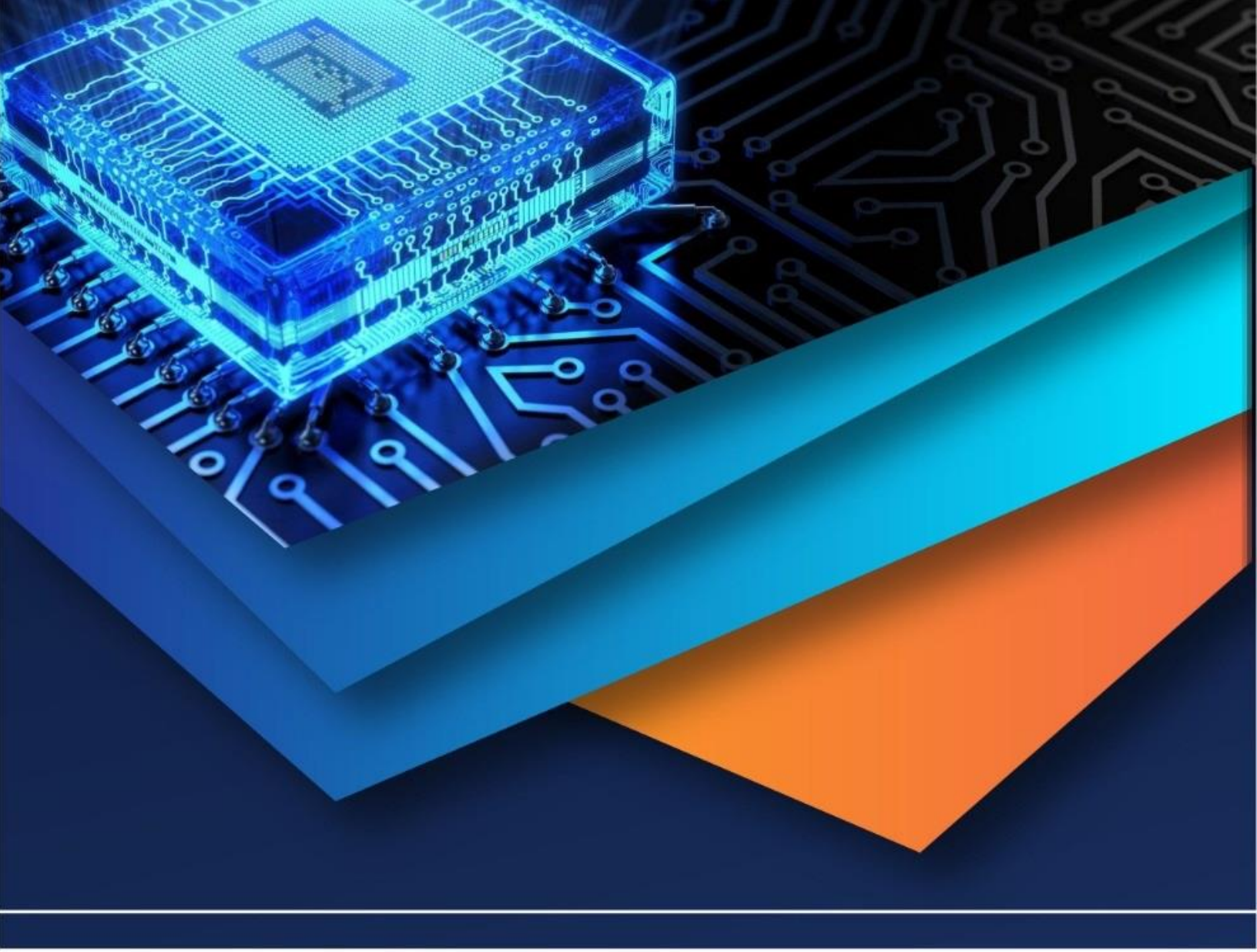

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