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Effect of Scaling on Power Dissipation on Single Phase wide fan-in Domino Logic Circuits

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Abstract: ***In this paper, the performance of CMOS transistor is analyzed on the basis of scaling. The change of device characteristics with decreasing dimensions of transistor is studied under scaling theory. Transistors are scaled for the requirement of high functionality and high density of chips. In this paper, existing circuits are designed and simulated at 180nm, 90nm and 45nm scaling technologies. We have calculated the power dissipation of existing circuits at different scaling technologies for load capacitance of 1fF and clock frequency of 2.4MHz. At 90nm, existing circuits such as sp-domino, cpd, tpod and cpod has reduced power dissipation of 35.13%, 39.84%, 60.13% and 39.38% as scaling technology changes from 180nm to 90nm, and from 90nm to 45nm reduction in power dissipation is 61.21%, 75.83% for cpd and cpod circuits respectively.***
Keywords: Domino logic, Scaling, Power dissipation, Precharge pulse

I. INTRODUCTION

Domino logics are used for implementing high speed logic designs. They have an advantage of faster transition and glitch free operation. Domino logics circuits are CMOS based design techniques which consists of a clocked PMOS pull up transistor, a clocked NMOS footer transistor and the pull down NMOS network. They have several applications such as memory[1], multiplexers, comparators, adder[2] etc. They are also used in microprocessors[3]. The speed is enhanced as they reduces output load capacitance and requires less area. It uses dual phase such as (i) precharge, (ii) evaluate[4]. Domino circuits have disadvantage of high power consumption, clock loading, incapable to implement inverting functions also charge leakage and charge sharing reduces noise margin. However, by adding keeper transistor charge leakage and charge sharing can be reduced to certain level. Due to unwanted redundant switching, domino logic circuit consumes more power at dynamic and output node [5].

Scaling of a MOS transistor means reducing the dimensions of the device[6]. Thus scaling increases functional capacity of the chip and device density. Scaling is done in such a way that the performance of device is not affected. Switching power dissipation and switching time of output is reduced due to reduced capacitance and capacitance is reduced due to the scaling.

Parameter	Symbol	Constant voltage scaling	Constant field scaling
Voltage	V	1	$1/S$
Current	I	S	$1/S$
Field	ε	S	1
Gate Length	L	$1/S$	$1/S$
Gate Width	W	$1/S$	$1/S$
Oxide Capacitance	C_{ox}	S	S
Gate Capacitance	C_G	$1/S$	$1/S$
Substrate Doping	N_a	S^2	S^2
Oxide Thickness	t_{ox}	$1/S$	$1/S$
Power	P	S	$1/S^2$
Power delay product	$P\Delta t$	$1/S$	$1/S^3$
Transit Frequency	t_f	S^2	S
Transit Time	t_r	$1/S^2$	$1/S^2$

Table1. Effect of scaling on parameters

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However, scaling is not restricted to only reducing the gate length and width but also other dimensions such as- gate/drain and gate/source alignment, depletion layer widths and oxide thickness.

Two different types of scaling are there:-(i)constant voltage scaling, (ii)constant field scaling. Both the types have their own effect on the device performance. For high switching speed applications, constant voltage scaling is preferred while constant field scaling is preferred for low power application. Depending upon the application, both the methods can be used accordingly[7]. Table1 shows effects of scaling on various parameters.

Disadvantages of scaling are:-with the reduction in scaling the electrical properties of MOS changes, difficulty in the fabrication process, maintaining of proper threshold voltage so as to maintain sub-threshold leakage power dissipation.

II. PREVIOUS WORK

A. Single- Phase SP-Domino Logic

SP-domino employs delayed clock for precharge and evaluation[8]. It uses single phase for both pull up and pull down network. Figure1 shows the circuit diagram of sp-domino Evaluation phase uses single phase for pull-up and pull-down. When M1 and M8 are ON, small contention current flows for pulse P.

If M8 is OFF, dynamic node is charged to high voltage. If dynamic node is at low value for M7 remains OFF, at the end of pulse P, pulse P is pulled up by M4 in that case[9].

The mathematical expression for P is

$$P=\overline{CLK_i.CLK_j + DYN}$$

where DYN is dynamic node and CLKi and CLKj are clock delayed and its delayed inverse.

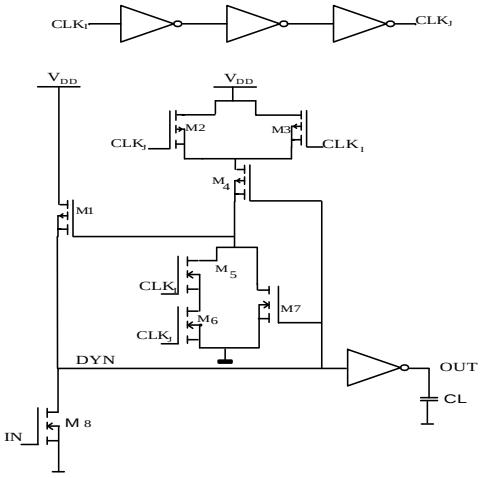

Figure1. single phase domino circuit

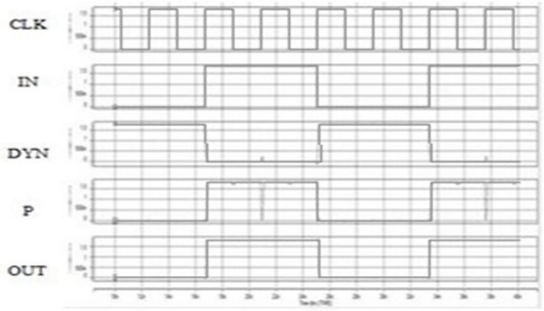

Figure2.voltage characteristics of sp-domino

SP-domino uses M1 as both pull-up and keeper. Size of M1 has to be carefully chosen as increased keeper ratio increase delays and contention current so the circuit lacks flexibility. Figure2 shows the voltage characteristics of circuits.

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B. Conditional Precharge Dynamic Buffer Circuit

Conditional precharge dynamic circuit uses M3 as keeper transistor and both M1 and M2 as pull up network. Figure3 shows the circuit diagram of cpd. At the start of each clock dynamic node is conditionally charged to high voltage when M6 is turned OFF and pull-up network is turned ON for short duration Td. This allows propagation of precharge pulse at dynamic node and stops the precharge pulse at the output node[10]. Figure4 shows voltage characteristics.

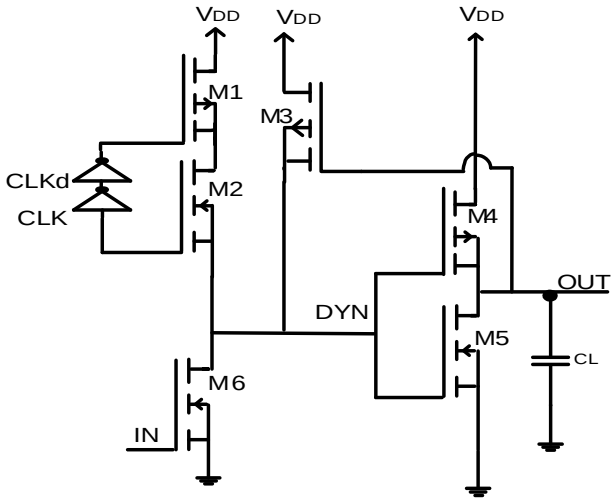

Figure3. Circuit diagram of conditional precharge dynamic circuit.

C. Trigger Pulse Operated Domino

TPOD is a simple footless domino operated by periodic trigger pulse. M1 works as pull-up transistor and is controlled by trigger pulse generator. Transistor M2 is used as keeper.

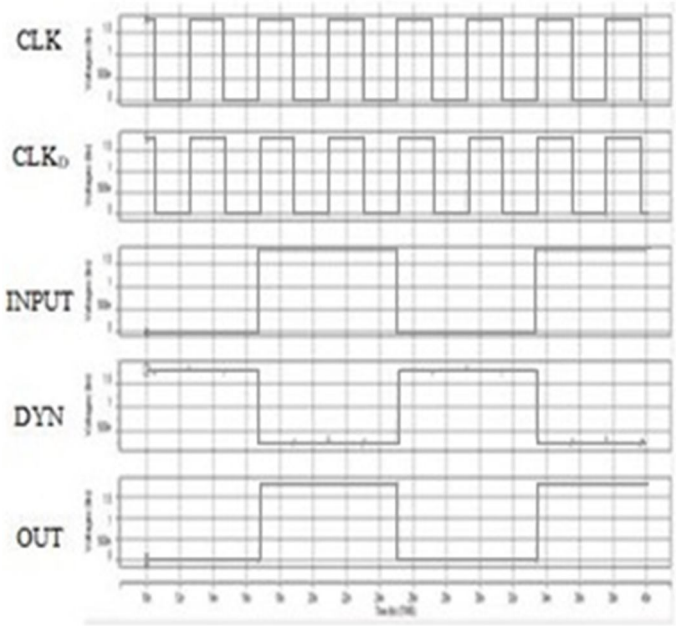

Figure4.Voltage characteristics of circuit

Mathematical expression for trigger pulse is

$$T=\overline{CLK.CLK_D}$$

where CLK and CLK_D are clock and its clock delayed inverse. Figure5and figure6 shows circuit diagram and voltage characteristics. TPG's main function is to generate low trigger pulse T for short duration at start of rising edge of clock. At dynamic node, this circuit allows propagation of precharge pulse and stops the propagation of precharge pulse at the output node[11].

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D. Control Pulse Operated Domino

Control pulse operated domino is a footless circuit with static characteristic. Figure7 shows circuit diagram. Here M6 and M7 are used as pull up and keeper to control independent rising and falling delays. M6 is controlled by control pulse P which always remains high except for short duration.

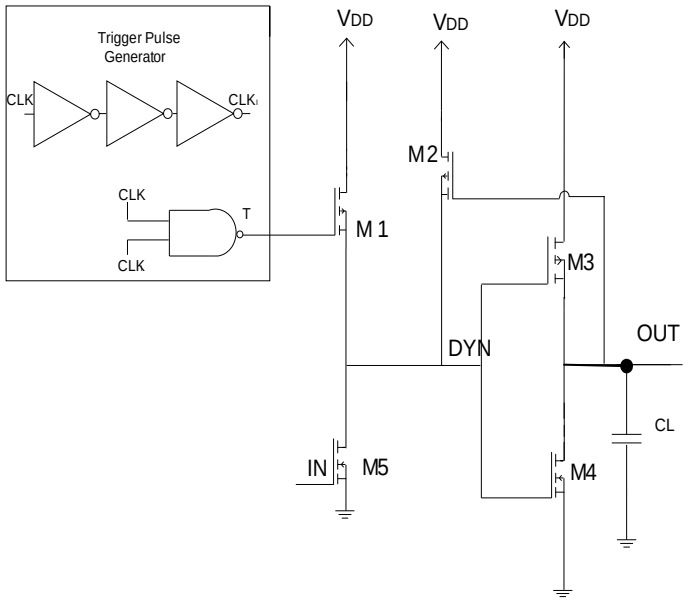

Figure5.Circuit diagram of TPOD

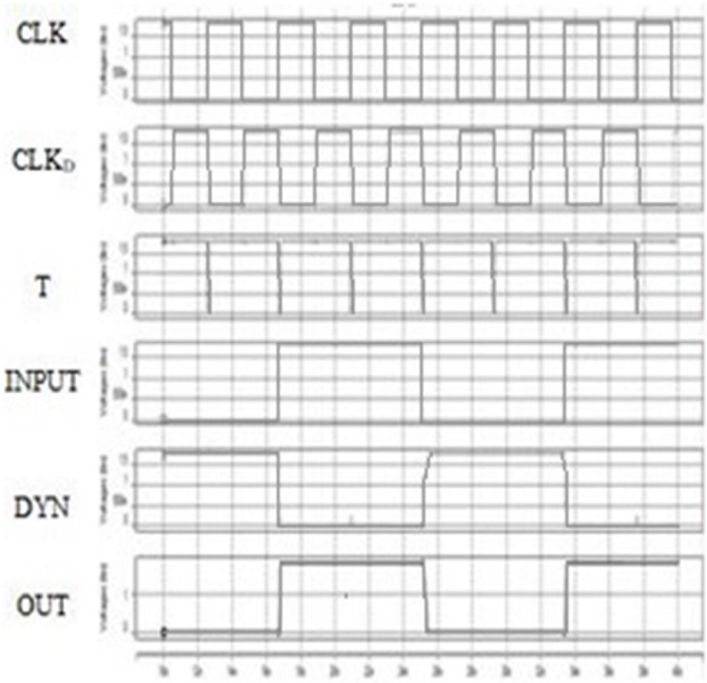

Figure6. Voltage characteristics of TPOD circuit.

Control Pulse Generator has clock pulse CLK, delayed inverse clock CLK_i and feedback from output node. CPG is basically a NAND gate and M5 is connected at the foot of NAND gate and output is connected as input to its gate[12]. Figure8 shows voltage characteristics of cpod circuit. CPOD uses different transistors for pull-up and keeper transistor which provide flexibility to the circuit.

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III. SCALING EFFECT

A. Scaling effect on Single Phase SP-Domino Logic

Scaling means reducing the dimension of the device which increases device density and functional capacity of the device. In proposed algorithm, scaling reduces capacitance and power supply voltage and provides lowering power consumption of MOSFET.

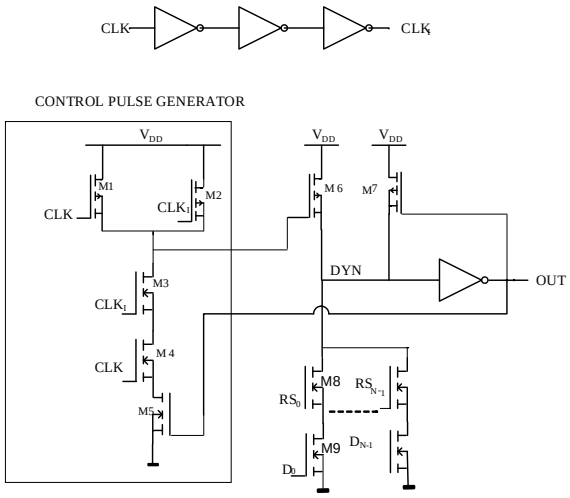

Figure7. Circuit diagram of CPOD

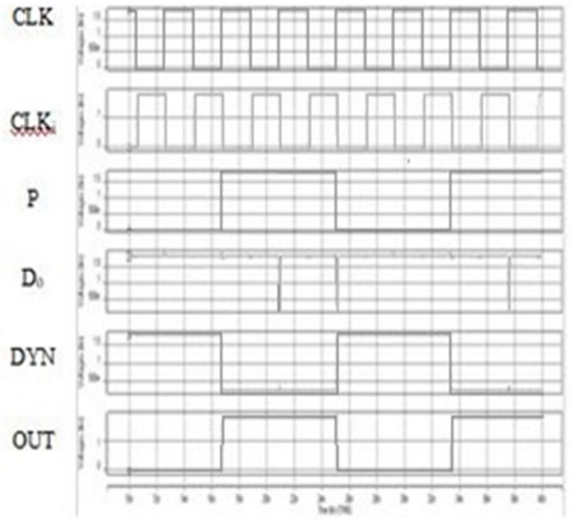

Figure8.Voltage characteristics of circuit

If we increase the frequency of MOSFET the power consumption of MOSFET increases and therefore the power dissipation of the circuit increases.

In Effect of Scaling on Power Dissipation proposed algorithm, we have reduced the dimension of the transistor at various scaling. In proposed algorithm, three scaling dimension is considered which are 180nm, 90nm and 45nm.

In proposed algorithm, the frequency considered is 2.4MHz and load capacitance is 1fF. The power dissipation of the circuit is calculated against each scaling.

B. Scaling effect on Conditional Precharged

1) *Dynamic Buffer:* Dynamic Precharge buffer reduces frequent switching at dynamic node and output node. This circuit saves power consumption by propagating precharge pulse at dynamic node and stopping precharge pulse at output node. The conditional precharge dynamic buffer circuit is scaled at three scaling dimensions- 180nm, 90nm and 45nm.The power dissipation of each scaling is calculated and compared.

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C. Scaling effect on Trigger Pulse Operated Domino

Trigger pulse operated domino uses periodic trigger pulse in place of clock pulse. This circuit reduces frequent switching at dynamic and output node and thus reduces power consumption.

The trigger pulse operated domino circuit is scaled at three dimensions which are 180nm, 90nm and 45nm. The power dissipation is then calculated and compared for each scaling.

D. Scaling effect on Control Pulse Operated Domino

In control pulse operated domino power consumption is reduced because of reduced switching activity. This circuit uses modified size of pull-up transistor as small size of pull-up will degrade circuit performance and increase in size of pull-up transistor will increase power consumption. Thus power consumption of control pulse operated domino is than other circuits.

Control pulse operated domino is scaled at three scaling dimensions-180nm, 90nm and 45nm. The power dissipation is calculate and compared for each scaling.

IV. SIMULATION RESULT

Comparison of power dissipation of various circuits with clock frequency 2.4MHz and load capacitance 1fF with varied scaling is shown in fig.11. As a result, 90nm has reduced power dissipation of 35.13%, 39.84%, 60.13%, 39.38% for sp-domino, cpd, tpod, cpod respectively as scaling is going down. As further scale is going down to 45nm, the power dissipation reduces to 61.21%, 75.83% for cpd and cpod while there is an increase in power dissipation for sp-domino and tpod by 36.66% and 75.84%. Scaling shows better results for cpd and cpod circuits except for sp-domino and tpod circuits.

Table2Comparison of power dissipation of different circuit

Scaling	SP-Domino circuit	CPD circuit	TPOD circuit	CPOD circuit
180nm	3.70e-10	6.30e-10	2.66e-10	7.44e-10
90nm	2.40e-10	3.79e-10	1.06e-10	4.51e-10
45nm	3.28e-10	1.47e-10	2.13e-10	1.09e-10

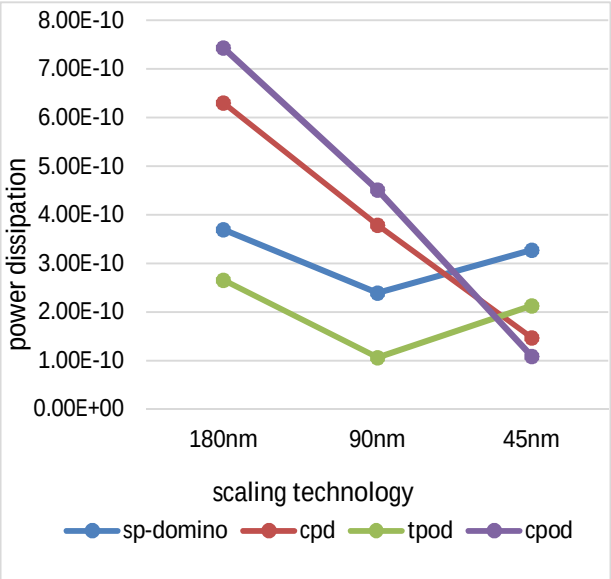

Figure9. Power dissipation versus scaling

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V. CONCLUSION

Scaling has an extensive effects on the circuits. Scaling increases the functional capacity of the chip and device density by reducing the dimension of device. MOSFET capacitances are also reduced due to scaling which reduces switching power dissipation and output switching time.

The existing circuits are simulated at 180nm, 90nm and 45nm using HSPICE. Power dissipation is calculated for particular frequency, load capacitance and fan-in. For a frequency of 2.4MHz, the existed circuits reduces power dissipation of 35.13%, 39.84%, 60.13%, 39.38% for sp-domino, cpd, tpod and cpod respectively from 180nm to 90nm and from 90nm to 45nm, the reduction was 61.21%, 75.83% for cpd and cpod circuits. Hence, cpd and cpod shows better result of scaling.

REFERENCES

[1] Wei. H, Josji. R. H and Henkels, 1999, “a 500-Mhz, 32-word,a 64 bit, eight-port self-resetting CMOS register file”, IEEE Tranactions on Solid-State Circuits, pp.56-67.
[2] Agrawal. A. K, Wairya. S, Nagaria. R.K,Tiwari. S,2009, “Mixed gate diffusion input full adder topology for high speed low power digital circuits”, World Applied Sciences Journal (WASJ: Special Issue of Computer & IT), IDOSI Publication,vol.7,pp.138-144.
[3] Nowka. K. J and Galambos. T, 1998, “Circuit design techniques for a gigahertz integer microprocessor”, IEEE International Conference on Computer Design, pp.11-16.
[4] Krambeck. R. H, Lee. C. M, and Law.H, 1982, “High-speed compact circuits with CMOS”, IEEE Journal of Solid-State Circuits, vol.SC-17, no.3, pp.614-619.
[5] Ankita Sharma, Divyanshu Rao, Ravi Mohan, December (2016) ,“ Design and Implementation of Domino Logic Circuit in CMOS”, Journal of Network Communications and Emerging Technologies (JNCET) www.jncet.org Volume 6, Issue 12.
[6] Manish Kumar (Jan - Feb. 2015),,“ Effects of Scaling on MOS Device Performance”, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 5, Issue 1, Ver. III PP 25-28.
[7] Bijan Davari, Robert H. Dennard and Ghavam G. Shahidi, April 1995,”CMOS Scaling for High Performance and Low Power-The Next Ten Years”, Proceedings of the IEEE,vol.83.no.4,pp.595-606.
[8] G. Yee and C. Sechen, “Clock-delayed domino for dynamic circuit design,” *IEEE Trans. Very Large-Scale Integr. (VLSI) Syst.*, vol. 8, no. 4,pp. 425–430, Aug. 2000.
[9] Charbel. J. A and Magdy. A. B, 2008, “Single-phase SP –domino: A limited-switching dynamic circuit technique for low-power wide fan-in logic gates “, IEEE Transactions on Circuits and Systems, vol.55,no.2, pp.141-145.
[10] A. K. Pandey, Vivek Mishra, R. A. Mishra, R. K. Nagaria, V. K. Rao. K, ‘Conditional Precharge Dynamic Buffer Circuit’, International Journal of Computer Application, 2012, vol.6, pp.0975-8887.
[11] A.K.Pandey, Vivek Mishra, R.K.Nagaria, R.A.Mishra, 2013 ,”Design of triggered pulse operated low power domino buffer circuit”, Mediterranen journal of electronics and communication,vol.9/No.1,pp.485-493,ISSN:1744-2400.
[12] Vivek Mishra, Vivek Kumar Modanwal, 2017, ”Low Power Wide Fan-In Control Pulse Operated Domino (CPOD) Multiplexer with Static Switching”, International Journal of Computer Application, vol.65 ,pp 356-360.

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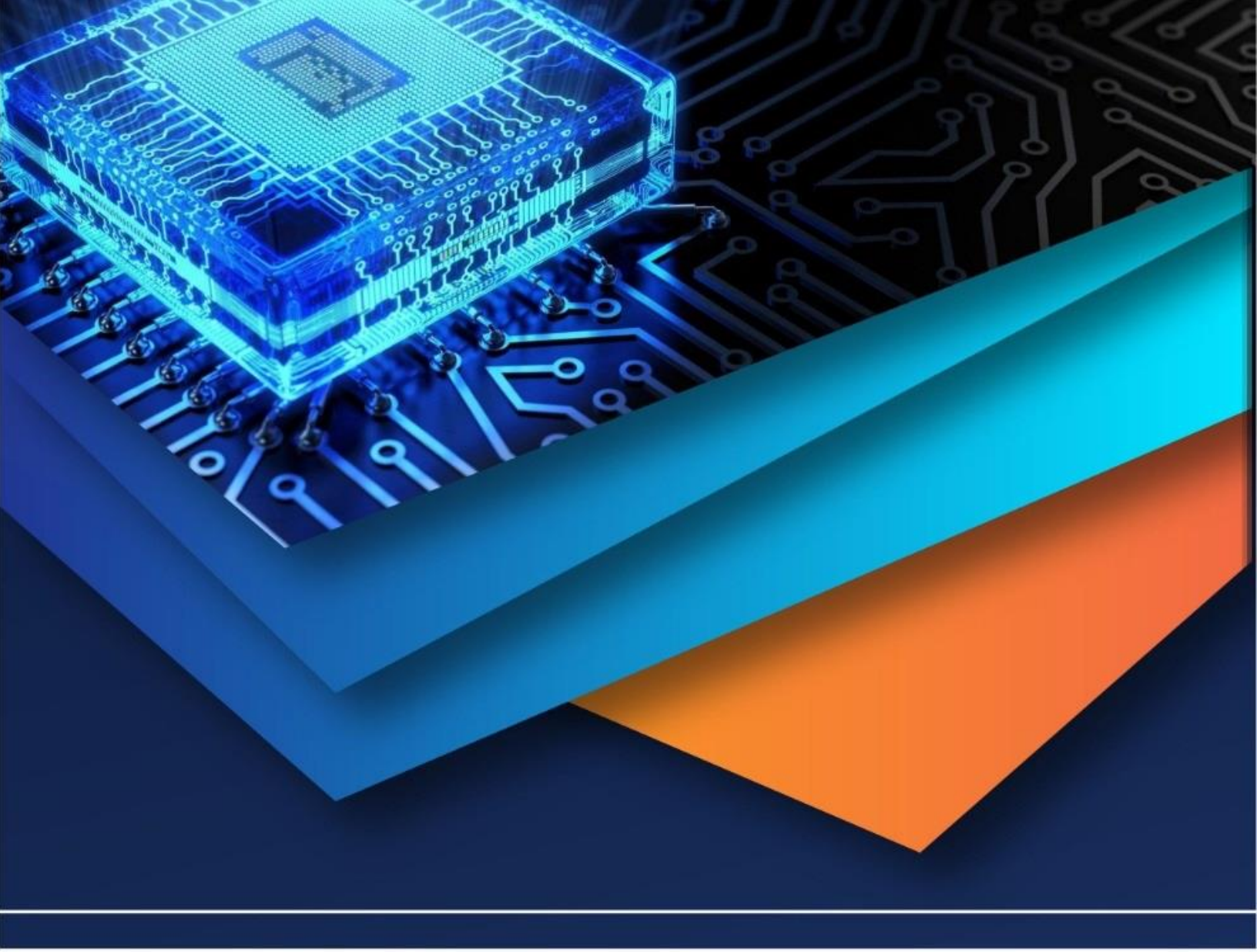

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