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Energy Efficient High Speed Multiplier for Image Compression

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Abstract: ***The aim of this study is to increase the speed of the multiplier for image compression. The image compression is used to reduce the redundancy of the image and store the data in efficient form. This paper show the use of vedic multiplier with pipelining to increase the speed. multiplier is the keyblock of Digital Signal Processing and High performance processors. Vedic mathematics is used in this multiplier to increase the speed. The vedic multiplier is formed by the gates and adder circuits. In this vedic multiplier each and every gate and adder circuit is converted to multiplexer for high speed. CADENCE software is used for designing and simulating the system and the system is coded in verilog HDL.***
Keywords: Vedic multiplier, multiplexer, verilog HDL, vedic mathematics, pipelining, image compression

I. INTRODUCTION

Multiplication is an important block of real-time digital signal processing (DSP) applications and high performance processors. To increase the speed of the circuit using vedic mathematics in the multiplier for implement the image compression. 'Veda' means 'Knowledge'. It is a Sanskrit word. Vedic Mathematics is a collection of sutras to solve mathematic problem in a easy and faster way. Vedic Mathematics consists of 16 sutras which can be used for problems involved in arithmetic, algebra. Urdhva Tiryagbhyam is the most generalised sutra for implementation of There are five sutras for multiplication such as Nikhilam Sutra, Anurupyena Sutra, Urdhva Tiryagbhyam Sutra, Ekayunena Purvena and Antyaordaske'pi. Among these technique, Urdhva Tiryagbhyam is generalized multiplication method.

Urdhva Tiryagbhyam is the vertically and crosswise multiplication which consist of simple addition and multiplication. The beauty of Vedic Multiplier lies in the fact that they can be used to solve cumbersome mathematical operations and thereby improving speed.Vedic multiplier consist of gates and adders circuit. Gates is a electronic circuit having one or more inputs and only one output. Gates are not give the output directly. It do the operation then give the output. Adder is a digital circuit it do the addition operation. In this vedic multiplier each and every block is converted to multiplexer. Multiplexer is a electronic device it has a multiple inputs and a single line output. It also has selection line input. The select lines determine which input is connected to the output and so it also known as data selector. Multiplexer is directly give the output without perform any arithmetic operation and so speed of the vedic multiplier is increased. The 8x8 bit vedic multiplier formed by using four 4x4 vedic multiplier and three 8 bit adders. The 4x4 vedic multiplier is formed by four 2x2 vedic multiplier and three adders. The 2x2 vedic multiplier is formed by two adders and four AND gates.

AND gate can be designed using 2x1 Multiplexer and. the half adder id designed using two 2x1 multiplexer in the 2x2 vedic multiplier. Design is converted into coding by using verilog HDL. This verilog code of 2x2 vedic multiplier is designing and simulating in the CADENCE software. This 2x2 vedic multiplier four and three 4 bit adders are used in 4x4 vedic multiplier. This 4x4 vedic multiplier is coded in verilog HDL. This verilog code of 4x4 vedic multiplier is designing and simulating in the CADENCE software. This 4x4 vedic multiplier four and three 8 bit adders are used in 8x8 vedic multiplier. This 8x8 vedic multiplier is coded in verilog HDL.

This verilog code of 8*8 vedic multiplier is designing and simulating in the CADENCE software. Power dissipation, critical path and cell area are calculated for 2x2 , 4x4 and 8x8 vedic multiplier which converted by multiplexer.Vedic multiplier with pipelining is used to increase the speed of the system. Pipelining is the process of separate the block by register to store the output of the previous block to achieve the parallel performance. Pipelining is consist of D flip flop as a register. Pipelining is the system processing is divided into multiple Stages then system can respond maximum multiple jobs at the same time. A pipelining design is that new data can begin processing before the prior data has been finished because of this, the speed of the vedic multiplier is increased.After analysed the performance of high speed multiplier, to check the performance by apply in application named Discrete Cosine Transform. DCT is used to convert the image spatial domain into frequency domain. This DCT is used in image compression.

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II. EXISTING SCHEME OF 8x8 VEDIC MULTIPLIER

Vedic mathematics is used in this existing scheme Vedic mathematics consist of 16 sutras. Urdhva Tiryagbhyam is the most generalized sutra so Urdhva Tiryagbhyam is used in the multiplier. In the existing scheme adder circuit is converted to MUX and EXOR gate to increase the speed but by using of MUX lot of area was taken so adder circuit only converted to MUX to reduce the Area. The 8x8 vedic multiplier is consist of 4x4 vedic multiplier and three 8 bit adders. The 4x4 vedic multiplier consist of four 2x2 vedic multiplier and three 4 bit adders. The 2x2 vedic multiplier consist of logic gates and adder circuits. First take 2x2 vedic multiplier. In this 2x2 vedic multiplier all adder circuits are converted to MUX and EXOR gate. After converting the 2x2 vedic multiplier the 2x2 vedic multiplier is given to the 4x4 vedic multiplier then in this 4x4 vedic multiplier all adder circuits are converted to MUX and EXOR gate after finishing the 4x4 vedic multiplier this 4x4 vedic multiplier is given to 8x8 vedic multiplier then in this 8x8 vedic multiplier all adder circuits are converted to MUX and EXOR gate. To execute the existing scheme of 8x8 vedic multiplier by using Cadence tool. We can do the simulation, synthesize and make a layout design in the Cadence tool. In the Xilinx timing report only analyzed. So here for analyze the power, area and delay using Cadence tool.In this existing scheme The total power of the design is 29548.58nW. The total area taken by the design is 1846.08 in the terms of cell area. The total delay of the 8x8 Vedic Multiplier is 1147.90 ps.

III.PROPOSED 8*8 VEDIC MULTIPLIER IN DCT

A. 8x8 vedic multiplier

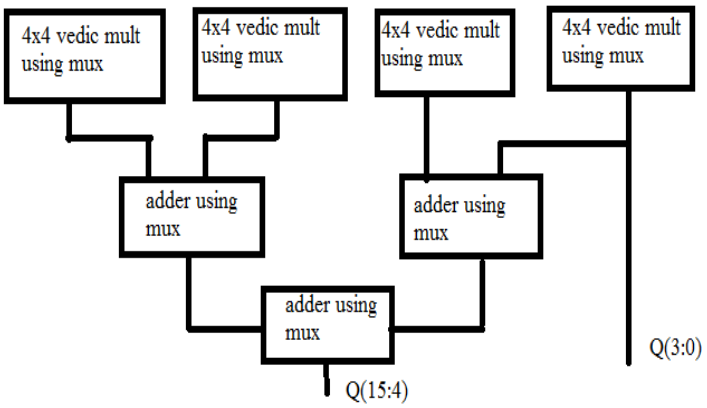


Figure 1:Block diagram of 8x8 vedic multiplier

In this vedic multiplier each and every block is converted to MUX to resuce the power and delay of the circuit. The power,delay and area was analyzed using Cadence tool.

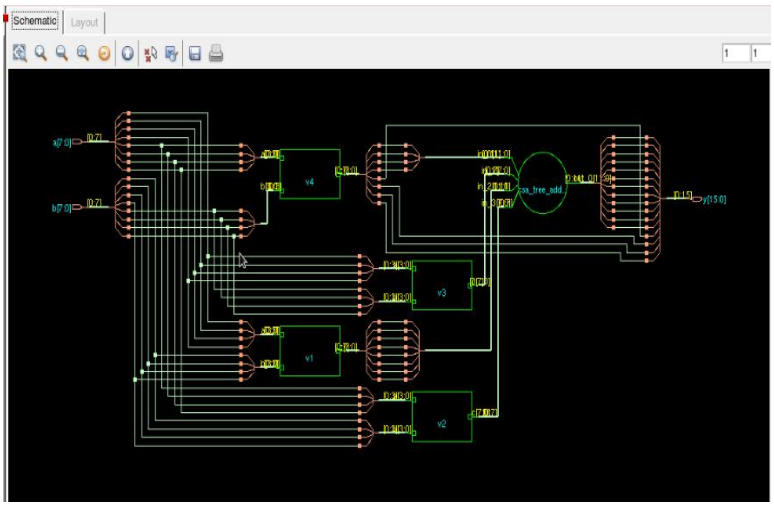


Figure. 2. Schematic diagram of 8x8 vedic multiplier

Table I
Power Analysis of multiplexer based multipler

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
vmult_8	286	20536.53	76536.80	30749.13	107285.92
vmult_8/csa_tree_add_41_44_groupi	34	3235.46	25535.53	7994.82	33530.35
vmult_8/v1	63	4334.66	13755.23	5227.58	18982.81
vmult_8/v1/v1	8	525.21	1051.65	497.86	1549.51
vmult_8/v1/v1/f1	2	173.36	224.04	68.06	292.10
vmult_8/v1/v1/f1/h2	2	173.36	224.04	68.06	292.10
vmult_8/v1/v1/f1/h2/m2	1	128.73	136.26	50.10	186.37
vmult_8/v1/v1/f1/h2/m3	1	44.62	87.76	17.96	105.74
vmult_8/v1/v1/h1	2	173.36	406.31	198.52	604.83
vmult_8/v1/v1/h1/m2	1	128.73	319.10	145.58	464.68
vmult_8/v1/v1/h1/m3	1	44.62	87.21	52.94	140.15
vmult_8/v1/v1/m1	1	44.62	112.39	83.19	195.57
vmult_8/v1/v1/m2	1	44.62	84.22	53.88	138.10
vmult_8/v1/v1/m3	1	44.62	140.43	58.29	198.73
vmult_8/v1/v1/m4	1	44.62	84.25	35.92	120.17
vmult_8/v1/v2	8	525.21	1363.84	530.32	1894.16
vmult_8/v1/v2/f1	2	173.36	374.30	121.32	495.61

Table II
Delay Analysis of multiplexer based multipler

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g542/CO	ADDFX1	1	5.10	27.30	69.40	539.20	F
g537/CI					0.00	539.20	
g537/CO	ADDFX1	1	5.10	27.30	69.40	608.60	F
g536/CI					0.00	608.60	
g536/CO	ADDFX1	1	5.10	27.30	69.40	678.00	F
g535/CI					0.00	678.00	
g535/CO	ADDFX1	1	5.10	27.30	69.40	747.40	F
g534/CI					0.00	747.40	
g534/CO	ADDFX1	1	5.10	27.30	69.40	816.80	F
g533/CI					0.00	816.80	
g533/CO	ADDFX1	1	5.10	27.30	69.40	886.20	F
g532/CI					0.00	886.20	
g532/CO	ADDFX1	1	5.10	27.30	69.40	955.60	F
g531/CI					0.00	955.60	
g531/CO	ADDFX1	3	6.40	39.50	72.00	1027.60	F
g2/A1					0.00	1027.60	
g2/Y	OAI21X1	3	5.30	39.40	38.00	1065.60	R
g526/AN					0.00	1065.60	
g526/Y	NAND2BXL	2	3.50	25.20	33.20	1098.80	R
g524/A					0.00	1098.80	
g524/Y	NAND2XL	1	1.80	23.30	15.80	1114.60	F
g523/B0					0.00	1114.60	
g523/Y	OAI21XL	1	0.00	18.00	12.10	1126.70	R
csa_tree_add_41_44_groupi/out_0[11]							
y[15]	out port				0.00	1126.70	R

Table III
Area Analysis of multiplexer based multipler

Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
vmult_8	286	2004.27	0.00	2004.27	<none>	(D)
vmult_8/csa_tree_add_41_44_groupi	34	399.64	0.00	399.64	<none>	(D)
vmult_8/v1	63	401.16	0.00	401.16	<none>	(D)
vmult_8/v1/v1	8	43.90	0.00	43.90	<none>	(D)
vmult_8/v1/v1/f1	2	12.87	0.00	12.87	<none>	(D)
vmult_8/v1/v1/f1/h2	2	12.87	0.00	12.87	<none>	(D)
vmult_8/v1/v1/f1/h2/m2	1	8.33	0.00	8.33	<none>	(D)
vmult_8/v1/v1/f1/h2/m3	1	4.54	0.00	4.54	<none>	(D)
vmult_8/v1/v1/h1	2	12.87	0.00	12.87	<none>	(D)
vmult_8/v1/v1/h1/m2	1	8.33	0.00	8.33	<none>	(D)
vmult_8/v1/v1/h1/m3	1	4.54	0.00	4.54	<none>	(D)
vmult_8/v1/v1/m1	1	4.54	0.00	4.54	<none>	(D)
vmult_8/v1/v1/m2	1	4.54	0.00	4.54	<none>	(D)
vmult_8/v1/v1/m3	1	4.54	0.00	4.54	<none>	(D)
vmult_8/v1/v1/m4	1	4.54	0.00	4.54	<none>	(D)
vmult_8/v1/v2	8	43.90	0.00	43.90	<none>	(D)
vmult_8/v1/v2/f1	2	12.87	0.00	12.87	<none>	(D)

In this Proposed scheme the Total power consumed by MUX based Vedic Multiplier is 30749.13nW. The total area taken by the design is 2004.27 in the terms of cell area. The total propagation delay of the Vedic Multiplier is 1126.70 ps.

B. 8x8 vedic Multiplier with Pipelining

Pipelining is used to reduce the delay of the circuit. In this pipelining D Flip Flop is used to proceed the parallel processing in the circuit. Compare with normal 8x8 vedic multiplier, multiplexer based vedic multiplier give the high speed and low delay with power efficiency.

Similarly compare with multiplexer based vedic multiplier, pipelined multiplexer based multiplier provide energy efficient (low power consumption) and high speed (Less delay)

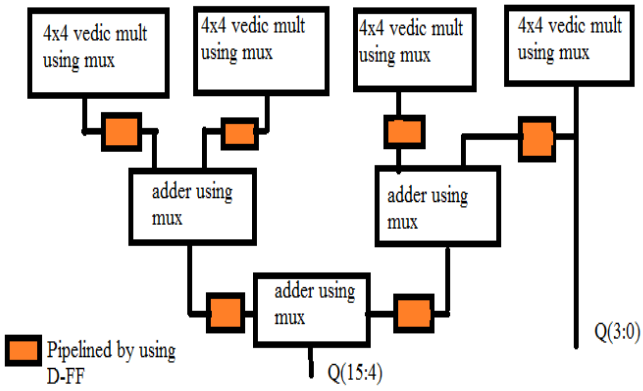


Figure. 3.Block diagram of 8x8 vedic multiplier with pipelining

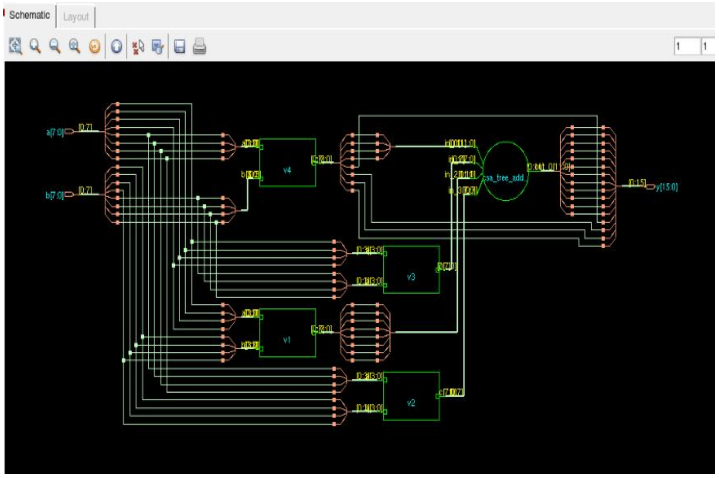


Figure .4.Schematic diagram of 8x8 vedic multiplier with pipelining

Table IV

Delay Analysis of multiplexer based multipler with pipelining

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g536/CO	ADDFX1	1	5.10	27.30	69.40	507.90	F
g531/CI					0.00	507.90	
g531/CO	ADDFX1	1	5.10	27.30	69.40	577.30	F
g530/CI					0.00	577.30	
g530/CO	ADDFX1	1	5.10	27.30	69.40	646.70	F
g529/CI					0.00	646.70	
g529/CO	ADDFX1	1	5.10	27.30	69.40	716.10	F
g528/CI					0.00	716.10	
g528/CO	ADDFX1	1	5.10	27.30	69.40	785.50	F
g527/CI					0.00	785.50	
g527/CO	ADDFX1	1	5.10	27.30	69.40	854.90	F
g526/CI					0.00	854.90	
g526/CO	ADDFX1	1	5.10	27.30	69.40	924.30	F
g525/CI					0.00	924.30	
g525/CO	ADDFX1	3	6.40	29.50	72.00	996.30	F
g2/A1					0.00	996.30	
g2/Y	OAI21X1	3	5.30	39.40	38.00	1034.30	R
g520/AN					0.00	1034.30	
g520/Y	NAND2BXL	2	3.50	25.20	33.20	1067.50	R
g518/A					0.00	1067.50	
g518/Y	NAND2XL	1	1.80	23.30	15.80	1083.30	F
g517/B0					0.00	1083.30	
g517/Y	OAI21XL	1	0.00	18.00	12.10	1095.40	R
csa_tree_add_41_44_groupI/out_0[11]							
y[15]	out port				0.00	1095.40	R

Table V
Power Analysis of multiplexer based multipler with pipelining

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
/mult8_pl	558	63464.83	58917.98	4350.64	63268.63
/mult8_pl/csa_tree_add_41_44_groupi	34	3235.46	0.00	0.00	0.00
/mult8_pl/v1	131	15071.48	14562.70	326.76	14889.47
/mult8_pl/v1/v1	25	3209.42	3686.65	85.71	3772.36
/mult8_pl/v1/v1/d1	1	181.73	312.56	0.00	312.56
/mult8_pl/v1/v1/d2	1	181.73	279.52	0.00	279.52
/mult8_pl/v1/v1/d3	1	181.73	312.56	0.00	312.56
/mult8_pl/v1/v1/d4	1	181.73	180.38	0.00	180.38
/mult8_pl/v1/v1/d5	1	181.73	345.61	0.00	345.61
/mult8_pl/v1/v1/f1	10	1424.59	1262.64	0.00	1262.64
/mult8_pl/v1/v1/f1/d1	1	181.73	180.38	0.00	180.38
/mult8_pl/v1/v1/f1/d2	1	181.73	180.38	0.00	180.38
/mult8_pl/v1/v1/f1/d3	1	181.73	180.38	0.00	180.38
/mult8_pl/v1/v1/f1/h1	1	181.73	180.38	0.00	180.38
/mult8_pl/v1/v1/f1/h1/d2	1	181.73	180.38	0.00	180.38
/mult8_pl/v1/v1/f1/h2	6	697.66	541.13	0.00	541.13
/mult8_pl/v1/v1/f1/h2/d1	1	181.73	180.38	0.00	180.38

Table VI
Area Analysis of multiplexer based multipler with pipelining

Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
/mult8_pl	558	5843.27	0.00	5843.27	<none>	(D)
/mult8_pl/csa_tree_add_41_44_groupi	34	399.64	0.00	399.64	<none>	(D)
/mult8_pl/v1	131	1360.91	0.00	1360.91	<none>	(D)
/mult8_pl/v1/v1	25	283.84	0.00	283.84	<none>	(D)
/mult8_pl/v1/v1/d1	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/d2	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/d3	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/d4	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/d5	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/f1	10	124.89	0.00	124.89	<none>	(D)
/mult8_pl/v1/v1/f1/d1	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/f1/d2	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/f1/d3	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/f1/h1	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/f1/h1/d2	1	15.89	0.00	15.89	<none>	(D)
/mult8_pl/v1/v1/f1/h2	6	61.31	0.00	61.31	<none>	(D)
/mult8_pl/v1/v1/f1/h2/d1	1	15.89	0.00	15.89	<none>	(D)

In this Vedic multiplier with pipelining total power consumed by MUX based Vedic Multiplier is 4350.64nW. The total area taken by the design is 5843.27 in the terms of cell area. The total propagation delay of the Vedic Multiplier is 1095.40 ps.

C. Application of high speed multiplier

For analyse the performance of multiplier which had to be applied in specific application. Discrete Cosine Transform is the one of the best application of multiplexer. Transform coding constitutes an integral component of contemporary image/ video processing application. Transform coding relies on the premise that pixels in an image exhibit a certain level of correlation with their neighbouring pixels. Discrete Cosine Transform has emerged as the image transformation in the most visual system. It is same family of Fourier Transform.

The block of Discrete Cosine Transform is consist of adder, multiplier and register circuits. Replace the multiplier block by multiplexer based multiplier with both with pipelining and without pipelining. Then analyse the performance of DCT on basic parameter such as power consumption, critical path delay and area

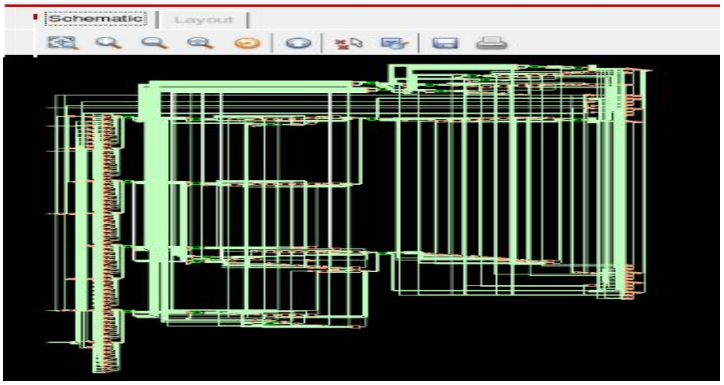


Figure. 5. Schematic diagram of DCT using 8x8 vedic multiplier without pipelining

Table VII
Delay Analysis of DCT using vedic multiplier without pipelining

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g161/A					0.00	1698.30	
g161/Y	NAND2XL	1	1.80	20.60	16.50	1714.80	F
g160/B0					0.00	1714.80	
g160/Y	OAI21XL	1	3.80	49.30	25.90	1740.70	R
v3/c[3]							
g472/B					0.00	1740.70	
g472/Y	CLKXOR2X1	2	3.50	18.40	53.40	1794.10	F
g459/B					0.00	1794.10	
g459/Y	NOR2XL	1	1.80	24.30	23.80	1817.90	R
g456/B0					0.00	1817.90	
g456/Y	AOI21XL	2	3.50	27.80	16.90	1834.80	F
g453/B					0.00	1834.80	
g453/Y	NOR2XL	1	1.80	25.50	26.50	1861.30	R
g452/B0					0.00	1861.30	
g452/Y	AOI21XL	2	3.50	33.40	17.10	1878.40	F
g449/A					0.00	1878.40	
g449/Y	NAND2XL	1	1.80	20.10	22.60	1901.00	R
g448/B0					0.00	1901.00	
g448/Y	OAI21XL	1	1.70	20.30	17.90	1918.90	F
v16/y[7]							
g2824/B0					0.00	1918.90	
g2824/Y	AOI22XL	1	1.60	34.20	30.40	1949.30	R
g2787/A					0.00	1949.30	
g2787/Y	NAND3XL	1	0.00	18.20	12.70	1962.00	F
data_out[7]	out port				0.00	1962.00	F

Table VIII
Power Analysis of DCT using vedic multiplier without pipelining

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
dct	1649	105543.23	675662.76	303619.58	979282.34
dct/b1	68	2362.20	7518.06	8167.19	15685.24
dct/b2	66	2642.79	8753.58	10316.83	19070.41
dct/b3	66	2642.79	8761.82	11056.06	19817.88
dct/b4	68	2362.20	7966.87	8513.17	16480.04
dct/b5	61	2522.41	17415.63	14211.51	31627.14
dct/b6	61	2522.41	19078.95	16754.09	35833.04
dct/b9	24	1502.97	24343.77	12149.47	36493.24
dct/b11	66	2617.50	44423.41	25435.52	69858.93
dct/b12	68	2353.77	45152.58	23652.35	68804.93
dct/v1	63	3814.10	24266.57	9589.88	33856.45
dct/v1/v3	10	795.72	3707.49	1225.76	4933.25
dct/v1/v3/v3	1	128.73	408.62	95.79	504.42
dct/v1/v3/v3/h1	1	128.73	408.62	95.79	504.42
dct/v1/v3/v3/h1/m2	1	128.73	408.62	95.79	504.42
dct/v1/v3/v4	4	346.72	1464.91	421.92	1886.84
dct/v1/v3/v4/f1	2	173.36	668.15	163.85	832.01

Table IX
Area Analysis of DCT using vedic multiplier without pipelining

Gate	Instances	Area	Library
NAND3XL	16	72.66	fast
NOR2BXL	83	376.94	fast
NOR2XL	100	302.76	fast
NOR3BXL	2	12.11	fast
OAI21X1	10	45.41	fast
OAI21XL	225	1021.82	fast
OAI22XL	7	42.39	fast
OAI2BB1XL	40	211.93	fast
OAI31XL	2	12.11	fast
OR2X1	5	22.71	fast
SDFFQX1	64	1307.92	fast
XNOR2X1	46	382.99	fast
XNOR2XL	4	33.30	fast
XOR2X1	31	258.10	fast
XOR2XL	2	16.65	fast
TOTAL	1649	10277.19	

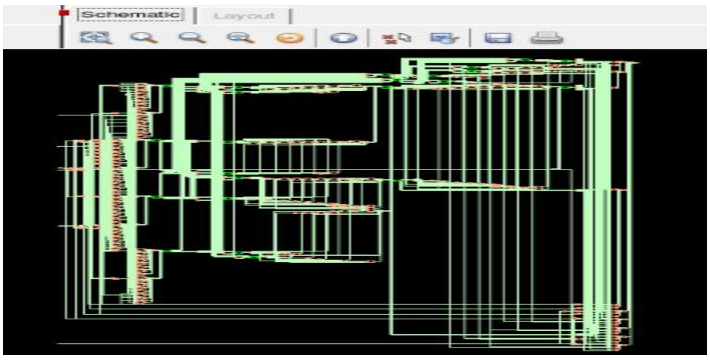
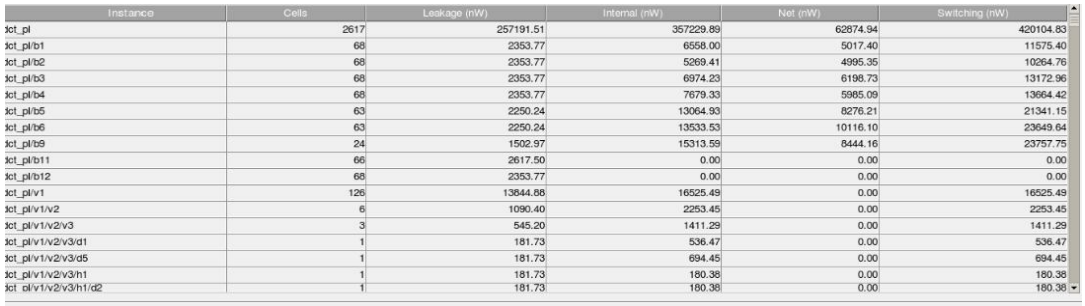


Figure. 6. Schematic diagram of DCT using 8x8 vedic multiplier with pipelining

Table X
Delay Analysis of DCT using vedic multiplier with pipelining

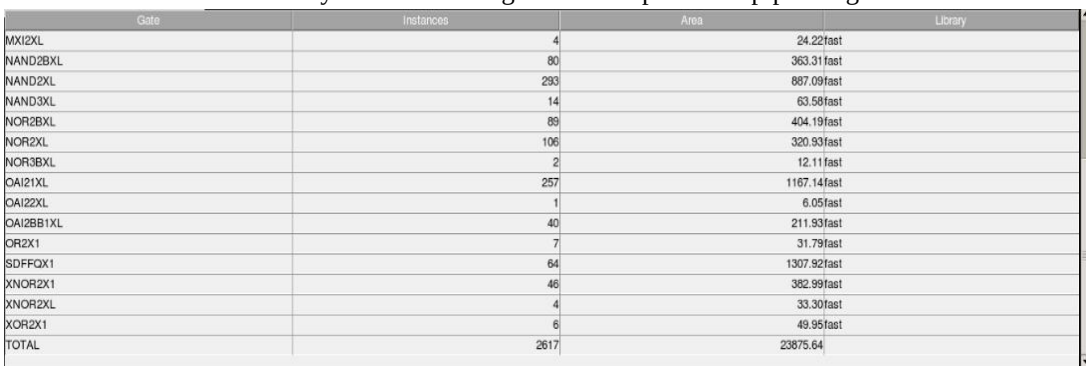
Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
g971/Y	NOR2BXL	2	3.60	41.20	46.00	917.50	R
g953/AN					0.00	917.50	
g953/Y	NAND2BXL	3	7.30	43.80	46.70	964.20	R
g915/B					0.00	964.20	
g915/Y	CLKXOR2X1	2	3.60	18.60	53.40	1017.60	F
b12/sum[6]							
g2859/B					0.00	1017.60	
g2859/Y	NOR2BXL	2	3.60	40.40	35.50	1053.10	R
g2855/AN					0.00	1053.10	
g2855/Y	NAND2BXL	2	3.50	25.20	33.30	1086.40	R
g2849/A					0.00	1086.40	
g2849/Y	NAND2XL	1	1.80	18.50	15.80	1102.20	F
g2848/B0					0.00	1102.20	
g2848/Y	OAI21XL	2	3.60	46.90	24.60	1126.80	R
v16/a[6]							
v3/a[2]							
v3/a[0]							
m3/sel							
g11/B					0.00	1126.80	
g11/Y	AND2X1	1	1.70	13.00	34.70	1161.50	R
m3/out							
d2/data							
q_reg/D	DFFQX1				0.00	1161.50	
q_reg/CK	setup				0.00	103.30	1264.80	R

Table XI
Power Analysis of DCT using vedic multiplier with pipelining



Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
dct_pl	2617	257191.51	357229.89	62874.94	420104.83
dct_pl/b1	68	2353.77	6558.00	5017.40	11575.40
dct_pl/b2	68	2353.77	5269.41	4995.35	10264.76
dct_pl/b3	68	2353.77	6974.23	6198.73	13172.96
dct_pl/b4	68	2353.77	7679.33	5985.09	13664.42
dct_pl/b5	63	2250.24	13064.93	8276.21	21341.15
dct_pl/b6	63	2250.24	13533.53	10116.10	23649.64
dct_pl/b9	24	1502.97	15313.59	8444.16	23757.75
dct_pl/b11	66	2617.50	0.00	0.00	0.00
dct_pl/b12	68	2353.77	0.00	0.00	0.00
dct_pl/v1	126	13844.88	16525.49	0.00	16525.49
dct_pl/v1/v2	6	1090.40	2253.45	0.00	2253.45
dct_pl/v1/v2/v3	3	545.20	1411.29	0.00	1411.29
dct_pl/v1/v2/v3/d1	1	181.73	536.47	0.00	536.47
dct_pl/v1/v2/v3/d5	1	181.73	694.45	0.00	694.45
dct_pl/v1/v2/v3/h1	1	181.73	180.38	0.00	180.38
dct_pl/v1/v2/v3/h1/d2	1	181.73	180.38	0.00	180.38

Table XII
Area Analysis of DCT using vedic multiplier with pipelining



Gate	Instances	Area	Library
MXI2XL	4	24.22	fast
NAND2BXL	80	363.31	fast
NAND2XL	293	887.09	fast
NAND3XL	14	63.58	fast
NOR2BXL	89	404.19	fast
NOR2XL	106	320.93	fast
NOR3BXL	2	12.11	fast
OAI21XL	257	1167.14	fast
OAI22XL	1	6.05	fast
OAI2BB1XL	40	211.93	fast
OR2X1	7	31.79	fast
SDFFQX1	64	1307.92	fast
XNOR2X1	46	382.99	fast
XNOR2XL	4	33.30	fast
XOR2X1	6	49.95	fast
TOTAL	2617	23875.64	

IV. CONCLUSIONS

The proposed scheme provide the low power consumption to achieve energy efficiency and provide less delay to achieve high speed by altering the existing scheme. Design can be further develop into image compressor which consist sub block of DCT, quantizer and encoder. By replace the DCT block with DCT by using multiplexer based multiplier provide energy efficient and high speed performance.

Parameter	DCT using multiplexer based multiplier without pipelining	DCT using multiplexer based multiplier with pipelining
Power in nW	303619.13	62874.94
Delay in ps	1962.00	1264.80
Area in cell	16277.19	23875.65

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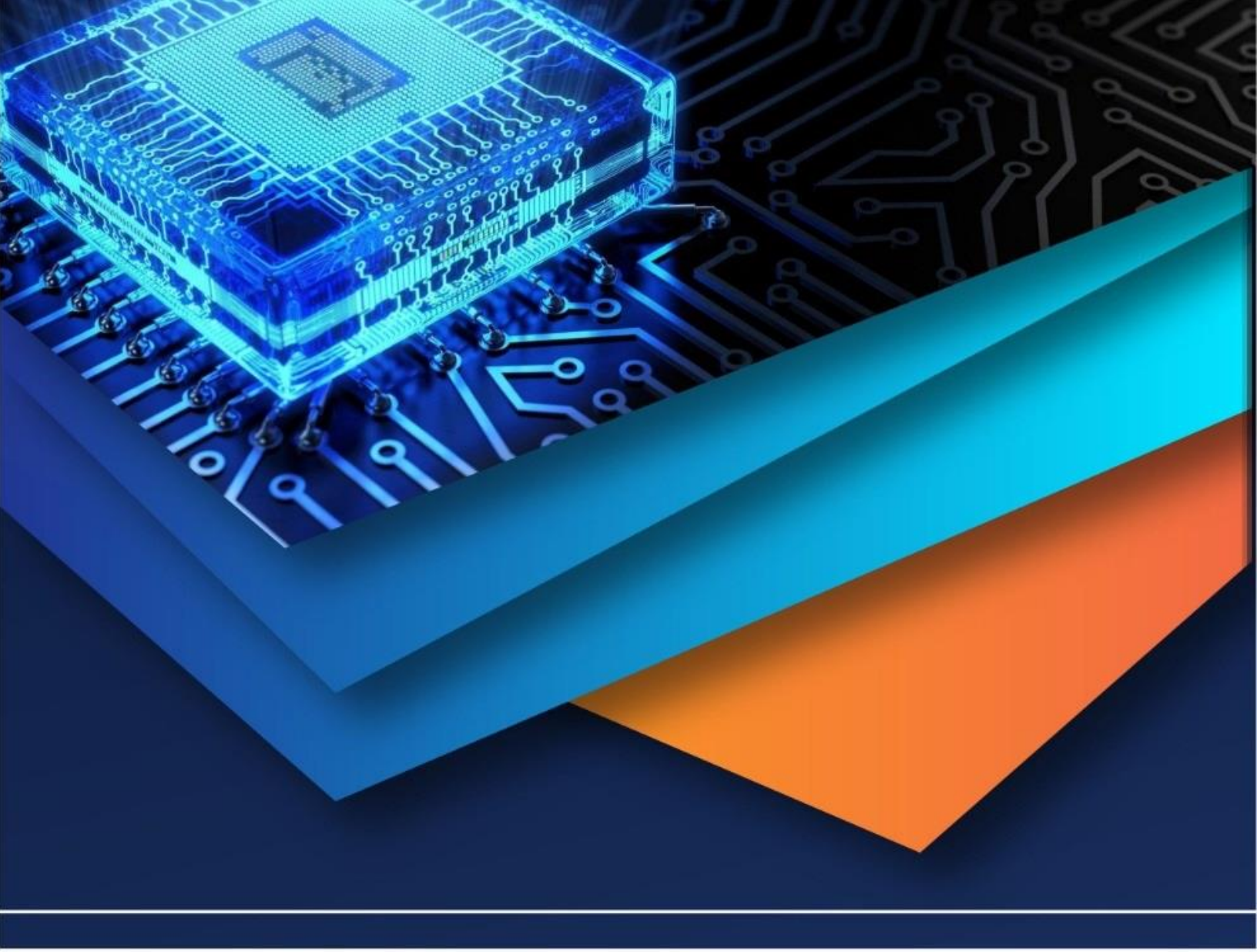

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IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

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