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Design of low offset Dynamic Comparators for High speed ADC Architectures

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Abstract*— A Switched Dynamic Comparator proposed for a 4 bit 12 GS/s ADC solely attains the various requirements under Radio Astronomy. Here the Non-interleaved Full Flash ADC architecture overcomes the mismatches (phase skew error) in traditional Time Interleaved ADC's using SDC with clock $f_s/2$ followed by reducing the input capacitance. Also, the offset error voltage is cancelled by the Digital Background Calibration circuit.

Keywords*— Analog-to-digital conversion; Dynamic comparator; Interleaved analog-to-digital converter; Phase skew error; Switched Dynamic Comparator (SDC); Reference Switched Dynamic Comparator (R-SDC).

I. INTRODUCTION

Comparators are probably the second most widely used electronic component after operational amplifier. They are also popularly known as the 1-bit analog to digital converter and abundantly used in A/D converters. Analog to Digital Converter (ADC) is a basic device in digital signal processing systems. ADC bridges the gap between the analog world and the digital systems. Very high-speed, low resolution A/D converters have applications in wideband communications such as SKA (Square Kilometer Array). The SKA will be an array of coherently connected antennas whose key scientific requirement is the ability to carry out sensitive observations of the sky over areas. They also include software defined radio and measurement equipment such as high speed oscilloscopes. High speed oscilloscopes require internal circuitry that runs at very fast sampling rate so that high speed signals can be captured [1].

Traditional way of achieving the target speed while minimizing power consumption is by using combinational circuit technique, including serial sampling and high speed latching. The most common approach is to use the interleaving architecture for A/D converter. However their performance benefits are not without drawbacks, in additions to the increased power consumption and physical layout area that accompany a large design, there are some issues that are unique to time interleaving [2]. These problems degrade the accuracy of the time interleaved systems, and include gain errors, offset errors and phase skew [3].

To alleviate this effect and to save power consumption the Switched Dynamic Comparator (SDC) is proposed. It allows a non-interleaved architecture in order to obtain high speed with simple circuitry.

In Section II, provides a detailed description of the conventional dynamic comparator. Section III, shows the analysis made to overcome the issues faced by existing comparator with simulation results. Section IV, gives an overview of Flash analog-to-digital converter and Section V, describes ADC with the proposed SDC.

II. CONVENTIONAL DYNAMIC COMPARATOR

In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison [4]. A drawback of traditional flash architectures is the large static power consumption in the preamplifier chain [5].

The dynamic latched comparators are very attractive for many applications such as high speed analog to digital converters (ADCs), memory sense amplifiers (SAs) and data receivers, due to fast speed, low power consumption, high input impedance and full swing output [6] [7]. Fig 1 (a) shows the conventional two stage circuit where $V_{ip,n}$ are the signal inputs, $V_{op,n}$ are the outputs and V_{clk} is the single phase clock input.

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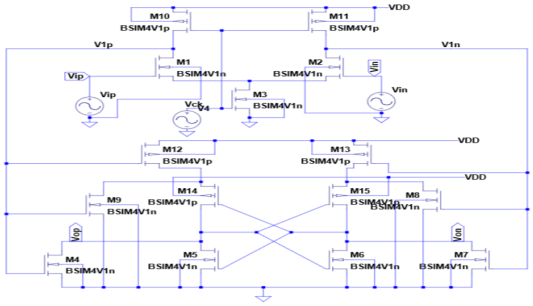

Fig 1 a. Dynamic Comparator Circuit representation using LTspice IV

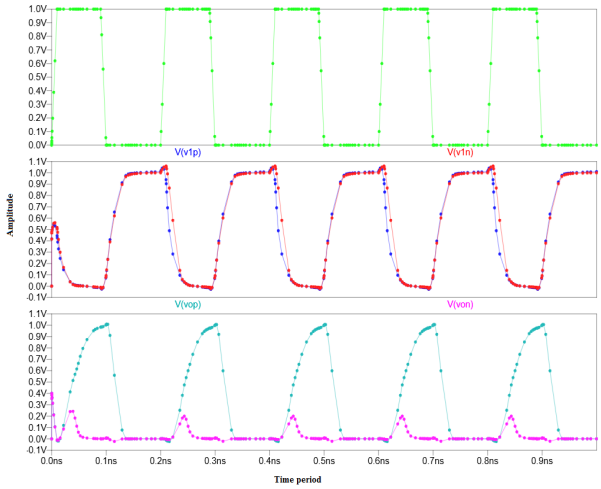

Fig 1 b. Signal Waveform illustrates the working of dynamic comparator

The operating principle is in either during reset phase (V_{clk}==0) or set phase (V_{clk}==VDD). Here the charge/discharge time τ_d is small for the first stage compared to the second stage. This particular behavior of the second stage limits the regeneration time causing the stage 1 to be idle for most of the period as shown in the Fig 1 (b), which creates a challenge for them to operate at maximum operating frequency. Hence in order to operate at high speed with small LSB, SDC is proposed. The simulation results of the above circuit and its waveform generated during transient analysis.

III.PROPOSED SWITCHED DYNAMIC COMPARATORS

The architecture consists of dynamic preamplifier stage and two latches LAT1 and LAT2 as in Fig 2. The pre-amp operates in the first stage eventually drives the LAT1 and LAT2. Shown in Fig 3 (a) Sharing of the stages will reduce power consumption. Vck0 is the clock input of the dynamic pre-amp which operates at T_{ck0} clock period whereas the LAT1 and LAT2 operates at 2 x T_{ck0} as the clock period. The signal pairs are $V_{1p,n}$ and $V_{2p,n}$ are the inputs for which the circuit exhibits the output signal pairs as V_{op1}/V_{on1} and V_{op2}/V_{on2} respectively.

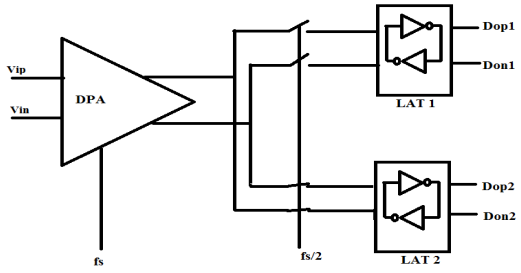

Fig 2. Block diagram of Switched dynamic comparator

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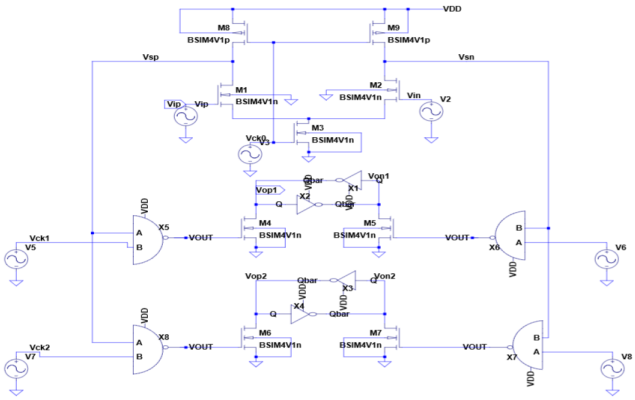

Fig 3 a. Circuit representation of Switched dynmamic comparator

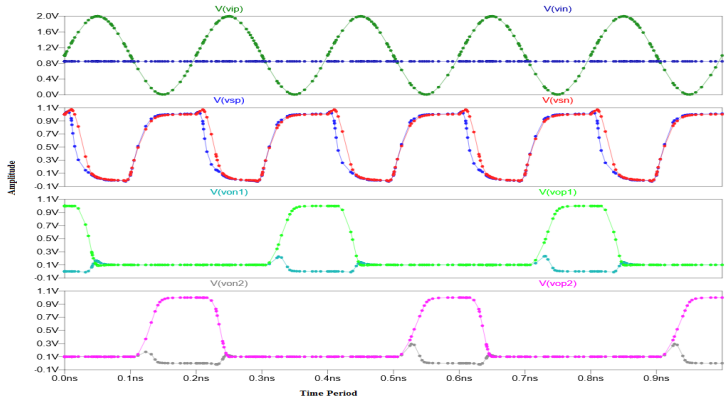

Fig 3b. Waveform explaining the operation of proposed swiched dynamic comparator

Here the two dynamic comparators in the SDC are exactly the same and we have discussed about one of them as an example. Their operation lies in either "reset" or "regeneration" phase of the time frame. The circuit thus exhibits an extended regeneration time for it to operate at maximum operating frequency which could be inferred from the Fig 3 (b), which is 1.5 times the clock period of T_{ck0}. Thus the clock speed is 3 times that of the conventional dynamic comparators. The simulated signal behaviour of the proposed SDC using a simulation tool is as follows. To dynamically correct the offset error voltage. Tuneable capacitor arrays were added to the nodes V_{1pn} and V_{2pn} depicted in the Fig 4a and 4b.

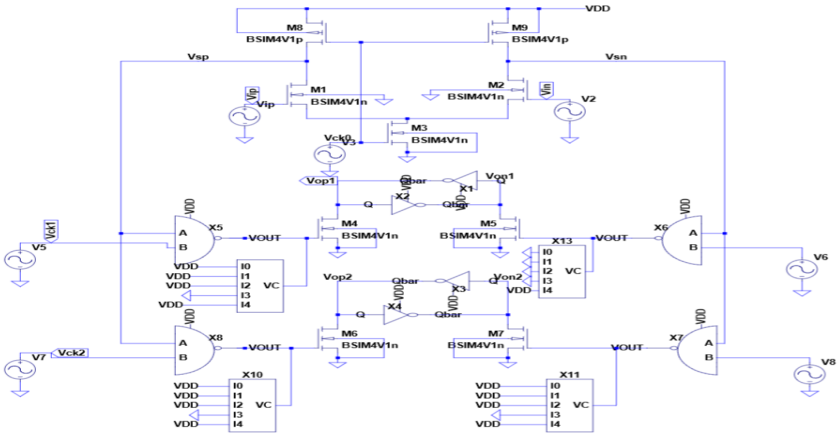

Fig 4a Switched dynamic comparator with tuneable capacitor array for error voltage correction

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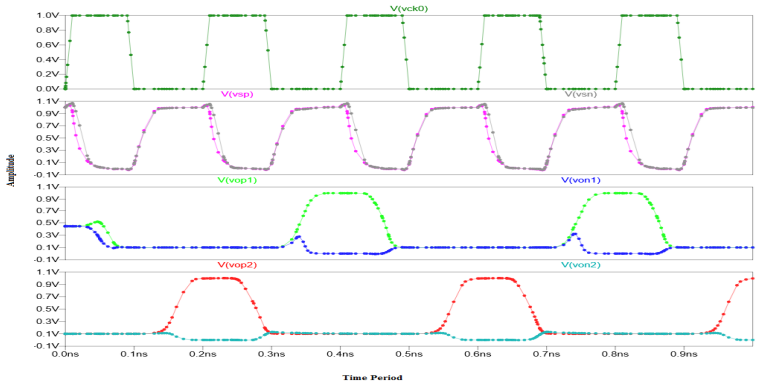

Fig 4b. Signal waveform of SDC with tuneable capacitor array

The Noise analysis on the comparator circuitry help us to significantly identify the efficient circuitry,

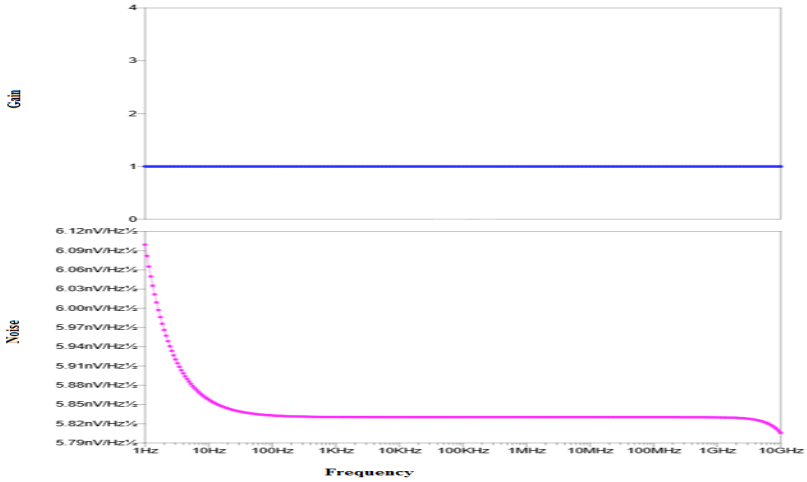

Fig 5 a. Waveform representing the noise component of the dynamic comparator circuit

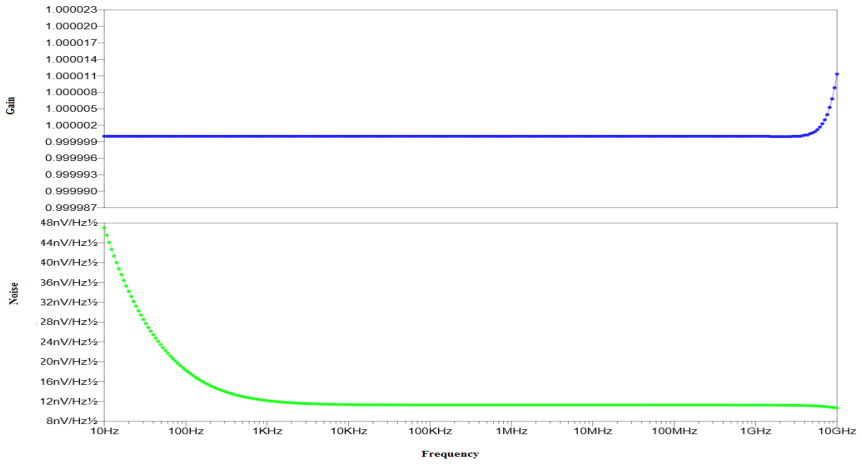

Fig 5 b. Waveform representing the noise component of the switched dynamic comparator circuit

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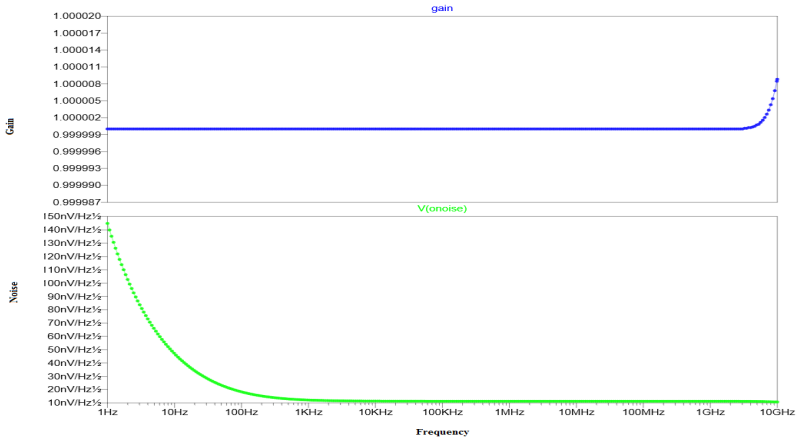

Fig 5 c. Waveform representing the noise component of the switched dynamic comparator circuit with tunable capacitor array

IV. NON INTERLEAVED FLASH ADC ARCHITECTURE

The block diagram of the ADC architecture shown in Fig 6 is with 15 SDCs quantizes the input signal, followed by encoded and multiplexing circuitry. One reference SDC is used for the background calibration which measured the trip voltage generated by introducing an intentional imbalance in each differential pair [8]. The measured ADC output spectrum obtained with the FFT observed to be 12000 MHz (approximately) for the input signal with full swing at 600 MHz (approximately).

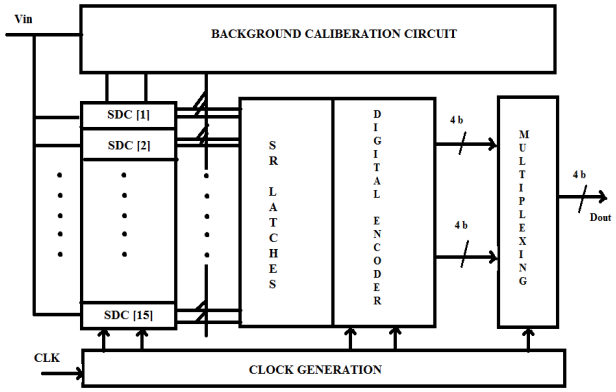

Fig 6. Detailed block diagram of the Full Flash ADC

Below are the various essential circuit which are building block of the analog-to-digital converter,

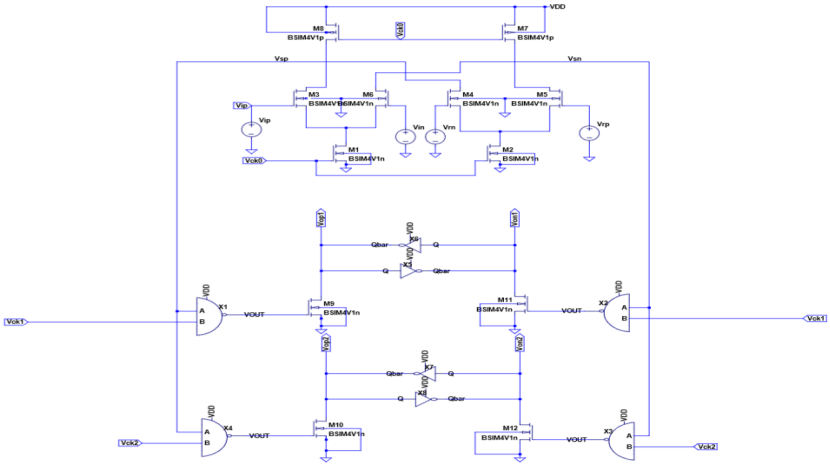

Fig 7a. Schematic circuit representation of the Reference-SDC

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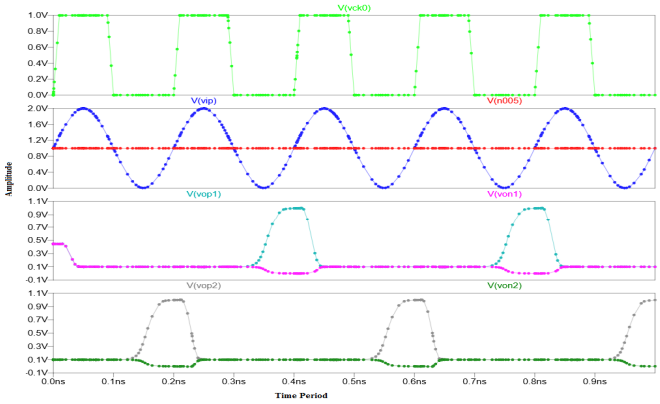

Fig 7 b. Signal waveform of Reference-Switched dynamic comparator

The background calibration circuit shown uses the single reference comparator concept and this scheme is realized by sampling the analog input signal with one R-SDC, the circuit is represented in Fig 7 a, with selectable reference levels from a high-impedance reference ladder, and comparing the results sequentially with each SDC to correct errors in the comparator trip voltages. The R-SDC is a modified version of the SDC [9].

The proper reference voltage VR_n should be chosen for the R-SDC, where VR_n is the expected trip voltage for SDC_n [10]. Since the R-SDC and SDC_n sample the same analog input, their outputs should be the same when trip voltages are identical as in Fig 7 b.

Operation of the Flash architecture is governed by the clocking circuit which operates with the differential input producing rail to rail output shown in Fig 8a and 8b.

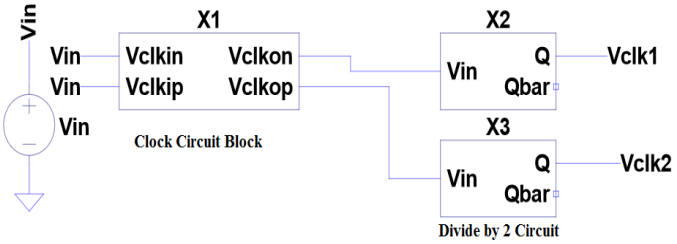

Fig 8 a. Block diagram of Clock circuitry

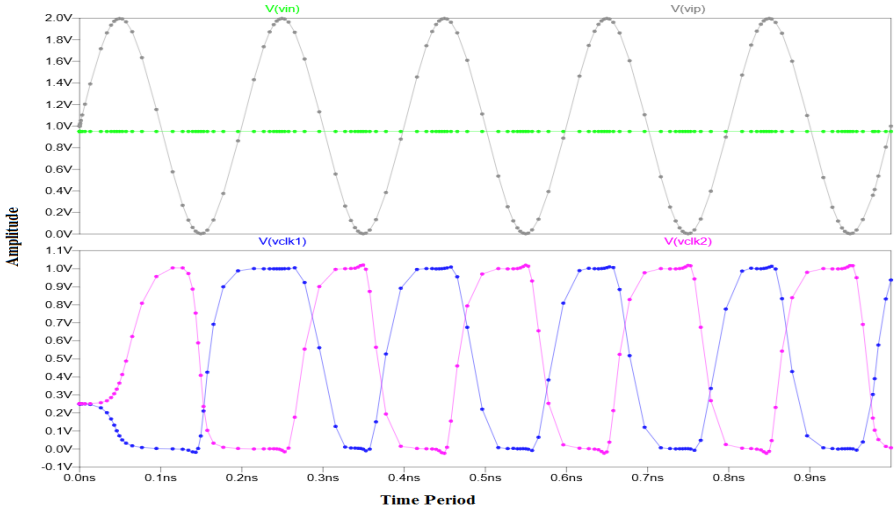

Fig 8 b. Signal waveform of clock input to ADC

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Table 1 summarizes the designed ADC whose operating frequency is high and thus suitable for high speed applications.

TABLE I
DEVELOPED ADC USING THE PROPOSED SDC

Parameter	Values
Technology	IBM 65nm CMOS
Power Supply	1 V
Input Range	200mV
Resolution	4-bit
Auto-calibration	background
Sample Rate	12 GS/s

V. CONCLUSIONS

This paper representing the 12 GS/s ADC using SDC suitable for the SKA receiver chain as it satisfies its requirement of high operating speed, low power consumption. Thus SDC alleviates the phase skew calibration and overcomes the various mismatches experienced with the traditional architectures. Thereby it resolves the speed limitations with the small LSBs in conventional dynamic comparators caused due to the problems with the charging /discharging at the first stage and also due to short regeneration at the second stage of amplification.

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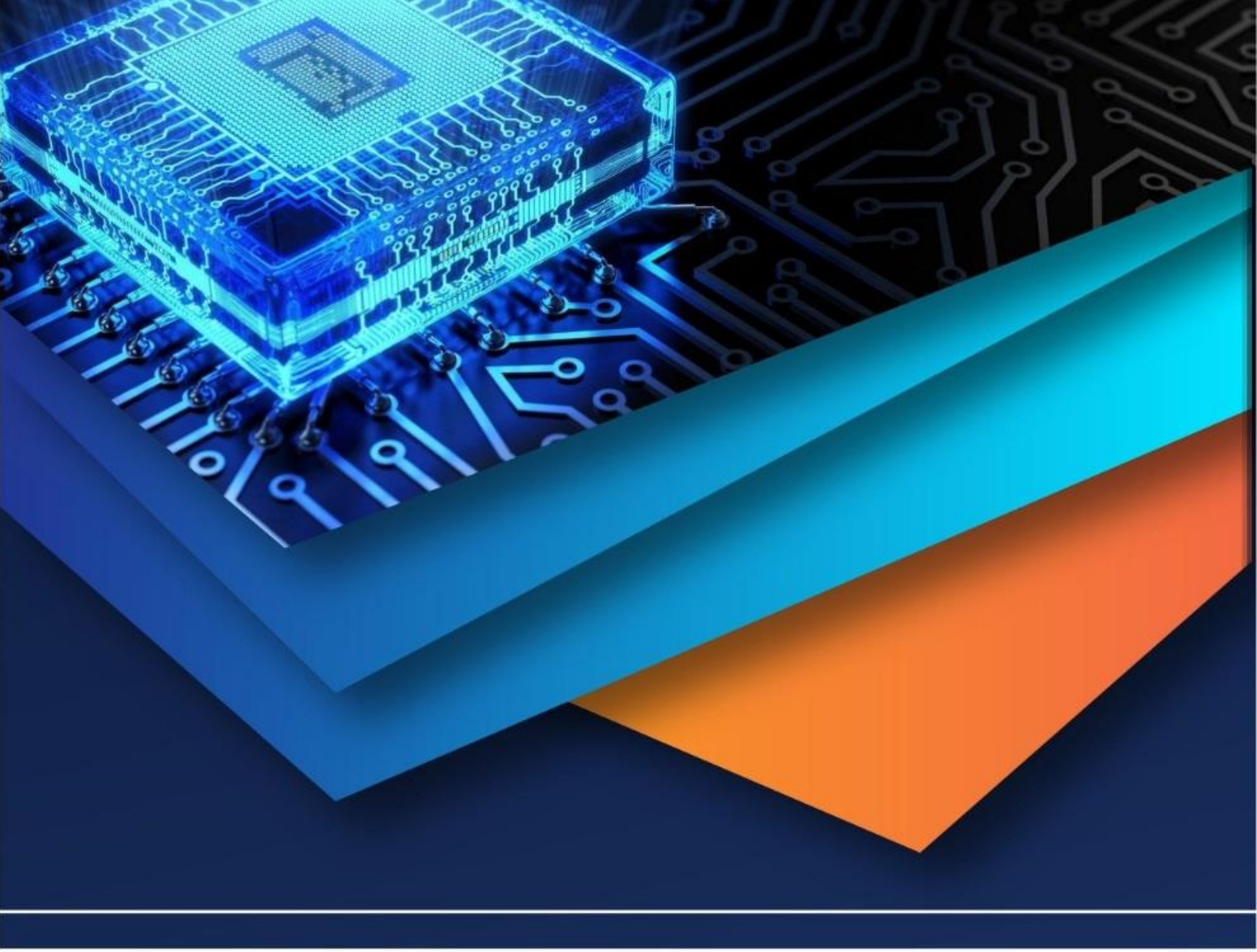

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