iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 8 **Issue:** V **Month of publication:** May 2020

DOI: http://doi.org/10.22214/ijraset.2020.5129

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue V May 2020- Available at www.ijraset.com

NOC based Router Architecture to Reduce Power using Round Robin Algorithm

Nanammal. V[1], Shaju Christo. C[2]
[1]*Asst.Professor, Department of Electronics and Communication Engineering, Jeppiaar Engineering College, Chennai – 600119.*
[2]*P G Scholar, Department of VLSI Design, Jeppiaar Engineering College, Chennai – 600119.*

Abstract: ***A network on a chip is a network based communication subsystem on an integrated circuit, most typically between modules in a system on chip (SoC). The modules on the IC are typically semiconductor IP cores schematizing various functions of the computer system and are designed to be modular in the sense of network science. The network on chip is a switching network between SOC in the router. Deadlock and Livelock freedom in Routing is one of current issue in NoC routing. The Deadlock and livelock freedom prohibiting certain routing turns. NOC based architecture uses great amount of power. To schedule the processes, a round-robin scheduler generally allocate time for sharing, giving each job based on time slot (its allowance of CPU time) and interrupts the duty if it's not completed by them. When the duty is resumed next time a time slot is assigned to it. If the process ends or changes its state to waiting during its fixed time quantum, the scheduler selects the primary process within the ready queue to execute. In the absence of time sharing, or if the quantum were large relative to the size of the role, a process that produced large jobs would be preferred over other processes. Round-robin algorithm is a pre algorithm technique as the scheduler forces the process out of the CPU once the time allocation expires. Round robin algorithm reduces the dynamic power in the module. The algorithm is written by using Verilog HDL and tested on Xilinx 14.7 ISE and the algorithm is implemented by using FPGA VERTEX5 kit.***

Keywords: Round Robin Algorithm, Crossbar Switch, Network on Chip, Routing, Unidirectional, Livelock and Deadlock, System on Chip, TTL, IP, Look up Table(LUT).

I. INTRODUCTION

Routing is the process of selecting a path for traffic in a network between or across multiple networks. Broadly, routing process will be carried out in many types of networks, including circuit switched networks, such as the public switched telephone networks (PSTN) and computer networks, such as the Internet. In packet switching networks, routing is the higher level decision maker that directs the network packets from their source toward their destination through their intermediate network nodes by specific packet forwarding mechanism process. Packet forwarding is the transit of network packets from one network interface to another network interface. Intermediate nodes such as routers, firewalls gateways or switches are some of the network hardware devices. General purpose computers are also forward packets and perform routing process, although they have no specially optimized hardware for their task.

The routing process usually transmit on the basis of routing table, which maintain an enlist of the routes to various network destinations. Routing tables can be specified by an administrator, learned by observing network traffic or built with the help of routing protocols. Routing is a narrower sense of the term, often refers to IP routing and is contrasted with unstructured addressing process.

IP routing assumes that network addresses gets structured and that similar addresses imply proximity within the network. Structured addresses allow a single routing table entry to represent the router to a group of devices. In large area networks, structured addressing i.e. routing in the narrow sense, outperform bridging (unstructured addressing). Routing has become the dominant form of addressing in the Internet. Bridging is still widely used within most local area networks (LAN).

Router architecture is designed in such a way that routers are forced to perform two major functions: Process routable protocol and routing protocol, to determine their best path. The best example of a routed protocol is IRA very basic definition of IP is that it acts as the mailman of the Internet.

Its job is to organize data into a packets, which is then addressed for the delivery. IP can place a target and source address on the packet. This is similar to addressing a package before delivering it to the postal office. In the world of IP, the postage is a Time-to-live (TTL).

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue V May 2020- Available at www.ijraset.com

II. CIRCUIT DESCRIPTION

The Block diagram of the router architecture describes about the connections and the algorithm process that is carried out in the router. Here, the FIFO is connected to the crossbar and the round robin algorithm (arbiter). The crossbar switch is connected to the output of the FIFO and the arbiter input. The output is achieved from Crossbar switch. The output is based on the selection pin input of the arbiter. Arbiter changes the input based on the needs and the input given to it. It works as the CPU of the router. The same input is given as the processed output. P1, P2, P3, P4 are the four different inputs given from the IP of another cell.

The routing process usually transmits on the basis of routing tables, which maintain a record of the routes to various network destinations. Routing tables may be specified by an administrator, learned by observing network traffic or built with the help of routing protocols. Routing means, often refers to IP routing and is contrasted with bridging. IP routing assumes that network addresses are structured and that similar addresses and process imply proximity within the network. Structured addresses (routing in narrow sense) allow a single routing table entry to represent the route to a lot of devices. In large networks, structured addressing outperforms unstructured addressing. Routing has become the major form of addressing on the Internet. Bridging is still widely used within local area networks (LAN). Three multiplexers namely X, Y and Z of the DSP48E1 slice are of main interest as their operation can be reconfigured based on the cycle.

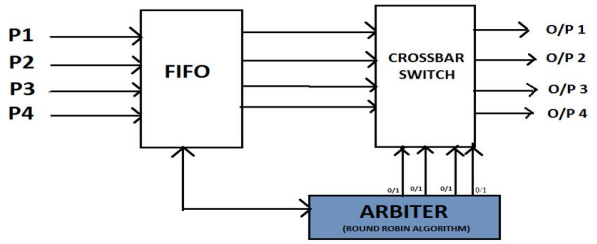


Fig. Router Architecture

III. PRINCIPLE OF OPERATION

The main purpose of a router is to connect various networks and forward packets destined for their networks or any other networks. A router is considered as a 3-layer device. The packet is placed in a transmit queue until the link layer processor is ready to transmit the packet to the output interface. This is like the receiver queue or FIFO queue and usually takes the form of ring memory buffers. The operation of the router is controlled by one or more general purpose processor which is generally similar like standard high end CPU.

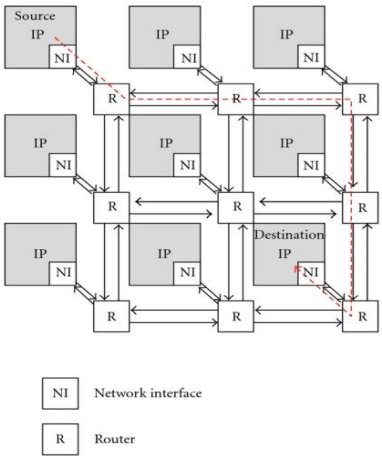


Fig: Router Internal Functions

The processor's performs various tasks, which may be divided into three groups; they are Process Switching, Fast Switching and Routing. The first two tasks are considered first and remaining is followed by concern packet forwarding. The final task, may be in some routers be performed by a separate processor, Every router allows packets to be handled by a CPU using software which implements the various protocols which define the IP network layer. This process is known as the "Slow Path", It is generally much slower than processing by Fast Switching.

©IJRASET: All Rights are Reserved

IV. ROUND ROBIN ALGORITHM

Round Robin algorithm is employed as the network schedulers in routing process. Round robin scheduling is usually used for time slices (This process is named as time quanta) are assigned to each and every process in equal portions and in a circular order, handling all processes without priority (also known as cyclic executive process). Round-robin scheduling is simple and easy to implement and also starvation free. Round-robin scheduling can also be applied to any other scheduling process like data packet scheduling in computer networks. It is an operating system concept. The name Round robin algorithm came from the round robin principle.

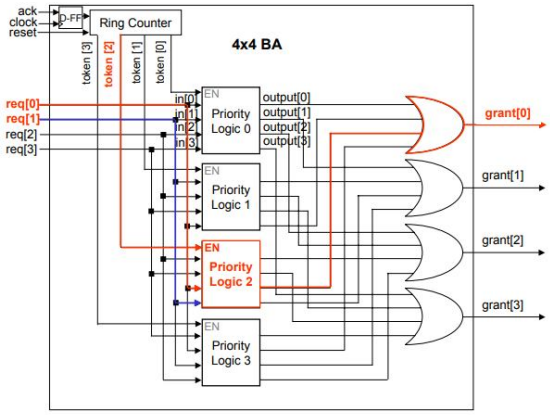


Fig: Round Robin Internal Architecture

V. CROSSBAR SWITCH

The X, Y and Z multiplexers and ALU unit along with the IN MODE, OP MODE and ALU MODE control signals are responsible for mapping the crossbar functionality of the NoC router onto the DSP48E slices. The multiplexers are controlled based on a per cycle basis by modifying the OPMODE (output mode) signals as per the user needs. The ALU MODE is configured to handle (X+Y+Z) operation in the proposed work. Two DSP48E1 slices of a DSP tile has been aware of map the functionality of the crossbar switch. The configuration of the X, Y and Z multiplexers of the DSP48E1 slice are based on the NoC crossbar unit. Two DSP48E1 slices are interconnected by using the cascaded links. They are PCIN and PCOUT.

The input ports are mapped to the DSP48E. Slice inputs and the OPMODE signals are configured based on these encoded signals from the arbiter. As an example, if the East input has been granted with the Local output port by the arbiter, (Fig. shows the crossbar switch internal functions) the corresponding encoded signal, i.e., 00110 is used to configure the NoC router inputs at the DSP48E1 slice inputs. As per the encoded signal by the arbiter, the East inputs are configured at the C input of the DSP48E1 slice with the OPMODE control signals set to 0001110.

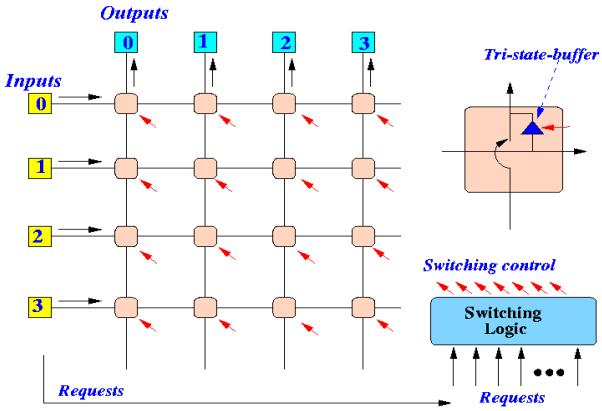


Fig: Crossbar Internal Functions

This configuration will map the East input port to the Local output port. By employing these properties, the right inputs to the X, Y and Z multiplexers of the DSP48E1 slices have been presented at the right time to achieve the behavior of NoC crossbar.

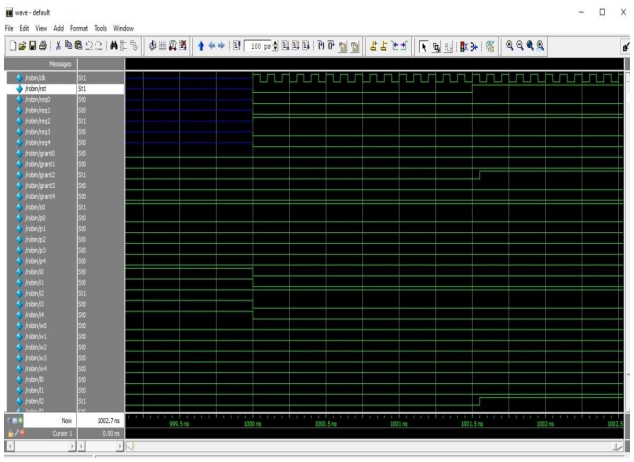
©IJRASET: All Rights are Reserved

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue V May 2020- Available at www.ijraset.com

VI. RESULTS AND DISCUSSION

In this work, The performance of Arbiter (Round Robin Algorithm), Crossbar Switch and Router with Crossbar switch and Arbiter are explained and showed. Here it's showed that the LUT size and power are reduced the delay further and therfore and the power can be reduced by applying the other technique.

A. Output Simulation of Round Robin Algorithm



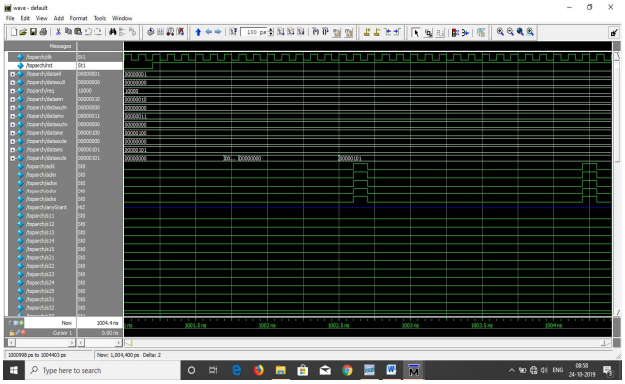
B. Device Utilization Summary of Crossbar Switch

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	120	3,840	3%
Number of 4 input LUTs	97	3,840	2%
Number of occupied Slices	73	1,920	3%
Number of Slices containing only related logic	73	73	100%
Number of Slices containing unrelated logic	0	73	0%
Total Number of 4 input LUTs	97	3,840	2%
Number of bonded IOBs	91	141	64%
Number of BUFGMUXs	1	8	12%
Average Fanout of Non-Clock Nets	2.37		

The device utilization summary of the Crossbar switch shows the usage of LUT in this paper, The usage of LUT was reduced in the proposed model which is tabulated below.

C. Router Output

The output is based on the selection pin which is connected between crossbar switch and arbiter. Here, arbiter works on the principle of Round Robin Algorithm.



©IJRASET: All Rights are Reserved

Crossbar only	High Performance NoC Simulation Acceleration frame-work employing the Xilinx DSP48E1 blocks.	NoC based router architecture to reduce power using round robin algorithm
No. of slice Flip Flops	148	120
No. of slice LUTs	163	97
No. Of occupied Slices	79	73

VII. CONCLUSION

In this work, the router architecture was implemented by using the round robin algorithm. It is one of the simplest forms of scheduling process it helps to reduce the power in the NoC module and it also reduces the few amount of Area in the module. It also reduces the delay by reducing the livelock and dead lock problems. The crossbar switch acts as the both MUX and DEMUX. The crossbar switch helps to implement and to transfer the information based on the selection pin from the arbiter which works on the round robin algorithm. This process is implemented as the unidirectional process. The Proposed technique is executed by utilizing Xilinx (ISE 14.7).

REFERENCE

[1] A. Guerrero, G. Maas, and W. Hogland, “Solid wa[1] T. Kogel, M. Doerper, A. Wiefrink, R. Leupers, G. Ascheid, ”A Modular Simulation Framework for Architectural Exploration of On-Chip Interconnection Networks,” in Proc. IEEE/ACM/IFIP International Conference on Hardware/ Software Codesign and Systems Synthesis (CODES/ISSS), pp. 712, 2003.

[2] B. Dally and B. Towles, ”Route Packets, Not Wires: On-Chip Interconnection Networks,” in Proc. of IEEE Design Automation Conference (DAC), pp. 684-689, 2001.

[3] N. Binkert, B. Beckmann, G. Black, S. K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. R. Hower, T. Krishna, S. Sardashti, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M. D. Hill and D. A. Wood, ”The GEM5 Simulator,” SIGARCH Computer Architecture News, vol. 39, no. 2, pp. 1-7, 2011.

[4] E. S. Chung, E. Nurvitadhi, J. C. Hoe, B. Falsafi and K. Mai, ”PROToFLEX: FPGA-Accelerated Hybrid Functional Simulator,” in IEEE Int’l Symp. on Parallel and Distributed Processing Symposium, vol. 1, no. 6, pp. 26-30, 2007.

[5] Z. Tan, A. Waterman, R. Avizienis, Y. Lee, H. Cook, D. Patterson and K. Asanovic, ”RAMP Gold: An FPGA-based Architecture Simulator multiprocessors, ”in Proc. Of IEEE Design Automation Conference (DAC), pp. 463468, 2010.

[6] S. S. Mukherjee, P. Bannon, S. Lang, A. Spink and D. Webb, ”The Alpha 21364 Network Architecture, ” in IEEE Micro, vol. 22, no. 1, pp. 26-35, 2002.

[7] S. Borkar, ”Thousand Core Chips: A Technology Perspective,” in Proc. of ACM/IEEE Design Automation Conference (DAC), pp. 746749, 2007

[8] J. Nan, J. Balfour, D. U. Becker, B. Towles, W. J. Dally, G. Michelogiannakis and J. Kim, ”A Detailed and Flexible Cycle-Accurate Network-on-Chip Simulator,” in Performance Analysis of Systems and Software (ISPASS), Proc. of Int’l Symp. on., pp. 86-96, 2013.

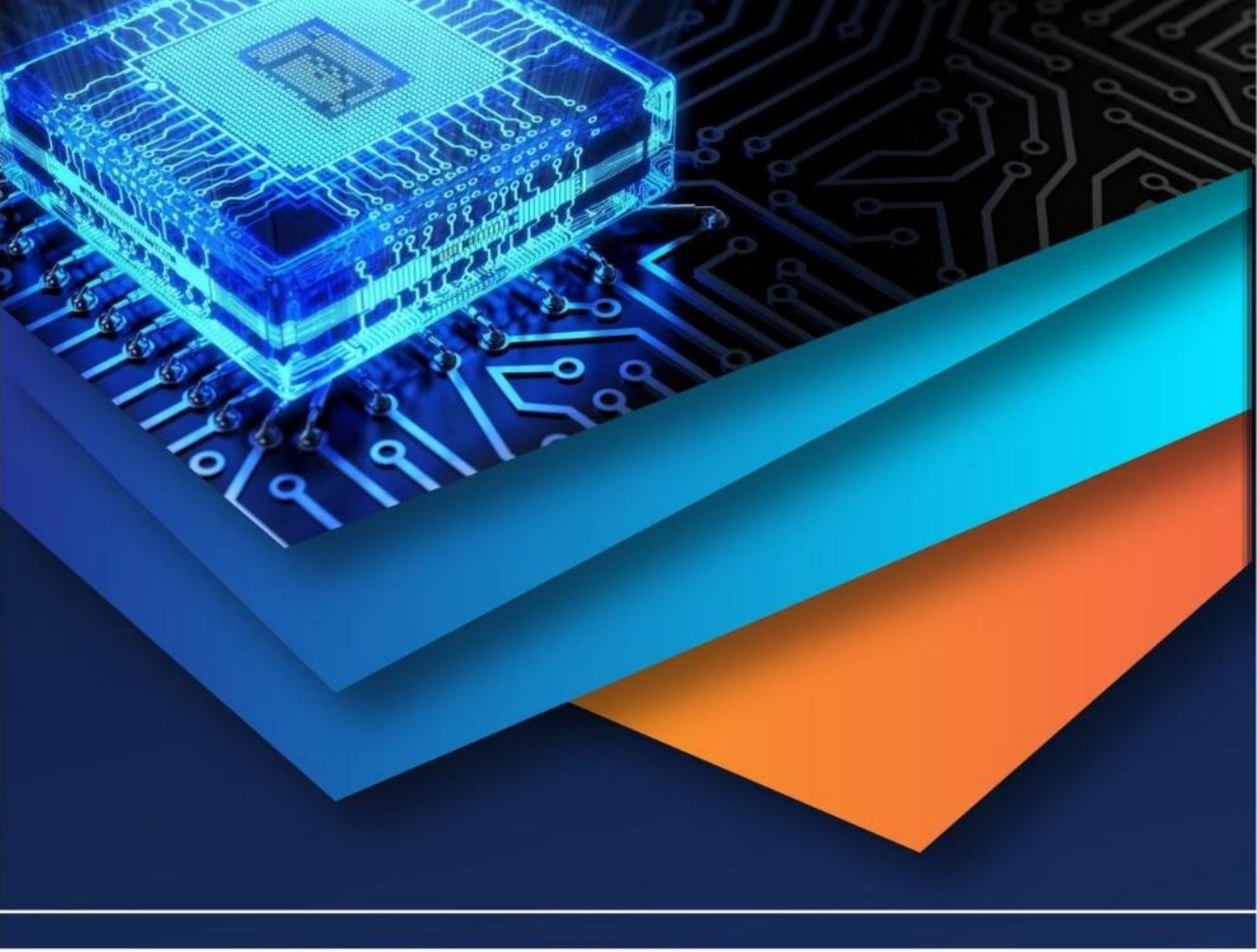
[9] K. Goossens, J. Dielissen, O. P. Gangwal, S. G. Pestana, A. Radulescu and E. Rijpkema, ”A Design Flow for Application-Specific Networks on Chip with Guaranteed Performance to Accelerate SOC Design and Verification,” in Proc. Design, Automation and Test in Europe(DATE), pp. 1182-1187, 2005

[10] L.-S. Peh and W. J. Dally, ”A Delay Model for Router Microarchitectures,” in IEEE Micro, vol. 21, no. 1, pp. 26-34, 2001.

[11] Xilinx Inc., ”ZC706 PCIe Targeted Ref. Design (UG963)” Available: https://www.xilinx.com/support/documentation/boards_and_kits/zc706/2_014_4/ug963-zc706-pcie-trd-ug.pdf,2015.

[12] D. Seo, A. Ali, W. T. Lim, N. Rafique and M. Thottethodi, ”Near-Optimal Worst-Case Throughput Routing for Two-Dimensional Mesh Networks,” in Proc. of Int’l Symp. on Computer Architecture (ISCA), pp. 432-443, 2005.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)