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An Efficient VLSI Design of Polar Encoder Architecture

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Abstract: ***In the developing world much know-how are growing faster and faster as they are becoming reduced, one such is the very large scale integrated design-VLSI. Many trials are faced in VLSI; among them is the crosstalk frequency. The emerging research is going on the polar codes in the application of MIMO system. Polar encoder & Decoder is mainly designed because of its high processing speed as compared with other techniques. The VLSI implementation process can be extended to a large extent by using radix-k based design. This Proposed System Implemented using Verilog HDL and Simulated by Modelsim 6.4 c.***
Keywords: MIMO, Polar encoder and decoder, VLSI

I. INTRODUCTION

To relieve the impacts of errors which happens during the transmission might be due to the nearness of clamor and obstruction, channel coding is utilized. It is principally utilized in versatile correspondence. An encoding is the way toward changing the data into another arrangement while going through the transmitting gadget and it is recouped at the less than desirable end. The transmitting gadget might be another client or another base station . The beneficiary recoups the first data by wiping out the errors which happens during transmission. These days the channel limit is accomplished that is as close as the hypothetical worth with the goal that the data is transmitted with no error, which is known as the superior channel codes. For the transmission of little messages polar codes are favored since it gives better error execution. There is no accessibility of standard systems for this codes so it is seen as less develop as contrasted and different codes for example, turbo codes, LDPC codes. In third era applications, turbo codes are utilized though in Wireless Fidelity (WiFi) turbo codes isn't appropriate and Low Density Parity Check (LDPC) codes are utilized.
The benefit of utilizing the polar code is that isn't as it were lessens the multifaceted nature yet in addition accomplishes its Shannon limit by considering the Binary Discrete Memory less Channel (BDMC).
To figure the Discrete Fourier Transform (DFT) for playing out the procedure of range investigation FFT plays a very powerful job and its design is inferred utilizing different hypothesis, for example, hypercube hypothesis.

II. LITERATURE SURVEY

Many researchers have researched about polar encoding process. M. Garrido, proposed that the Polar codes are an as of late found group of limit accomplishing codes that are viewed as a significant leap forward in coding hypothesis. Inspired by the ongoing quick advancement in the hypothesis of polar codes, we propose a semi-equal design for the execution of progressive dropping deciphering. We exploit the recursive structure of polar codes to utilize preparing assets. The determined engineering has a low handling multifaceted nature while the memory unpredictability stays like that of past models. This exceptional decrease in handling multifaceted nature permits extremely enormous polar code decoders to be actualized in equipment. A N =2 17 polar code progressive abrogation decoder is executed in a FPGA. We additionally report union outcomes for ASIC [16].
Yoo Ho Young and Park In Cheol said for achieving channel capacity easily ,polar codes can be implemented. The parallel encoder is easy to implement, but difficult to support long polar codes. So efficient encoder model must be implemented to reduce complexity [1]. Kia Nin, KaiChen compared polarcodes with different coding techniques like successive cancellation coding and turbo coding. They said that polar cods has limitation in code length. To overcome this problem they implemented rate compatible punctured polar codes using puncturing algorithm [7]. Manohar Aiynala and Michael Brown grouped together and introduced parallel architecture for FFT. The operating frequency is reduced in order to reduce power consumption. This architecture was designed for real valued FFT [4]. Mathis Seidl & Andreas Scherk introduced technique to optimize polar coding and 2m-ary Digital Pulse Amplitude Modulation schemes. Then later Multilevel coding and Bit-Interleaved coded modulation is considered[5]. Heesam Mahdavifar constructed polar codes for two user multiple access channels. Time sharing concept was introduced. Here encoding process is done by polar encoder and decoding process is done by successive cancellation decoder and the results are analyzed [14].

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Harish Vangala and Emanuel Viberto has researched about systematic and non-systematic polar codes. Arikan said computation complexity of systematic and non-systematic polar codes are same. They proposed three efficient encoders with (NlogN) complexity. Their encoder uses same number of XORs as that of non-systematic polar encoder[15].

Mangala J, Manikandan J proposed that the correspondence frameworks are widely utilized in an enormous number of uses, for example, radar, aviation, maritime/oceanic correspondence, submerged correspondence, portable correspondence and some more. The most significant module in planning correspondence framework incorporates structure of modulators. Various applications request various kinds of modulators. Reconfigurable processing is considered as a best in class approach for framework structure, wherein a similar equipment can reconfigure itself to perform various functionalities and is henceforth utilized for different applications. Plan and usage of reconfigurable modulators on Virtex-5 FPGA is proposed right now, the sort of adjustment can be powerfully reconfigured on-the-fly dependent on the necessity at a specific example. The sort of modulators that are utilized for reconfiguration right now Amplitude Modulation (AM), Frequency Modulation (FM), Frequency Shift Keying (FSK), Phase Shift Keying (PSK), and Amplitude Shift Keying (ASK). Right now, approaches of activating utilized for proposed reconfigurable modulator configuration is accounted for. Additionally the proposed plan is executed utilizing single and two reconfigurable squares and the outcomes are accounted for. It is seen that 10.20 - 91.43% of equipment assets and 76.38% of intensity are saved money on utilizing the proposed reconfigurable modulator over the ordinary non-reconfigurable modulator[17].

Song Nam Hong and Dennis Hui designed low complexity decoders. They have proposed system consists of number of polar codes in parallel along with information bit divider at the input of each polar encoder. This code is called as parallel concatenated polar codes. Since it has limitation in length, it extends its support only to some set of rates. This limitation can be overcome by using punctured polar codes which can provide flexibility as advantage[13].

III. EXISTED METHOD

The data bit is applied as the contribution to the polar encoder whose yield will be the encoded bit which at that point goes through different stages to improve the security of the data. Figure 1 shows the fundamental outline for a polar code channel. The whole procedure is separated into numerous stages. In the stage 1, the information u0 and u1 is applied to A0 where the exclusive- Or on the other hand (XOR) activity is performed. For instance, on the off chance that we take the estimation of information u0=111 and u1=111, at that point we get the ideal yield as A0=111. The double info data bits may shift from 000 to 111.Similarly, when u2 and u3 is applied as the contribution to A1 and its yield is acquired in the wake of playing out the XOR activity and the procedure goes on.

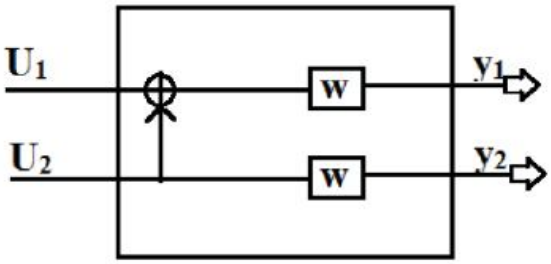

Figure 1: Basic0Polar0code0channel

The output of stage 1 is applied as the input to next stage which is denoted by w_{ij} where 'j' represents the edge and 'i' represents the stage. Generally the output B0 will be generated by performing the addition operation of the two obtained inputs A0 and A1 from stage 1 and B1 is obtained by performing the subtraction operation of the same value of A0 and A1. The same operation can be performed for the following values of B2 and B3 which is obtained by performing the addition and subtraction operation of A2 and A3 from stage1. Similarly B4, B5, B6, B7 is obtained in a similar way with the inputs A4, A5, A6, A7 respectively. The output of stage2 is then applied as the input to stage.

In case of pre final stage3, the complex coefficients $W_N{}^K$ are multiplied with B3 and B7 (obtained from stage2) to generate the output. Such complex coefficient which is also known as "twiddle factor or phase factor" is denoted as W_N^K and it is calculated using the formula as shown below.

$$W_N = e^{-j2\pi/N}$$

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Third stage yield C0 is produced by thinking about the data sources w21 and w25 by playing out the expansion activity. The complex coefficients is duplicated with w27 and afterward the increased worth is added with w23 to deliver C1 yield (third stage yield). After that similar data sources w21 and w25 will create C2 by performing subtraction activity. In like manner the sources of info acquired from stage2, for example, w27 and w24 will produce C3 as yield while doing subtraction activity.

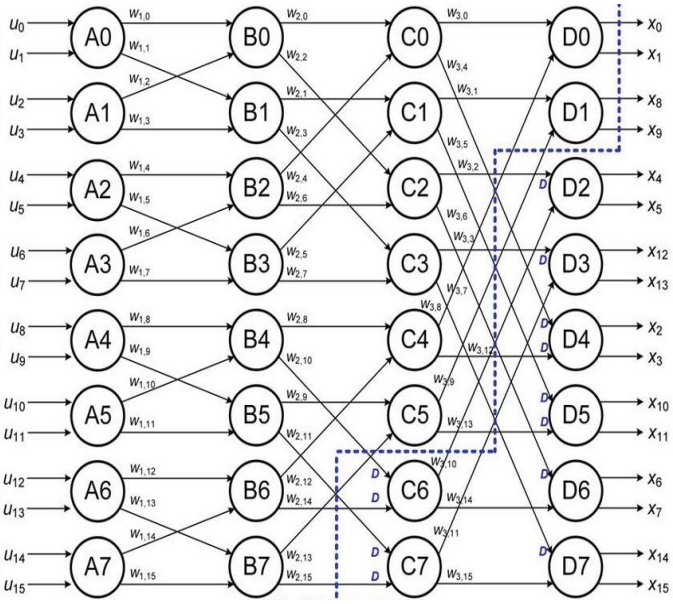


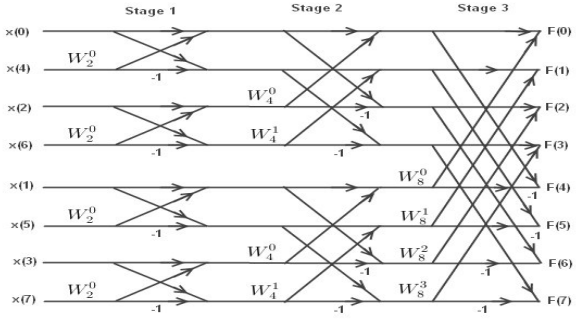
Figure 2: Polar Encoding flow0graph

The activity acted in initial four information data bits for example, B0,B1,B2,B3 is rehashed by the accompanying next four data bits signified as B4,B5,B6,B7 and produce the yield data bits C4,C5,C6,C7 individually. Since the coefficients is of complex worth, the yield is additionally seen as a complex worth (i.e) it comprises of both genuine and fanciful values.

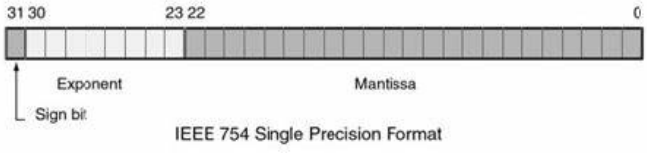
And, in the last stage, W_N^8 is taken as mind boggling coefficients that are increased to create the comparing yield. Here, consider the estimation of W_8^0 as 1, W_8^1 as 0.707-j0.707 and essentially consider j as an incentive for W_8^2, - 0.707-j0.707 as a worth for W_8^3. Finally, the last yield D0 is encoded by performing the expansion activity of C0 and acquired estimation of C4 (which is produced by increasing C4 with W_8^0). Correspondingly for ascertaining D1, C5 and C1 will be included yet with various complex coefficient W_8^1. At that point the duplicated estimation of C6 with its intricate coefficient W_8^2 and C2 bits are added to deliver the ideal incentive for D2. Comparative activity is rehashed to produce D3.And for the following four data bits, the duplicated estimation of C4 and its intricate coefficient is subtracted with C0 to get the incentive for D4. By executing the abovementioned activity the comparing yield bits D5, D6 and D7 is gotten. The different yields are gotten at each middle stage also, it is put away in a register for next stage handling. At long last, the yields are gotten in somewhat turned around request and it guarantees the security of the data. This is known as encoding process and the whole turn around process is done at the beneficiary to recover the first data.

IV. PROPOSED METHOD:

In order to increase the range and accuracy of the results in existed method and also to reduce the delay IEEE 754 floating point multiplier is implemented instead of normal multiplier used in the existing method.



A multiplication of two floating-point numbers is done in four steps: • non-signed multiplication of mantissas: it must take account of the integer part, implicit in normalization. The number of bits of the result is twice the size of the operands • normalization of the result: the exponent can be modified accordingly • addition of the exponents, taking into account the bias • calculation of the sign. The output of this encoder is difficult to get hacked and thus increases the security of the information.This proposed work is implemented in Modelsim 6.4a and it is synthesized by Xilinx13.1. The maximum combinational path delay for the proposed system is 26.801ns. The total memory used for the whole process is 269968 kilobytes.



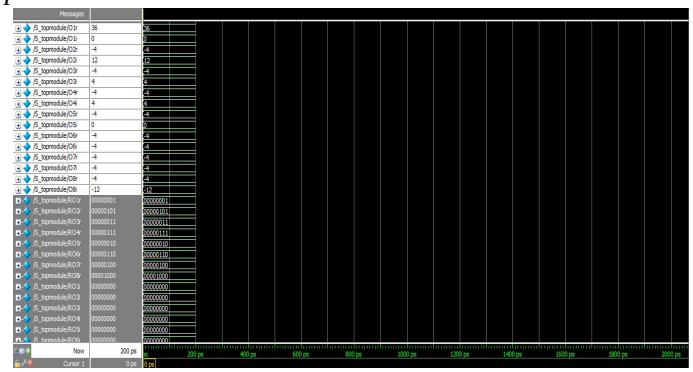
IEEE 754 Single Precision Format

Synthesis Report

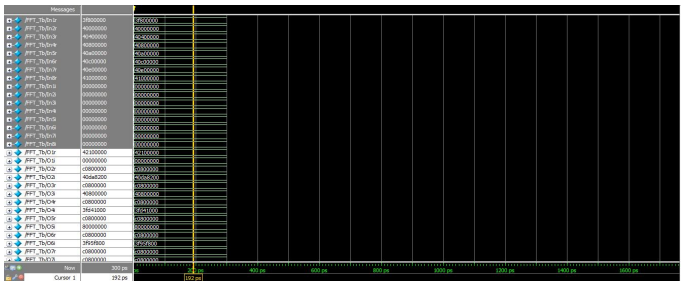
LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION(%)
Number of Slices LUTS	990	990	100
No of Bonded IOBs	512	512	100

V. EXPERIMENTAL RESULTS

A. *Encoder Using Normal Multiplier*



B. *Encoder Using FP Multiplier*



VI. CONCLUSION

The encoding unpredictability ought to be considered while transmitting the data bits securely. The complexity can be changed based on time. The multifaceted nature shifts in view of the information sources. So as to defeat such complexities, in our proposed work the info is checked before encoding the data bits thus the memory necessity is seen as diminished. This thus accelerates the exhibition. The tradeoff as far as its dormancy is additionally diminished. But the round off in the FP multiplier tends to affect the accuracy. It also improves safety of the transmitted information. The execution is done utilizing Model Sim 10.4a.

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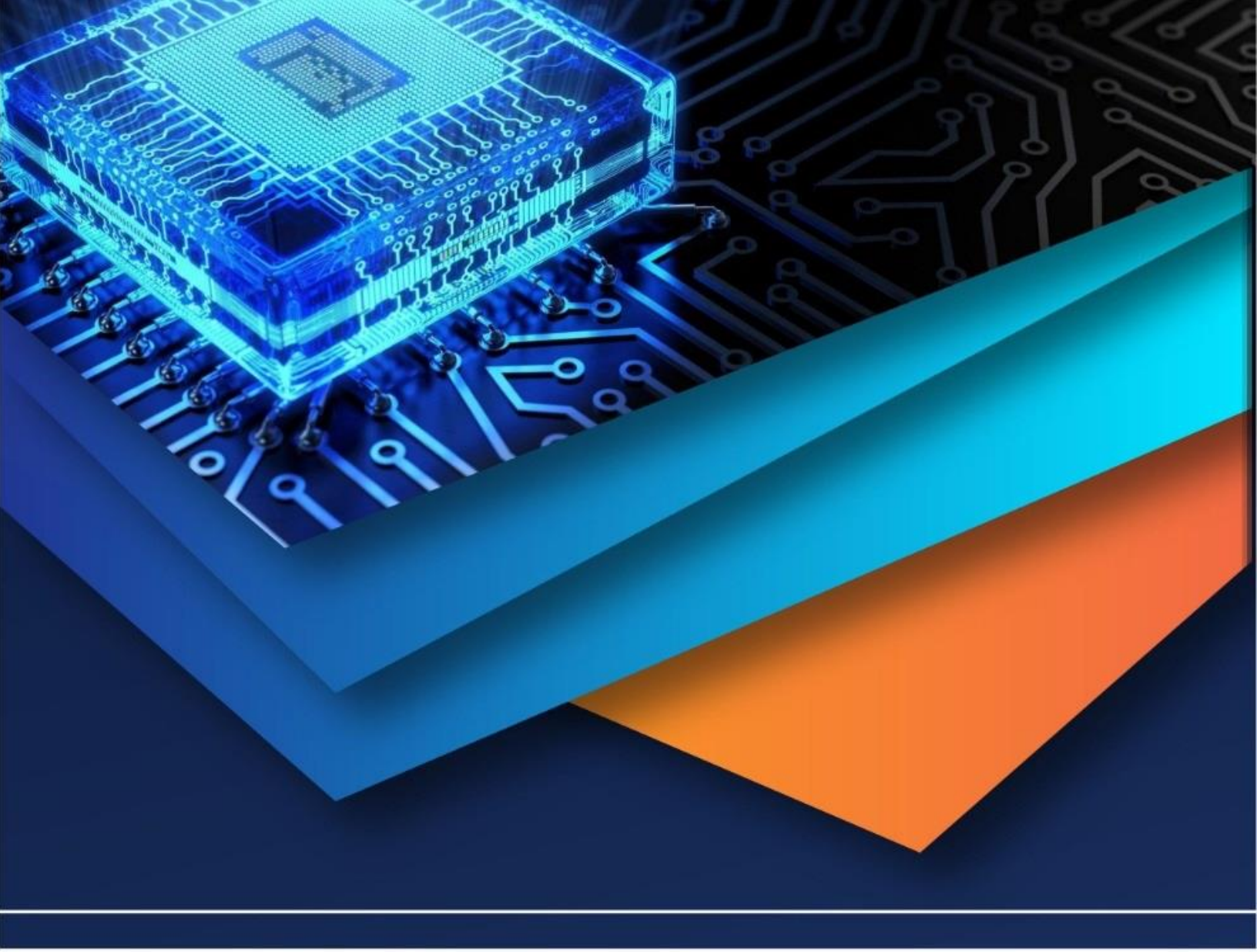

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