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Design of Efficient Adders and Subtractors based on Quantum Dot Cellular Automata (QCA)

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Abstract: ***Compatibility of a design is an archetype of three aspects, namely speed, power, and area. Achieving all three of them is exceptionally desirable. Quantum-dot Cellular Automata is one of the most surrogate nanotechnologies in the electronics industry. Being a low power utilizer, a high-speed operator, and Nano-size when it comes to the fabrication process, it has its own leverages. Quantum-dot Cellular Automata cells are assimilated in wires and logic gates as a fundamental building block of nanoscale digital circuits. Implementing QCA circuits with the help of the XOR gate, the circuit can be made simpler in delay and cell count. In this paper we propose our designs of basic digital circuits such as adders and subtractors by utilizing QCA technology with estimation of its energy dissipation. These designs are focused to reduce cell count, area consumption and delay as compared to the earlier and existing designs. All the designs are simulated with the help of QCA Designer software provided by Walus Lab at the University of British Columbia. The energy dissipation of designed circuits are calculated using QCA Designer-E software developed at the University of Bremen.***
Keywords: QCA, Quantum dot cellular automata, XOR, adders, subtractors

I. INTRODUCTION

Quantum Dot Cellular Automata (QCA) is a contemporary nanotechnology introduced by Lent et al. [7] to integrate quantum dots into classic cellular automata. The term quantum dot cellular automata has been coined in such a way that it is distinguishable from models of cellular automata performing quantum computations. In QCA, circuits are fabricated with the help of quantum cells. In the classical model, every cell encompasses four quantum dots with two electrons. Semiconductors such as InAs and GaAs are incorporated to forge nanoscale Quantum dots. Transmission of information is accomplished when a polarization state undergoes propagation instead of current in QCA realization. QCA is a progressive innovation that conceivably conquers the inescapable scaling issues of current CMOS based circuits in performing calculations. A portion of the benefits of Quantum Dot Cellular Automata (QCA) innovation incorporates low-power dissipation with high operating speed and device density. Interestingly, the large-scale manufacturing of nanosized QCA innovation is troublesome. Moreover, QCA innovation is inclined to high blunder rates which happen because of the scaffolding, dislodging, misalignment, and cell exclusion defects. Furthermore, QCA circuits and gadgets are likewise defenceless against transient issues which are incited by thermodynamic impacts, radiation, and other impacts. These errors and faults can be minimized with precision and efficiency in design and also by coplanar layering.

Since the introduction of QCA technology in 1993, various QCA based logical designs such as reversible logic circuits, multiplexers, memory cells, ALUs have been introduced. However, only a few QCA based adders and subtractors have been proposed so far. In this paper, an innovative design adders and subtractors are introduced. Simulations using QCA-Designer and QCA-Designer-E supports all the results presents. All the presented designs are compared to existing designs on the basis of cell count, area, delay and energy dissipation.

II. BACKGROUND OF QCA

A. QCA Fundamentals

QCA is commonly simulated as computer programs. But, Lent et al. [7] in 1993 expressed a solid usage of an automata using quantum-dots encapsulated within cells. It picked up prominence quickly, and it was then originally manufactured in 1997. The discrete idea of both cell automata and quantum mechanics were consolidated by Lent [7], to make nanoscale gadgets which are equipped for accomplishing calculation at extremely high exchanging speeds (request of Terahertz) and insignificant power utilization. Quantum innovation is presently step by step applied in different fields. QCA technology depends on the exchange of bi-stable called holes. Quantum cells developed from four quantum dots is portrayed in Fig. 1. [8][9]. The quantum cell is stacked with two free electrons that can tunnel between neighbouring quantum dots. These electrons will, in general, involve antipodal destinations in light of their shared electrostatic repulsion. In this way, there are two most stable arrangements for both the electrons as demonstrated in Fig. 2, yet it is noticed that no current is steered through the cell. These arrangements are termed as cell polarization P=+1 and P=-1; these two cell polarizations represent ”1” and ”0” respectively [10][11].

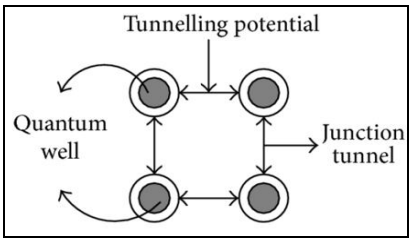

Fig. 1. Quantum-dot Cell

Dissimilar to standard electronics, where current is used to transmit information, QCA works by the intercellular Coulombic interaction hat associates the condition of one cell to one of its neighbours, which then results in data transfer.

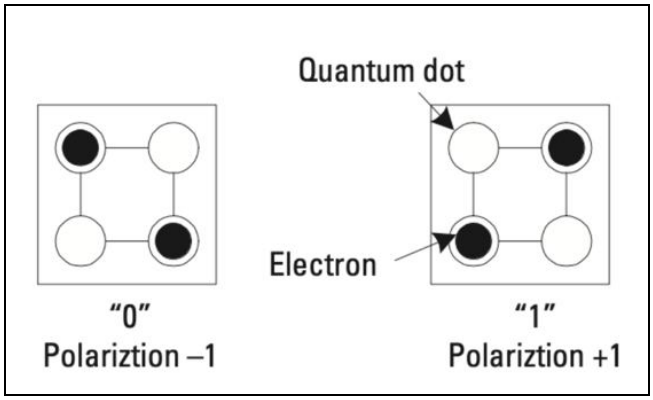

Fig. 2. Polarization in QCA

B. QCA Basic Gates

The most common among all primary logic gates in QCA is the majority voter (MV) or majority gate. It is formed by connecting five QCA cells in. The underlying function in the majority voter is shown in Fig. 3 and logic operation is shown in equation (1).

$$M(x, y, z) = xy + yz + xz \qquad (1)$$

By fixing any one input of majority voter permanently to 0 or 1 logical AND and OR function can be implemented. Another basic gate inverter in QCA is shown Fig. 3.

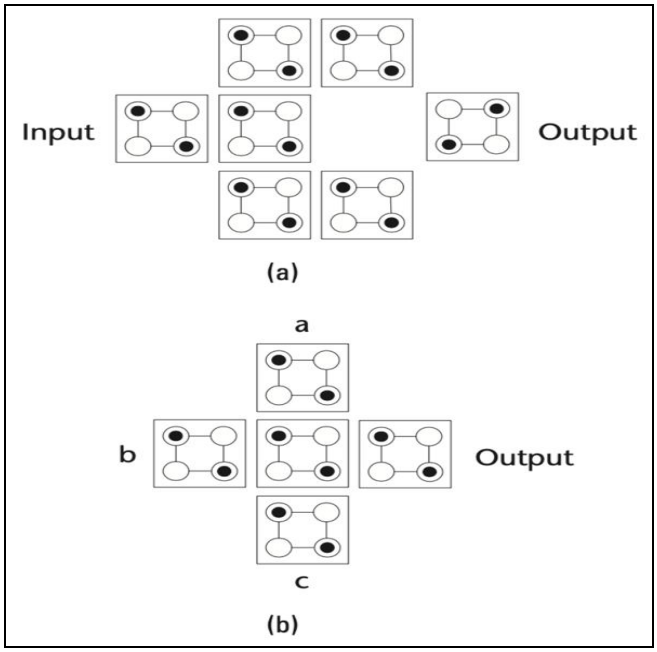

Fig 3. (a) QCA Inverter (b) QCA Majority Gate

C. QCA Clocking

Four distinct and periodical timing states achieve QCA clocking. A QCA circuit is divided into zones which are maintained in a phase. QCA requires a 4-phased clocking signal, termed as a quasi-adiabatic switching technique, which is created by CMOS wires or Carbon Nanotube (CNT) embedded underneath the QCA hardware for adjusting the electric field in cells [12], [13]. Four stages are named as Relax, Switch, Hold and Release [14], [15]. In the first phase the actual computation takes place; therefore, the barrier potential between holes is slowly raised, and a cell under the influence of its neighbours attains an absolute polarity. The barriers are kept raised, during the second phase, and a cell pauses its polarity. In the third stage, boundary potential is diminished bit by bit, and a cell losses its polarity. Finally, in the last phase, the cell remains un-polarized because of the absence of an inter-dot barrier. The Figure 5 shows four stages of a clock signal and the barrier potential at every stage. Each of the four clock signals are consistently 90 degrees out of phase with the earlier clock. Suppose if a level wire comprised of, 10 cells, and each back to back pair, beginning from the left were to be associated with each continuous clock, information would normally flow from of left to right. The first pair of cells will remain polarized until the second pair of cells gets polarized, and so on. In this way, information flow is controlled by clock zones.

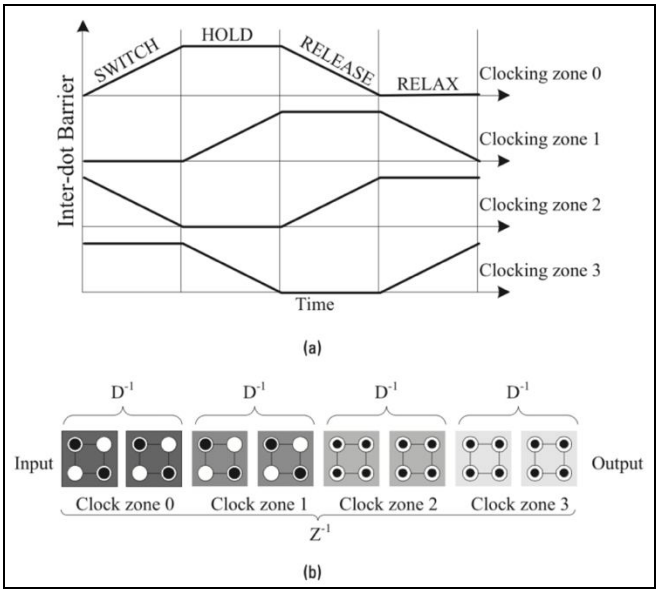

Fig. 4. (a) Four clocking signals (b) A clocked QCA wire

III. QCA XOR Gate

Universal gates such as NAND and NOR and basic logic gates such as NOT, AND, and OR are required to design digital electronic structures. Moreover, of these basic and universal gates, exclusive gates such as Exclusive-OR and Exclusive-NOR gates are also utilized to design advanced digital circuitry. The expression for an XOR gate can be observed in Equation (2).

$$A \oplus B = AB' + A'B \qquad (2)$$

In computation and digital electronics, an XOR is a coherent value relying upon the two information sources, and the logical output of XOR is accurate if the odd number of inputs are true; in any other case, the output is false. This forges a fundamental logic gate.

TABLE I. XOR input and output vectors

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

In [16], the XOR design proposed by the authors comprises of 13 cells with a utilization area of 0.012m2. In [17], the authors have introduced a robust exclusive-OR gate. This proposed gate consists of 28 cells with an area of 0.02 μm^2. They utilize fixed polarization cells with a five-input majority in their design. In [18], the authors presented a design consisting of 36 cells with a utilization area of 0.030 μm^2, and a delay of 0.75. Their design is based on coupled majority voter minority gates (CMVMIN). The authors in [19] introduced an XOR design consisting of 37 QCA cells along with a utilization area of 0.030 μm^2, and latency of 1 clock cycle. Another brilliant design of the XOR gate has been introduced by Baharetal et al. in [20], where they reduce the number of cells and area consumption drastically. Their design comprises of only 12 cells with a utilization area of 0.02 μm^2 and a delay of 1.25. In [21], the authors design an XOR-based on interactive cell arrangement. Here, no majority of gates are used to achieve the design. Both the data sources are outside of the circuit, and the yield is additionally outside of the circuit. The QCA configuration is reduced to just 9 cells with a utilization area of 8868.30 nm^2, or 0.01 μm^2, and a delay of 0.5, which is least among the circuits discussed above. This XOR proposed is used for designing the adders and subtractors in the next section.

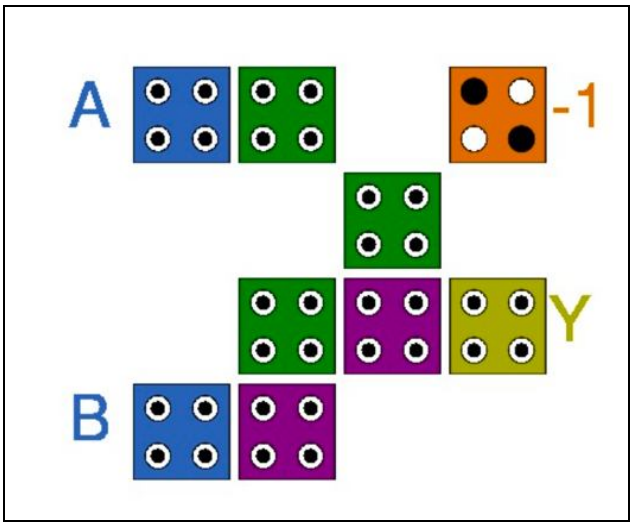

Fig. 5. QCA Layout of XOR gate

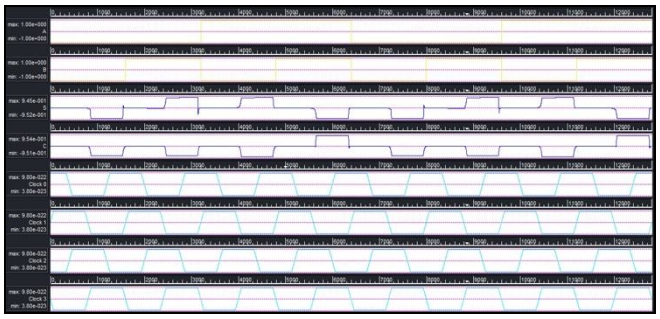

Fig. 6. Simulation outcome of XOR gate in [20]

IV. PROPOSED DESIGNS BASED ON QCA

A. Half Adder

Half adder is a combinational logic circuit that adds two digits and produces a sum (S) bit and a carry (C) bit as output. The design of a half adder includes one XOR gate and one AND gate. The XOR gate used in this design is proposed by [21].

The design layout of half adder is shown in figure 7. Our design consists of only 17 cells and circuit area is 24307.76 nm^2 . The simulation results of half adder circuit is shown in figure 8. The logic implementation of half adder sum and carry can be represented as in equation 5 and 6 respectively

$$Sum = A'B + AB' = A \oplus B \quad (5)$$

$$Carry = AB \quad (6)$$

Table II. Half Adder input and output vectors.

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

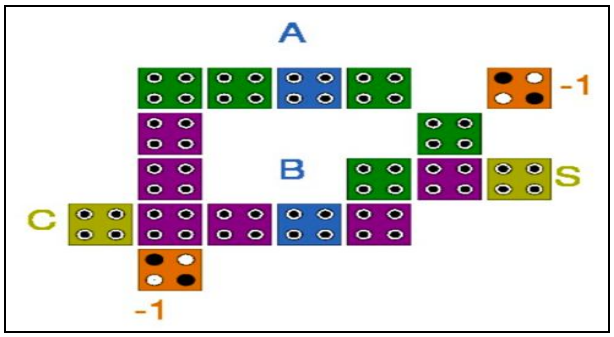

Fig. 7. Half Adder QCA Layout

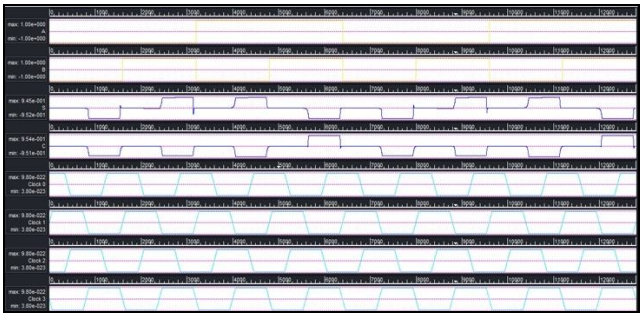

Fig. 8. Half Adder Simulation Outcomes

B. Full Adder

Full adder is a combinational logic circuit that adds three inputs and produces a sum (S) bit and a carry (C) bit as output. The design layout of full adder is shown in Fig. 9, which is implemented by one XOR gate and one majority voter. Using our previously designed XOR gate in QCA we now design a full adder. The design consists of only 32 cells and circuit area is 39071.46 nm^2. The logic implementation of full adder sum and carry can be represented as in equation 7 and 8 respectively.

$$Sum = (A \oplus B) \oplus C \quad (7)$$

$$Carry = AB + BC + AC \quad (8)$$

TABLE III. Full Adder input and output vector

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

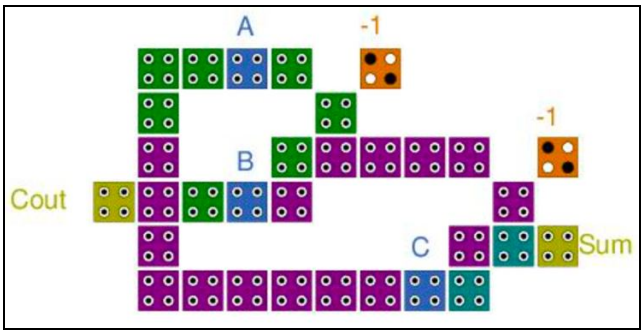

Fig. 9. Full Adder QCA Layout

The simulation results of full adder circuit is shown in Fig. 10. We see a minute latency of 0.5 in the output of Sum, but no latency in Carry.

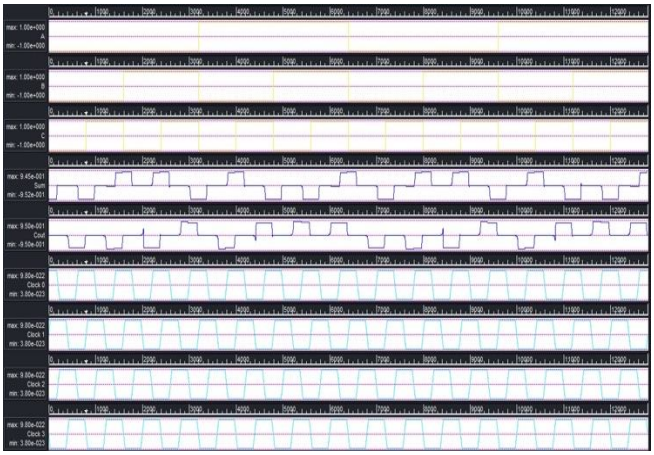

Fig. 10. Full Adder Simulation Outcomes

C. Half Subtractor

Half subtractor is a combinational logic circuit that subtracts two digits and produces a Difference (D) bit and a Borrow (B) bit as output. The design of a half subtractor includes one XOR gate, one AND gate and one NOT gate. The XOR gate used in this design is our proposed XOR which makes the circuit compact.

The design layout of half subtractor is shown in Fig. 11, which is implemented by one XOR gate and one AND gate.

The design consists of only 16 cells and circuit area is 29612.86 nm^2. The simulation results of half subtractor circuit is shown in Fig. 12. The logic implementation of half subtractor Difference and Borrow can be represented as in equation 9 and 10 respectively.

$Difference = A'B + AB' = A \oplus B$ (9)

$Borrow = A'B$ (10)

TABLE IV. Half Subtractor input and output vectors

Input		Output	
A	B	Diff	Borr
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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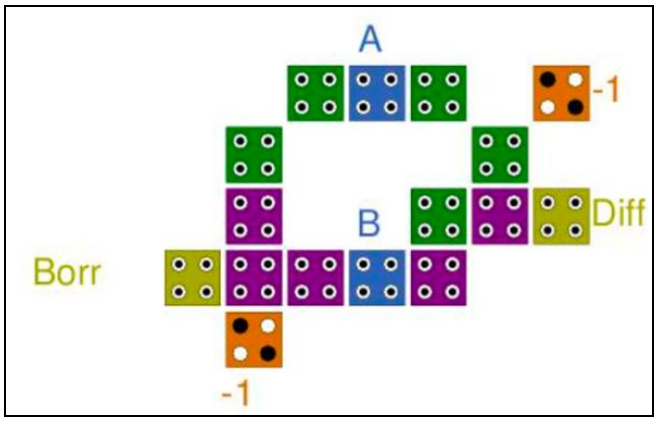

Fig. 11. Half Subtractor QCA Layout

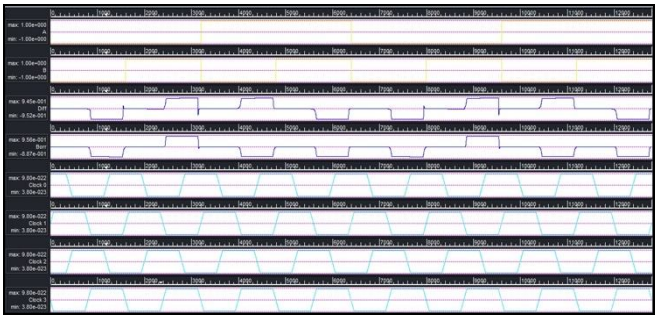

Fig. 12. Half Subtractor Simulation Outcomes

D. Full Subtractor

Full Subtractor is a combinational logic circuit that subtracts three inputs and produces a Difference (D) bit and a Borrow (B) bit as output. The design layout of full subtractor is shown in Fig. 13, which is implemented by one XOR gate, one majority voter and one inverter. Using our previously designed XOR gate in QCA we now design a full subtractor. The design consists of only 32 cells and circuit area is 40138.16 nm^2. The simulation results of full subtractor circuit is shown in Fig. 14. The logic implementation of full subtractor difference and borrow can be represented as in equation 11 and 12 respectively

$$Difference = (A \oplus B) \oplus C \quad (11)$$

$$Borrow = A'B + BC + A,C \quad (12)$$

Table V. Full Subtractor input and output vector

Input			Output	
A	B	C	Diff	Borr
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

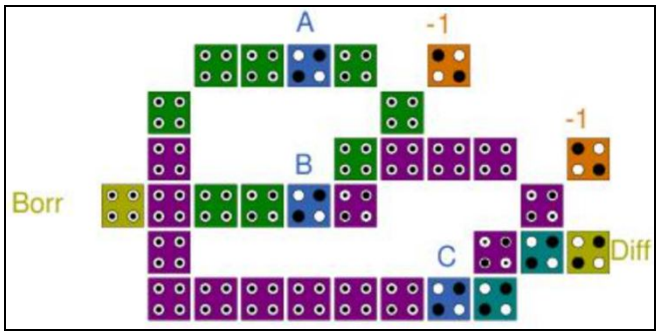

Fig. 13. Full Subtractor QCA Layout

The simulation results of full subtractor circuit is shown in Fig. 14. We see a minute latency of 0.5 in the output of Difference, but no latency in Borrow.

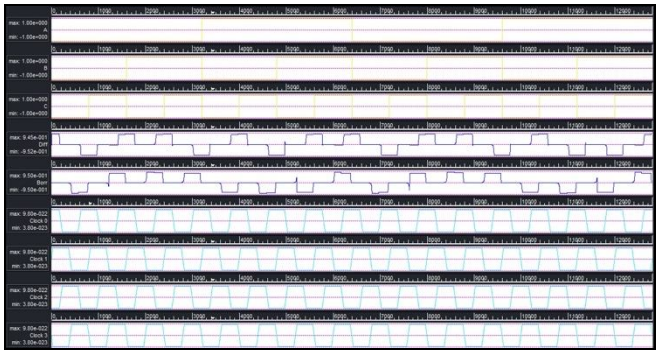

Fig. 14. Full Subtractor Simulation Outcomes

V. COMPARITIVE STUDY OF PROPOSED CIRCUITS

In this section, efficiency of the proposed structure are assessed by comparing their cell counts and area usage with those of existing designs. The results obtained after simulations done in QCADesigner ver. 2.0.3.In this study, we implement a compact design of half adder, full adder, half subtractor and full subtractor with fewer cells and less used area. The complexity parameters such as cell count, area consumption of the QCA circuit have been calculated with the help of QCA Designer 2.0[22]. Energy dissipation parameters have been calculated using QCADesigner-E software developed at the University of Bremen[23].

A. Specifications Of Our Designs

In this subsection we present the specifications of our proposed circuits. The specifications include complexity parameters such as cell count, area consumption and energy dissipation parameters such as Sum_Bath which is the total energy dissipation of the circuit.

Table VI. Design specification of proposed circuits

Circuit	Cell Count	Area (nm2)	Delay	Sum_Bath
XOR[21]	9	39457.41	0	1.84e-002 eV (Err:1.86e-003 eV)
Half Adder	17	24307.76	0	1.94e-002 eV (Err: 2.08e-003 eV)
Full Adder	32	39071.46	0.5	2.91e-002eV (Err: 3.04e-003 eV)
Half Subtractor	16	29612.86	0	1.94e-002 eV (Err: 2.10e-003 eV)
Full Subtractor	32	40138.16	0.5	2.63e-002eV (Err: 2.74e-003 eV)

B. Comparison of Full Adders

TABLE VII. Comparison of QCA full adders

Author	Cell Count	Area (um2)	Delay
[1]	93	0.09	5
[2]	59	0.043	4
[3]	41	0.03	4
[4]	82	0.07	1
Proposed	32	0.02	0.5

TABLE VIII. Energy dissipation parameter comparison of full adders

Author	Sum_Bath (eV)	Avg_Bath(eV)
[1]	3.52e-02 (Err: -3.08e-03)	3.20e-03 (Err: -2.80e-04)
[2]	3.16e-02 (Err: -1.93e-03)	3.97e-03 (Err: -1.75e-04)
[3]	3.00e-02 (Err: -2.87e-03)	2.73e-03 (Err: -2.61e-04)
Proposed	2.91e-002 eV (Err: 3.04e-003 eV)	2.64e-003 eV (Err: 2.77e-004 eV)

C. Comparison of Full Subtractors

TABLE IX. Comparison of QCA full subtractors

Author	Cell Count	Area (um2)	Delay
[5]	136	0.168	5
[6]	52	0.039	4
[7]	233	0.132	4
[8]	272	0.44	1
Proposed	32	0.01	0.5

TABLE X. Energy dissipation parameter comparison of full subtractors

Author	Sum_Bath(eV)	Avg_Bath(eV)
[5]	7.46e-02 (Err: -7.27e-03)	6.78e-03 (Err: -6.61e-04)
[6]	2.28e-02 (Err: -2.26e-03)	2.07e-03 (Err: -2.05e-04)
[7]	4.91e-02 (Err: -3.80e-03)	4.46e-03 (Er: -3.45e-04)
[8]	6.35e-03 (Err: -6.97e-04)	5.77e-04 (Er: -6.33e-05)
Proposed	2.63e-002 eV (Err: 2.74e-003 eV)	2.39e-003 eV (Err: 2.49e-004 eV)

1) *Sum_Bath:* Total energy dissipation
2) *Avg_Bath:* Average energy dissipation per cycle

VI. CONCLUSION

Quantum-dot cellular automata (QCA) is approaching nanotechnology with excellent possibilities to lend tiny circuits with moderate energy dissipation in comparison with CMOS technology. Compact and efficient designs of half adder, full adder, half subtractor and full subtractor have been presented in this paper. It uses less area and energy dissipation using XOR gate and majority gate as a raising block. Implemented circuits were reproduced and validated by employing the QCADesigner tool version 2.0.3 [22]. An analogy of several similar circuits, cell count, area and energy dissipation was discussed in this paper. The comparative study confirms that the designed QCA circuitry has improvement analyzed to other prevailing ones.

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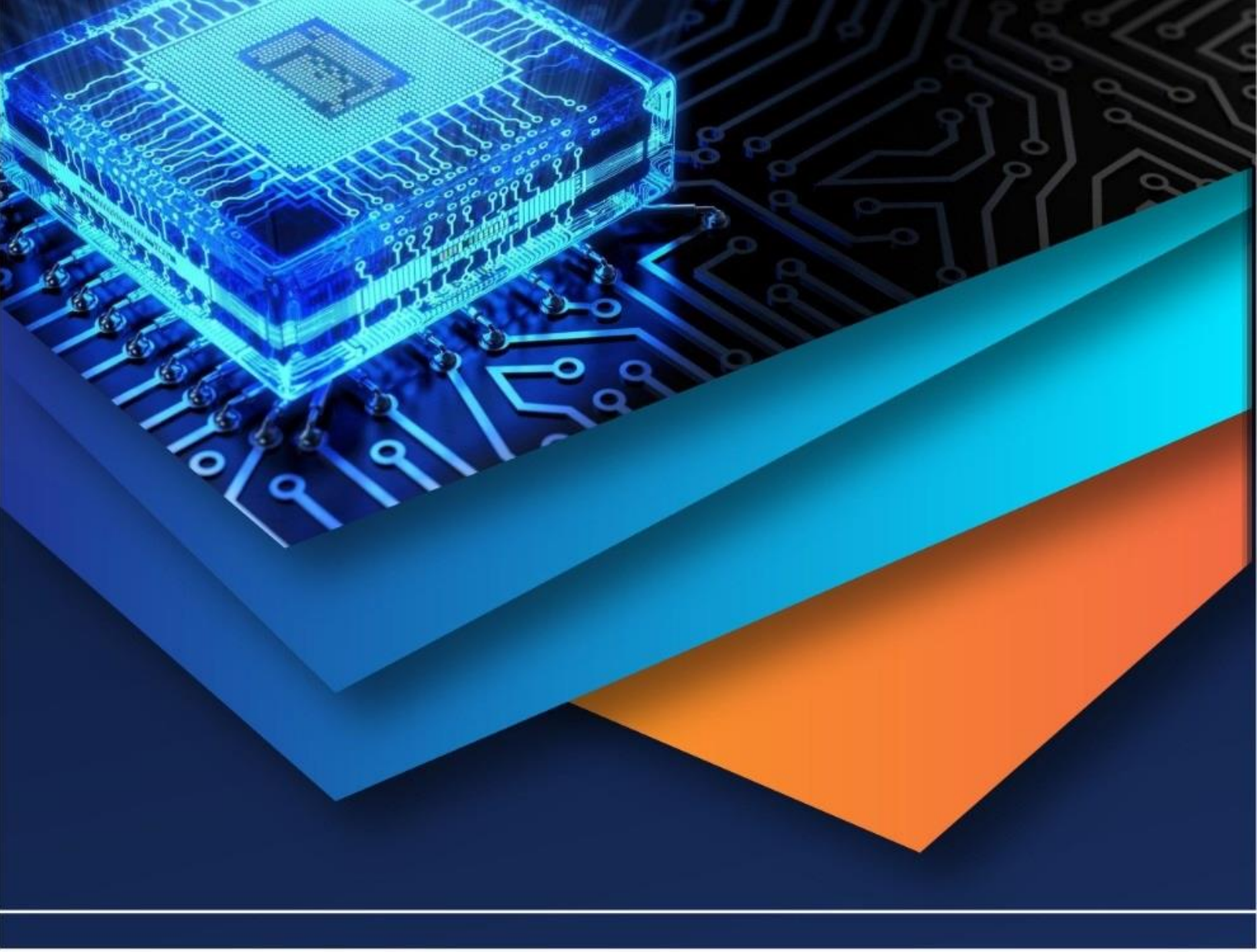

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