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A Novel Design of Low Power Comparator through Differential Amplifier in 90nm CMOS Technology Using Cadence Tool

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Abstract*— In digital world, Speed, area, power are very vital parameters for high speed devices like analog to digital converters. The comparator circuit with preamplifier increases the power consumption, as it requires large amount of currents than the latch circuitry. In this paper, a novel design of low power comparator is explained, which is able to provide high speed, and the low power using cross coupled differential amplifier in the latch stage in 90nm CMOS technology. The comparator is designed using cadence tool with 1.2 V DC power supply in 90nm CMOS technology. The power consumption of the proposed comparator is 0.8121uW which is very convenient for making high speed devices.
***Keywords*— ADC, Comparator, Differential amplifier, Dynamic Latch**

I. INTRODUCTION

A. Comparator

Analog-to-digital converter has become a important element driving the semiconductor industry over the last few years. Expanded integration of different functional blocks in a single chip makes analog to digital converters more conventional and they are capable to provide high speed as well as low power consumption [1][4]. Comparators are called as 1-bit ADC converter and because of that they are widely used in large amount in ADC converter. In the ADC conversion method, it is compulsory to first sample the input signal then this sampled signal is applied to a combination of comparators to find the digital alternative of the analog signal.

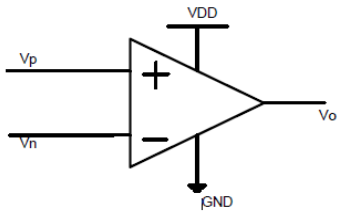


Figure.2. Symbol of Comparator

The basic symbol of the comparator is shown in above figure 2. The comparator is a decision making circuit. The basic property of a CMOS comparator is used to realize whether an input signal is greater or smaller than reference signal and results a binary signal based on comparison at the output stage [5][9]. If the input signal is greater than reference signal then the output of the comparator is logic '1' and the input signal is less than reference signal then the output of the comparator is logic '0'.

1) CHARACTERISTICS OF COMPARATOR

a) Static Characteristics: i) Gain

Gain of a comparator can be expressed as:

$$\text{Gain (AV)} = \lim_{\Delta V \to 0} [(VOH - VOL)/\Delta V]$$

Where ΔV= input voltage range

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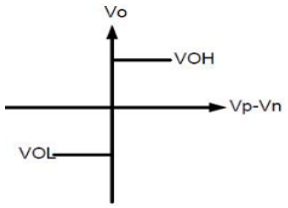


Figure.3. Ideal Characteristics of Comparator

b) Offset Voltage: If the input voltage difference crosses zero then the output changes. If the output did not change until the input difference reached a value +Vos then this difference is called as offset voltage. It is not a problem, it could be predicted but it varies randomly from circuit to circuit. The input offset voltage is applied between two input terminals to balance the amplifier and the output offset voltage is defined as the dc voltage present at the output terminal of the comparator when the two input terminals are grounded.

c) Input Resolution: It is the input voltage change which is sufficient to make output swing to valid binary states.

d) Noise: Noise of a comparator is modeled if the comparator were biased in the transition region. Noise leads to an uncertainty in the transition region which causes jitter.

e) Input Common Mode Range(ICMR): ICMR can be defined as the range of input voltage for which the comparator functions normally & meets all required specifications.

2) *Dynamic Characteristics:* The dynamic characteristics of the comparator comprise both small and large signal behaviour. At this point we do not know how the comparator takes to respond to the differential input.

a) Propagation Delay: The characteristics delay between input and output state is the time response of the comparator and this difference between input signal and output signal called as propagation delay.

It can be calculated as:

Propagation time delay= (Rising Propagation Delay time +Falling Propagation Delay Time) /2

b) Slew Rate: Rate of change of output voltage with respect to time is called slew rate. If the rate of rise and fall of a comparator becomes very large, the dynamics may be restricted by the slew rate.

C) Speed: It is the inverse of the Propagation delay.

Speed=1/propagation delay

II. RELATED WORK

Ili shairah abdul halim et al. [10] proposed the design and analysis of dynamic latch comparator using charge sharing topology for high speed and low power consumption. This design has focused on the reduction of delay and the power consumption of the comparator that improves the comparator performance. This design is implemented in 180nm technology with 1.8 V power supply using SILVACO tool. The average dynamic power dissipation is reduced approximately 94% and minimized the delay approximately 11%. Their proposed design of the comparator runs faster and provides more stable output signal than the previous work with low power voltage. Dhanisha N. Kapadia et al. [8] proposed dynamic latch comparator along with the output buffer in 130nm and 90nm technologies with 1.3 V and 0.9 V power supply respectively. The result shows the speed of 1.33GHz and 0.47GHz was executed and the power consumption is 4.89mW and 162.32mW in 90nm and 130nm cmos technologies respectively. Masoume Akbari et al. [7] presented rail to rail input high performance regenerative comparator which is suitable for low voltage and low power applications. This topology is proposed to expand the speed of the circuit. This comparator is designed in the 180nm technology with 0.5 V power supply. The propagation delay is 16.4ns and the power dissipation is 20nW. Bo Liu et al. [6] proposed comparator along with rail to rail input voltage range. In this technique 0.5um silicon on insulator (SOI) technology with 3.3 V power supply is used. The rail to rail operation is performed using two folded differential amplifiers operating in parallel manner as an input stage. M. Dinesh Kumar et al. [3] proposed a double tail dynamic comparator design through analysis of low power consumption of conventional dynamic comparator. In this paper, an analysis on the delay of the comparator were presented by adding few transistors and the positive feedback during the regeneration is strong which results in reduced delay time. The comparator is designed in 0.18um cmos technology. The average power consumption is 12uW with 7.4ns delay is reduced with 0.8 V power supply. D. Jackuline Moni et al. [9] proposed the comparison between the cmos dynamic latch comparator. The circuit using SPICE tool with 180nm technology and the dc voltage is 1.8 V. In this paper the power consumption of the comparator with inverter is 30% power as compared with the conventional method. Pardeep et al. [4] proposed clocked regenerative comparators. Low power consumption with low delay

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and high speed ADC converter used clocked regenerative comparators for the reduction in delay and power. In this paper the 180nm technology used which shows reduced delay time near about 30% in comparison with conventional double tail comparator.

III.DESIGN METHODOLOGY

A) *Double Tail Dual Rail Dynamic Latched Comparator*

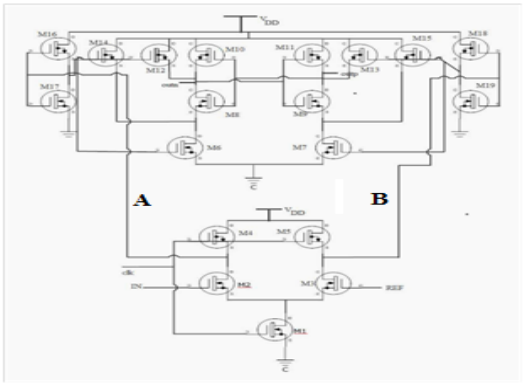


Figure.4. Schematic of double tail dual rail dynamic latched comparator

The schematic of the double tail dual rail dynamic latched comparator is shown in figure 4. The comparator removed the resolved A and B nodes by including an inverter between input and output stages. Because of inverter, weak voltage of A and B node is regenerated and given to the output buffer or post amplifier stage. This comparator shows fast operation and low power consumption as compared to the other comparators design [9].

B) *Proposed Comparator*

The block Diagram of proposed Comparator is shown in figure .5. This circuit primarily is a derived version of the double tail dual rail dynamic latched comparator. The consecutive latch stage is replaced with back to back cross coupled differential amplifier as shown in figure 6. Differential amplifier has such a lot of benefits over the conventional latch that nothing however an inverter. it eliminates common mode noise or in alternative words it has higher CMRR. Another property of differential amplifier is that the increase in maximum higher voltage swings. It additionally provides easier biasing and better linearity. Here the main purpose of the designing the proposed comparator is to reduced the noise that is present in the latch stage and that output is obtaining fluctuated with clock transition.

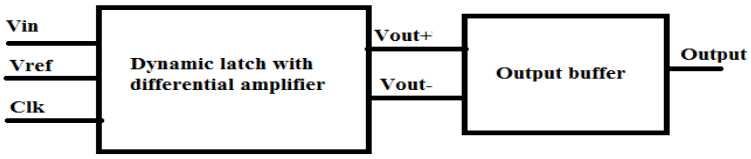


Figure.5. Block Diagram of Proposed Comparator

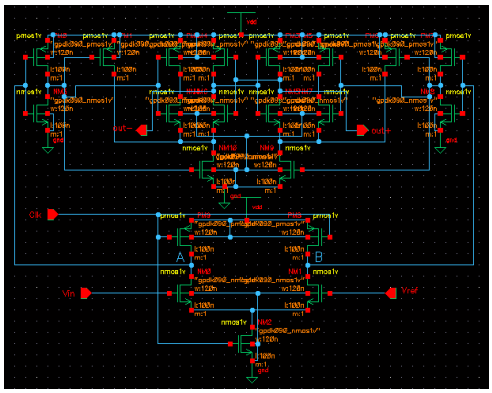


Figure.6.Schematic of Proposed Dynamic Latch

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The operation of the proposed comparator is explained below:

During precharge phase: In this phase Clk=0V, PMOS transistor PM8 and PM9 turn on and they charge A and B node voltages through Vdd. And NMOS transistors NM3 and NM8 are on and discharges A and B nodes voltages to gnd. Then PM1, PM6 and PMOS transistors of differential amplifier PM2 and PM5 turns on, NMOS transistors of differential amplifier NM6, NM5 and NM10, NM9 are off. The out+ and out- nodes are charges through Vdd.

During evaluation phase: In this phase Clk=Vdd, the A and B node capacitances are going to discharge from Vdd to gnd. At a certain voltage of A and B nodes, the inverter pairs PM0/NM3 and PM7/NM8 invert the A and B node voltages into a regenerated voltage. These regenerated voltages turn PMOS transistors PM1, PM2, PM5, and PM6 off. And finally NM10, NM9, NM4, NM7 are on. Hence the back to back cross coupled differential pair again regenerates the A and B node voltages and because of that NM10 and NM9 are on, the output latch stage converts the small voltage difference transmitted from A and B node into digital output.

IV. SIMULATION AND RESULTS OF THE PROPOSED COMPARATOR

A) Input Specifications

TABLE I: INPUT SPECIFICATIONS

Technology	Cadence gpdk 90nm
Supply Voltage(VDD)	1.2V
Input voltage range(VIN)	0V-1V
Reference voltage	0V-0.5V
Clock frequency	1MHz
Clock rise time	1ns
Clock fall time	1ns
Clock pulse width	0.5us
Clock period	1us

The schematic of the proposed comparator drawn in cadence tool is shown in figure 7. and figure 8. shows the transient response of the schematic. In transient response, it is confirmed that output voltage does not get fluctuated during clock transition and it works fine. Input specifications are mentioned in Table 1. The power plot of the proposed comparator is shown in figure 9. which shows the power consumption of the proposed comparator which is very less as compared to the other comparators architectures.

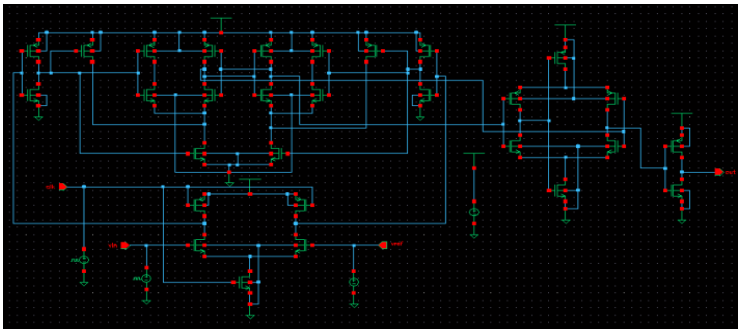


Figure.7. Schematic of Proposed Comparator

B) Transient Analysis

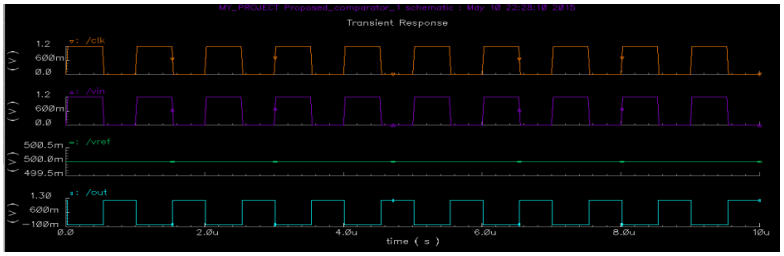


Figure.8. Transient Analysis of Proposed Comparator

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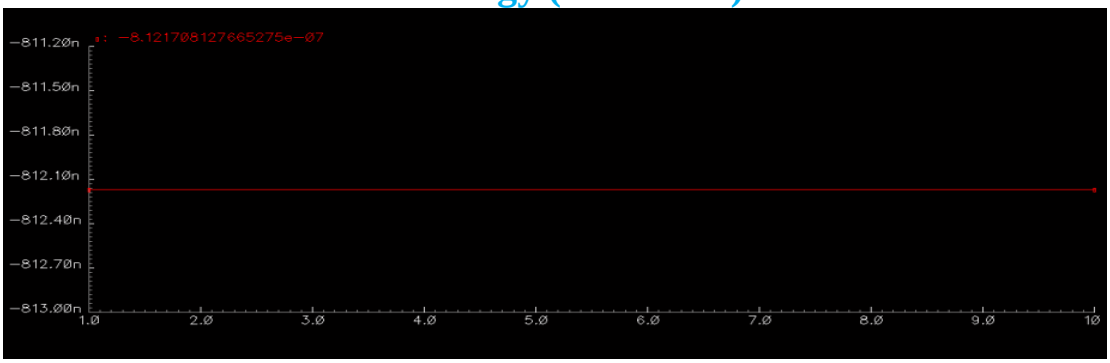


Figure.9. Power Plot of Proposed Comparator

The power, speed and area are very important parameters in the design of flash ADC converter. The proposed comparator is designed using cross coupled differential amplifier replaced with cross coupled inverters to reduce the power consumption. The proposed comparator is designed in 90nm technology using cadence tool with 1.2V power supply consumes 0.8121uW power which is very useful for making the low power flash ADC.

V. CONCLUSION

The comparator is a device for designing the mixed signal system and speed, area furthermore accuracy which is essentially characterized by its energy dispersal and speed is primary variables for high speed applications. The comparator is designed and simulated using cadence 90nm cmos technology. The total power dissipation is 0.8121uW with 1.2V power supply depending upon technology requirement the appropriate design can be chosen which is very useful for designed high speed applications.

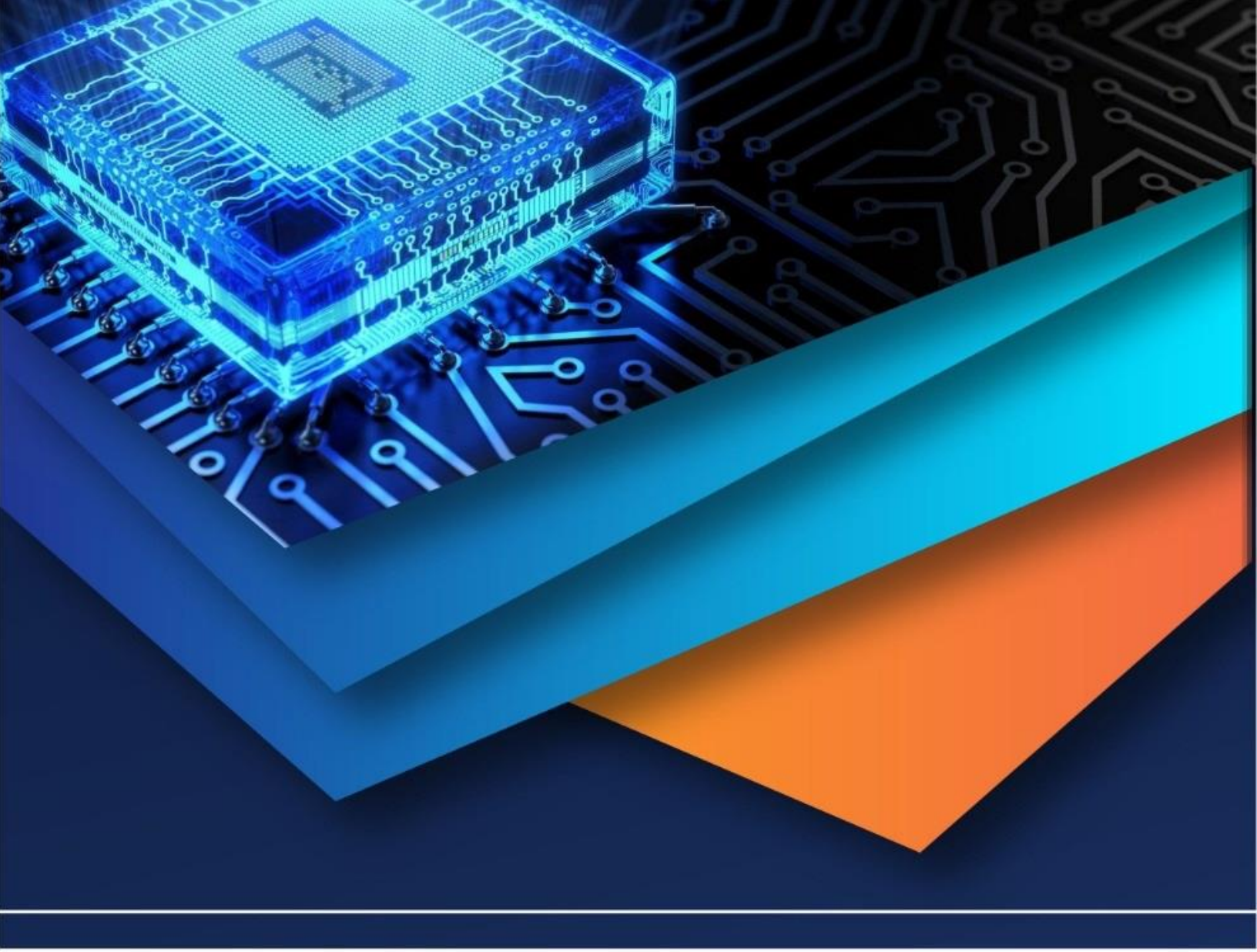
VI. ACKNOWLEDGMENT

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