iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 3 **Issue:** VI **Month of publication:** June 2015

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Fast Protection of Power System Using Pll and Fuzzy Logic Controller

K. Sanath kumar[1], M. Prasad[2]
[1]PG student (E.P.S) [2]Assistant professor, Department of EEE
Narayana Engineering College, Nellore, 524003, JNTUA Ananthapuramu

Abstract— In this paper a new method is proposed that can be used to differentiate faults from switching transients. The method is primarily intended for use in systems where fast fault detection and fast fault clearing before the first peak of the fault current are required. An industrial system, in which high short-circuit power is desired but in which high short circuit currents cannot be tolerated is an example of such a strong power system. A phase-locked loop (PLL) with FLC is used to perform the discrimination. Computer simulations have been performed and it has been demonstrated that the output of the PLL is completely different for a fault compared to a switching transient. This difference can be used for discrimination between a fault and a switching transient. The simulation work has been performed using MATLAB software.

Keywords— Phase Locked Loop (PLL), VCO, Fuzzy Logic Controller (FLC), Clarke transformation, Low Pass Filter.

I. INTRODUCTION

The protection is very much important task in a power system to get uninterrupted power supply. Generally a power system should be protected from abnormal conditions such as faults, transients etc. In power system protection both the fault detection as well as fault discrimination has equal importance. In some type of system the discrimination of fault is very much essential one. The discrimination can be done by various types of techniques such as time domain analysis, wavelet transform, equivalent instantaneous inductance technique, absolute difference of active power technique for discrimination in various equipments as well as in whole power system. Thus the protection of power system is very much essential to avoid the block out of power supply and avoid losses due to the unnecessary power disconnectivity. Strong Power System: The system which has low impedance between source and load and cause very less disturbance to the source during the faults, called strong power system. Most of the industrial systems are strong power systems. They desire high short circuit power to connect and disconnect loads without causing disturbances to sensitive equipment or processes. With the high short-circuit power, a high fault current develops in case there are faults in the system. This high fault current has to be considered when designing the switchgear and other components that build up the power system. This is easily done in new installations but can be problematic when there is a need for higher short-circuit power in an existing system. In these cases, the installation of a fault current limiter could be an alternative to rebuilding the switchgear. The installation of a fault current limiter can also provide the opportunity to make connections in the power system that otherwise would not be possible due to fault currents that exceed the rating of the switchgear. Power system protection is another important issue. It is essential for safe operation of the power system that faults are detected and cleared automatically in a fast and reliable manner so that the operation of the power system is not disturbed. A typical fault protection system is built from circuit breakers (CBs), protection relays, and primary transducers, such as voltage and current transformers and auxiliary equipment. There are many methods and algorithms available to detect short-circuit current in a power system. One simple (but yet efficient) method is to estimate the current from measured current samples. If the magnitude of the estimated current is larger than a predetermined threshold it is assumed that a fault has occurred (magnitude relay). The estimation of the current can be performed using several different techniques, such as, for example, by calculating the root mean square (rms) value, or by a Fast Fourier transform (FFT) method, or by a least-square (LSQ) method. The accuracy of the estimation and the amount of information that is available for the estimation are correlated. In general, if more information is available, the estimation will become more accurate. On the other hand, if faster fault detection is required, the estimation becomes less accurate since less information is available. Even though the detection of faults is the primary concern for fault protection devices (dependability), the ability to distinguish between a fault and a switching transient (security) is also important. Switching transients can, under certain circumstances, give rise to high currents, which are much larger in magnitude than normal load currents. In existing relay protection, capacitor energization and transformer energization have been detected by analyzing the measured current to find certain characteristics of the two types of current

©IJRASET 2015: All Rights are Reserved

transient. A current transient caused by a transformer energization typically contains a superimposed dc component and a superimposed second harmonic component. A current transient caused by a capacitor energization typically contains higher frequency harmonic components. The harmonic components in the measured current can be identified with Fourier-based methods, but that typically requires more time. So to minimize the fault discrimination time PLL logic has been applied as a proposed algorithm. A large number of papers were referred for the implementation of fault discrimination technique in power system and many papers were referred for the implementation of PLL for the desired action. In [6], a new method proposed for high-precision positioning servomechanisms. The servo controller uses a two-phase-type phase-locked loop (PLL) to detect position tracking error and speed fluctuation with high resolution. Because the two-phase-type PLL has a wide frequency range and high noise suppression performance. In [17] – [19], a novel synchronization algorithm robust to grid faults. The novelty of the proposed Phase Looked Loop system consists in the employment of a repetitive controller to eliminate the unbalance effect when this exists in the grid voltages. Analogies and differences with the conventional PLL system have been highlighted. In [20], a new synchronization method which employs an enhanced phase-locked loop (EPLL) system. The operational concept of the EPLL is novel and based on a nonlinear dynamical system. As compared with the existing synchronization methods, the introduced EPLL-based synchronization method provides higher degree of immunity and insensitivity to noise, harmonics and other types of pollutions that exist in the signal used as the basis of synchronization. In [9], Operation of a three phase-phase locked loop-system under distorted utility conditions is presented. In [7], Analysis and design of a phase-locked loop (PLL) is presented for the power factor control of grid-connected three-phase power conversion systems. The dynamic characteristics of the closed loop PLL system with a second order are investigated in both continuous and discrete-time domains, and the optimization method is discussed.In [8], Phase-Locked Loop (PLL) systems have been used in several equipment used in power conditioning applications.In [15], A three-phase phase locked loop (3-Φ PLL) for control and protection in power system applications is presented. The 3- Φ PLL is a frequency adaptive digital system that consists of a positive sequence detector and a single-phase predictive phase locked loop (PPLL). The 3-Φ PLL is fully adaptive in extracting frequency, amplitude, and phase angle in time variant systems. and disturbances. The 3- Φ PLL is implemented on a field programmable gate array (FPGA).In [24], a new high-resolution interpolator for incremental encoders based on the quadrature phase-locked loop method proposed by Emura. The paper [3] , presents the analysis and software implementation of a robust synchronizing circuit, i.e., phase-locked loop (PLL) circuit, designed for use in the controller of active power line conditioners.The fundamentals of the PLL circuit are discussed. It is shown that the PLL can fail in tracking the system voltage during startup under some adverse conditions. Moreover, it is shown that oscillations caused by the presence of sub harmonics can be very critical and can pull the stable point of operation synchronized to that sub harmonic frequency. Oscillations at the reference input are also discussed.In [2], various applications of a nonlinear adaptive notch filter which operates based on the concept of an enhanced phase-locked loop (PLL).

II. PROPOSED POWER SYSTEM

The test system, as shown in Fig. 1, consists of an infinite source, an impedance load, a shunt capacitor (with an associated circuit breaker), a transformer (with an associated CB), and a fault selection arrangement. The data of the system are summarized as follows: The infinite source is modeled with a voltage source that is connected in series with impedance. The supply voltage of the source has been chosen as Us= 12 kV. The series impedance has been chosen so that the power system will have a shortcircuit power of approximately Sk=831MVA (R=12.2mΩ, L= 0.55 mH). The supply frequency of the voltage source is selected to f= 50 Hz. A short-circuit power of 831MVA will give a short-circuit current of approximately Ik=40 kA. The impedance load is modeled by impedance consisting of a resistor and an inductance. Their values are chosen so that the load current is approximately 630 A. The shunt capacitor is modeled by a capacitance of C=90.19μF. The shunt capacitor gives a reactive power supply of 4.08 MVAr at nominal voltage. The shunt capacitor is connected to the power system by a CB which, at the start of the simulation, is open. The capacitor is uncharged at the start of the simulation. The transformer is connected in delta on the primary side and in Y on the secondary side. The winding voltages of the transformer are 12 kV at the primary side and 240 V at the secondary side. The leakage reactance is 0.122 p.u. on a transformer rating of 10.2 MVA. The residual flux in the transformer is also modeled.

©IJRASET 2015: All Rights are Reserved

Volume 3 Issue VI, June 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

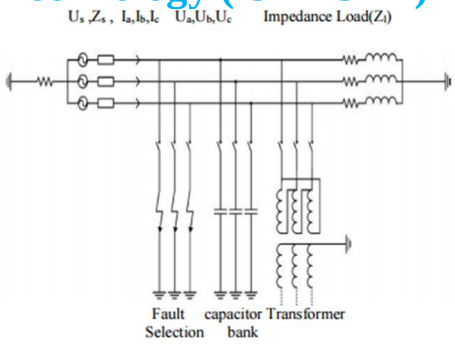


Fig. 1 Test Power System

III.PROPOSED PLL

The PLL (Phase Locked Loop) has been an important device in electronics and power system applications ever since the first implementation in the 1930s by de Bellescize.The first PLLs were analog devices but following the development in solid-state electronics and computer technology, the PLL has developed from an analog device via digital implementations to pure software implementations.PLL is a feedback loop which locks two waveforms with same frequency but shifted in phase. The fundamental use of this loop is in comparing frequencies of two waveforms and then adjusting the frequency of the waveform in the loop to equal the input waveform frequency. The heart of the PLL is a phase comparator which along with a voltage controlled oscillator (VCO), a filter and an amplifier forms the loop. If the two frequencies are different the output of the phase comparator varies and changes the input to the VCO to make its output frequency equal to the input waveform frequency. The locking of the two frequencies is a nonlinear process but linear approximation can be used to analyze PLL dynamics. In getting the PLL to lock the proper selection of the filter is essential and it needs some attention. If the filter design is understood from control theory point-of-view then the design becomes quite simple.

A. Basics Of PLL

A PLL is a circuit that is used to synchronize an input signal with a reference signal (an output signal that is generated by the PLL) with respect to phase and frequency. The function of the PLL can be explained from the block diagram of a simple PLL, as shown in Fig.2. The input signal u1(t) is compared with the reference signal u2(t) in the phase detector (PD). The output of the phase detector is zero as long as the input signal and the output signal is equal in phase and frequency. If the phase or frequency of the input signals changes, the output of the phase detector will deviate from zero. The error signal is passed through a low-pass filter (LF) and then to a voltage-controlled oscillator (VCO), which generates a reference signal (the output signal). If the error signal deviates from zero, the VCO will adjust the frequency of the reference signal so that the phase error becomes zero and the two signals are in phase. When the input signal is in phase with the reference signal, the PLL is in its locked state, hence the name phase locked.

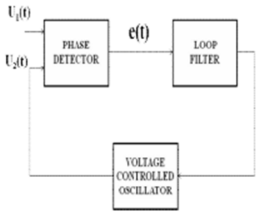


Fig. 2 Basic Block diagram of PLL.

B. Description Of PLL For Discrimination Between Faults And Transients

The PLL design which has been proposed for fault discrimination is drawn in the below figure. A vector implementation, as shown in Fig. 3, of a PLL is described in this paragraph. Compared to the block diagram of Fig. 2, the error signal e(t) corresponds to the output of the PD, whereas the proportional-integral (PI) regulator and the integrator corresponds to the loop filter and the voltage-controlled oscillator (VCO). The inputs to the PLL are the three phase-currents (Ia ,Ib , and Ic), which are first transformed to αβ

©IJRASET 2015: All Rights are Reserved

quantities (Iα and Iβ) using Clarke's transformation.

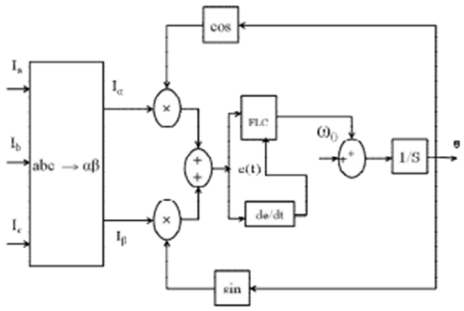


Fig. 3 PLL implementation

Then, the αβ quantities are projected onto a reference frame. Depending on the proximity of the αβ quantities to the reference frame, an error signal is formed. This error signal is fed through a PI regulator so that the error is controlled to zero. Once the error is zero, the input signals are in phase with the reference frame. The error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient occurs in the system, the error signal will deviate from zero. Depending on the characteristics of the transient, the deviation will have different magnitude and frequency. Since a fault is typically an ac fundamental power frequency character, the deviation will be different than for a switching transient that contains no fundamental power frequency components. The behaviour of the error signal of the PLL will also depend on the tuning of the PLL.

C. Tuning Of The PLL

The PLL will be tuned to the power system frequency. PLLs have been used for many years in HVDC transmission in order to synchronize the firing of the thyristors to the phase angle of the connected ac system. It is thus a well known procedure and it is advisable to use parameters from such an installation as a starting point for the tuning. Finetuning of the parameters can then be made by, for example, computer simulations or any other standard tuning method.

D. Fault Detection And Discrimination Using A PLL

The method that is used to detect a fault and discriminate the fault from a switching transient is described here. Two algorithms are executed in parallel. The first algorithm is based on the estimation of the magnitude of the current. If the estimated magnitude is higher than a preselected threshold, a flag is set. The second algorithm is as previously mentioned, monitoring the error signal of a PLL. If this error signal exceeds a preselected threshold, a second flag is set. If both flags are set, it is determined that a fault has occurred.

IV. DESIGN OF FLC

A. Design Of FLC

The FLC which is shown in above diagram has to be designed using fuzzy toolbox.The design starts with assigning the mapped variables inputs/output of the fuzzy logic controller (FLC). The first input variable to the FLC is the error e(t) and the second is change in error Δe(t). The output variable to the FLC is the current.

B. Membership Functions

After choosing proper variables as input and output of fuzzy controller, it is required to decide on the linguistic variables. These variables transform the numerical values of the input of the fuzzy controller to fuzzy quantities. The number of linguistic variables describing the fuzzy subsets of a variable varies according to the application. Here five linguistic variables for each of the input and output variables are used to describe them. Table 1 shows the Membership functions for fuzzy variables.

©IJRASET 2015: All Rights are Reserved

Volume 3 Issue VI, June 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

NB	NEGATIVE BIG
NM	NEGATIVE MEDIUM
NS	NEGATIVE SMALL
ZE	ZERO
PS	POSITIVE SMALL
PM	POSITIVE MEDIUM
PB	POSITIVE BIG

Table. 1 Membership functions for fuzzy variables

The membership function maps the crisp values into fuzzy variables. The triangular membership functions are used to define the degree of membership. Here for each input variable, seven labels are defined namely, NB, NM, NS, ZE, PS, PM and PB. Each subset is associated with a triangular membership function to form a set of seven membership functions for each fuzzy variable.

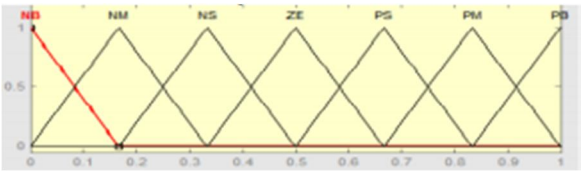


Fig.4 Membership function for e(t)

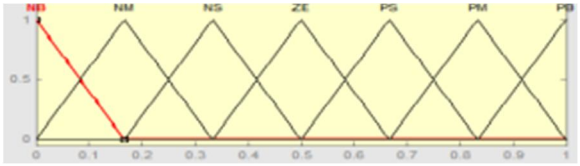


Fig.5 Membership function for Δe(t).

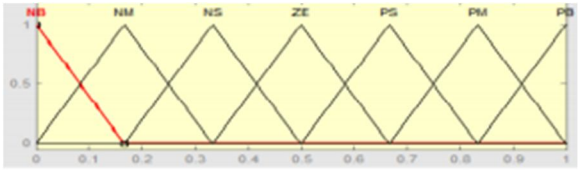


Fig. 6 Membership function for current

The membership function for e(t),Δe(t) and voltage are shown in Figure 6.11,Figure 6.12 and Figure 6.13 respectively. Knowledge base involves defining the rules represented as IF - THEN rules statements governing the relationship between input and output variables in terms of membership functions. In this stage the input variables speed deviation and acceleration are processed by the inference engine that executes 7×7 rules represented in rule Table 2.

E / ΔE	MF1 NB	MF2 NM	MF3 NS	MF4 ZE	MF5 PS	MF6 PM	MF7 PB
MF1 NB	NB	NB	NB	NB	NM	NS	ZE
MF2 NM	NB	NB	NM	NM	NS	ZE	PS
MF3 NS	NB	NM	NS	NS	ZE	PS	PM
MF4 ZE	NB	NM	NS	ZE	PS	PM	PB
MF5 PS	NM	NS	ZE	PS	PS	PM	PB
MF6 PM	NS	ZE	PS	PM	PM	PB	PB
MF7 PB	ZE	PS	PM	PB	PB	PB	PB

Table 2. Decision Table

©IJRASET 2015: All Rights are Reserved

The procedure for calculating the crisp output of the Fuzzy Logic Controller for some values of input variables is based on the following three steps.

Determination of degree of firing (DOF) of the rules The DOF of the rule consequent is a scalar value which equals the minimum of two antecedent membership degrees.

Inference Mechanism The inference mechanism consists of two processes called fuzzy implication and aggregation. The degree of firing of a rule interacts with its consequent to provide the output of the rule, which is a fuzzy subset. The formulation used to determine how the DOF and the consequent fuzzy set interact to form the rule output is called a fuzzy implication. In fuzzy logic control the most commonly used method for inferring the rule output is Sugeno method.

Defuzzification to obtain a crisp output value from the fuzzy set obtained in the previous step a mechanism called defuzzification is used. In this example output U is defuzzified according to the membership functions shown in Figure 6.13. Here center of gravity (COA) or centroid method is used to calculate the final fuzzy value.

V. SIMULATION OF PLL FOR E(T)

A. Under Transformer Energisation

The error signal has got from the scope ERROR e(t) while the breaker1 of fig 6.1is connected with a three phase transformer.

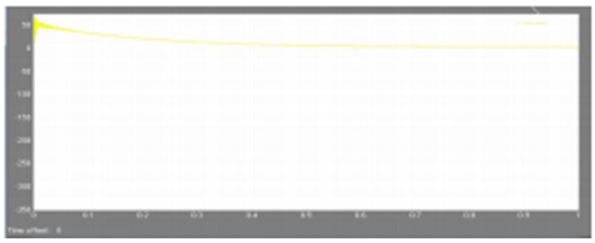


Fig .7 e(t) under transformer energisation

B. Under Capacitor Energisation

The error signal has got from the scope ERROR e(t) while the breaker1 of fig 6.1is connected with a three phase capacitor bank

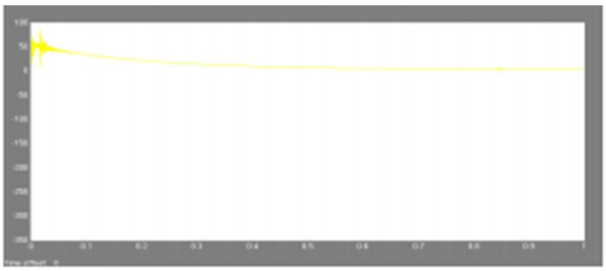


Fig .8 e(t) under capacitor energisation.

C. Under 3-ϕ Fault

The Error Signal has got from the scope ERROR e(t) while the breaker 1 of fig 1 is connected with a fault and which is set to 3-ϕ fault.

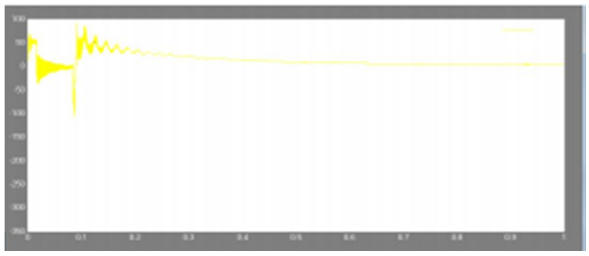


Fig.9 e(t) under 3Φ fault

D. Under LG Fault

The error signal has got from the scope ERROR e(t) while the breaker1 of fig 6.1is connected with a fault and which is set to LG fault.

©IJRASET 2015: All Rights are Reserved

Fig.10 e(t) under LG fault

E. Under LL Fault

The error signal has got from the scope ERROR e(t) while the breaker1 of fig 6.1is connected with a fault and which is set to LL fault

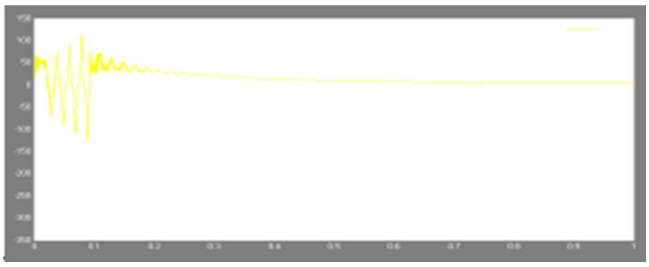


Fig .11 e (t) under LL fault

VI. SIMULATION OF POWER SYSTEM

A. Under Fault Condition

The power system model is simulated after designing PLL with FLC under the fault condition. The main consideration of work of CB is the line current in the power system. The current waveform is shown in the below fig. The fault has been created at 10 ms using the property window of fault as well as breaker1 in the model. The CB got open at time when the current become zero. The resultant waveform is shown in fig.

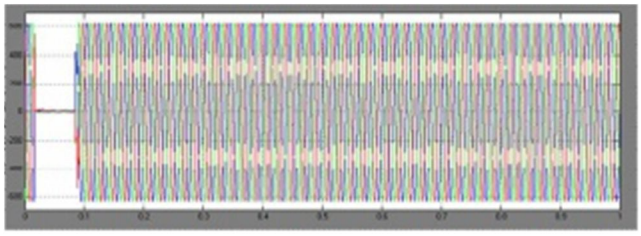


Fig.12 current waveform during fault

B. Result

The current waveform shown in above fig describes that the time taken to make the current value to zero is 16.7 ms and the occurrence of fault is 10 ms. So the time duration need to open the CB is around 7 ms. Thus the operating time is considerably reduced by using the FLC in the proposed PLL logic.

VII. CONCLUSION

In this paper, it has been demonstrated that a PLL can be used to determine whether a current transient is due to a fault in the system or due to a switching transient. Transformer and capacitor switching have been specifically studied due to the large occurrence of these switching transients in the power system. Simulations have been performed using a test system where faults and switching transients have been simulated. For all of these events, a large difference was observed in the error signal of the PLL when a fault or a switching transient was applied. This difference can be used to discriminate faults from switching transients. The PLL (with FLC) is discriminating the fault and transients in a fast manner than the previous one and also the operating time is considerably reduced to 7ms. Thus the FLC shows an improved performance than the conventional one. In this paper the discrimination between

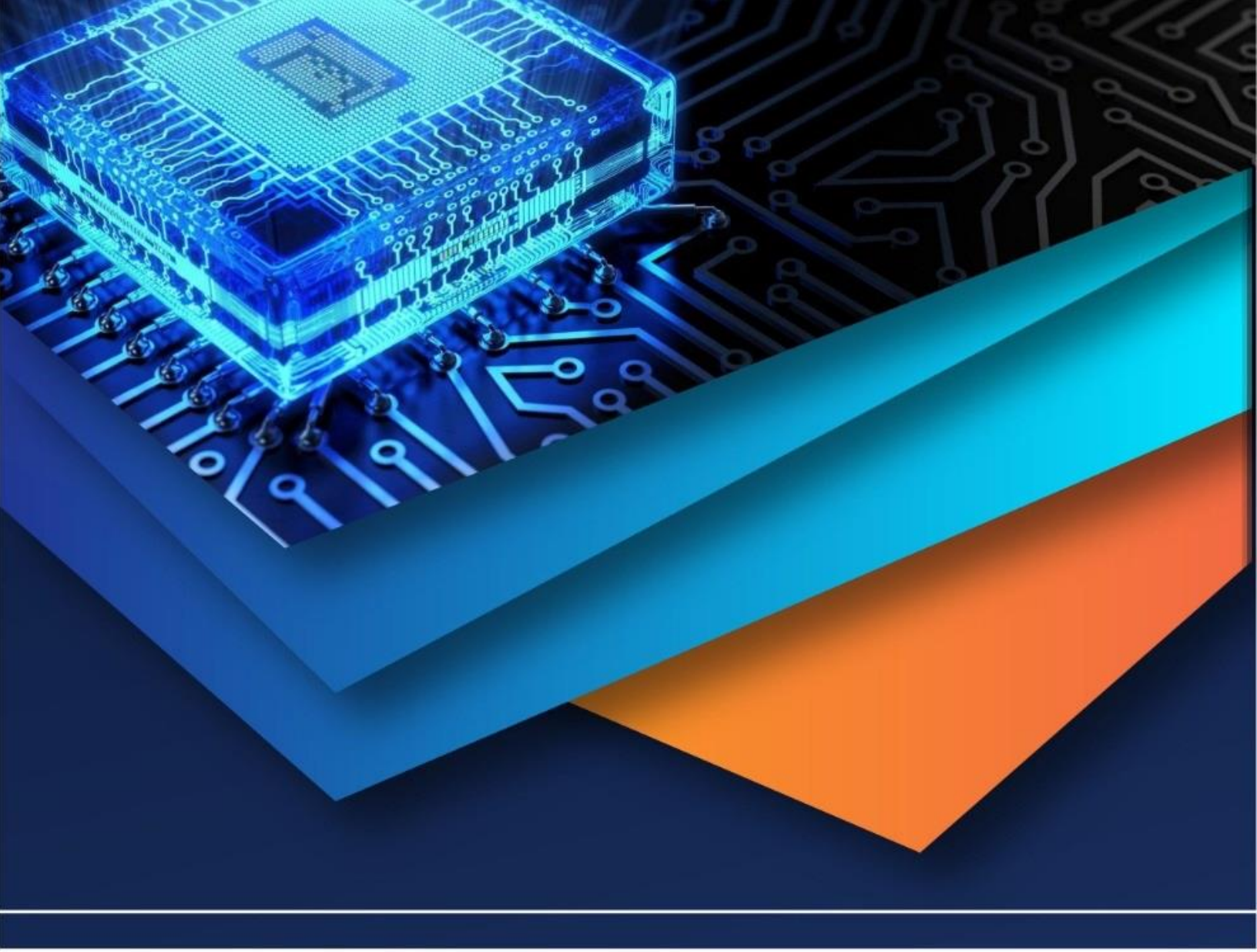
©IJRASET 2015: All Rights are Reserved

transients and low impedance fault has performed. For future work, high impedance faults must also be considered.

REFERENCES

[1] Magnus Ohrstrom and Lennart Soder, Member, IEEE, " Fast Protection of Strong Power Systems With Fault Current Limiters and PLLAided Fault Detection",IEEE Transactionsactions on Power Delivery Volume.26,NO.3,July 2011.
[2] M.Karimi-Ghartemani and M.R.Iravani, "A nonlinear adaptive filter for online signal analysis in power systems: Applications," IEEE Transactions 0n Power Delivery, Volume. 18, No. 4, June 2002.
[3] L.G.B. Rolim, D. R. da Costa, Jr, and M.Aredes, "Analysis and software implementation of a robust synchronizing PLL circuit based on the PQ theory," IEEE Transactions on Industrial Electronics, Volume.53, No.6, December 2006.
[4] M. ohrstrom, "Fast fault detection for power distribution systems," presented at the IASTED Conference. Power and Energy Systems, Marina del Rey, CA, May 13–15, 2002.
[5] A.Timbus, T. Teodorescu, F. Blaabjerg, M. Liserre, and P. Rodriguez,"PLL algorithm for power generation systems robust to grid voltage faults," presented at the Power Electronics Specialists Conference., Jeju,South Korea, 2006.
[6] T. Emura, L. Wang, M. Yamanaka, and H. Nakamura, "A highprecision positioning servo controller based on phase/frequency detecting technique of two-phase-type PLL," IEEE Transactions. Ind. Electron., volume. 47,no. 6, pp. 1298–1306, December. 2000.
[7] S.K. Chung, "Phase-Locked Loop for grid-connected three-phase power conversion systems," IEE Proceedings on Electronic Power Applications, volume. 147, no. 3, pp. 213–219, 2000.
[8] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL structure for utility connected systems," in Conference. Rec. 36th IEEE-IAS Annu. Meeting, volume. 4,pp. 2655–2660.
[9] V. Kaura and V. Blasko, "Operation Of A Phase Locked Loop System Under Distorted Utility Conditions," IEEE Transactions. Ind. Appl., volume. 33, no. 1, pp. 58–63, January./February. 1997.
[10] R. E. Best, " Phase-Locked Loops—Design, Simulation and Applications",5th ed. New York: McGraw-Hill, 2003.
[11] G. C. Hsieh and J. C. Hung, "Phase-locked loop techniques—A survey," IEEE Transactions. Ind. Electron., volume. 43, no. 6, pp. 609–615, December 1996.
[12] M.A. Beg , M.K. Khedkar, S.R. Paraskar and G.M. Dhole , "A Novel Clarke Wavelet Transform Method To Classify Power System Disturbances" International Journal on "Technical and Physical Problems of Engineering" (IJTPE) Published by International Organization on TPE (IOTPE), December 2010 Issue 5 Volume 2 Number 4 Pages 27-31.
[13] M. Karimi-Ghartemani and M. R. Iravani, "A signal processing module for power system applications," IEEE Transactions on Power Delivery, volume. 18, no.4, pp. 1118–1126, October. 2003.
[14] H. Shokrollah Timorabadi and F. P. Dawson in Proc. "A ThreePhase Frequency Adaptive Digital Phase Locked Loop for Measurement, Control and Protection in Power Systems", Nagoya, Japan, 2007, pp. 183–90.
[15] M. Ohrstrom, "Fast fault detection for peak current limitation based on few samples," presented at the 17th Int. Conference. Electricity Distribution, Barcelona, Spain, May 12–15, 2003.
[16] A.V. Timbus, M. Liserre, R. Teodorescu, and F. Blaabjerg, "Synchronization methods for three phase distributed power generation systems.An overview and evaluation," in Proc. of PESC'05, 2005, pp. 2474– 2481.
[17] M. C. Benhabib and S. Saadate, "A new robust experimentally validated Phase-Looked Loop for power electronic control," EPE Journal, volume. 15,no. 3, pp. 36–48, August 2005.
[18] P. Rodriguez, J. Pou, J. Bergas, I. Candela, R. Burgos, and D. Boroyevich, "Double synchronous reference frame PLL for power converters," in Proc. of PESC'05, 2005, pp. 1415–1421.
[19] Masoud Karimi-Ghartemani, "A Method for Synchronization of Power Electronic Converters in Polluted and Variable-Frequency Environments", IEEE Transactions On Power Systems, Volume. 19, No. 3, August 2004.
[20] S.-J. Lee, J.-K. Kang, and S.-K. Sul, "A new phase detecting method for power conversion systems considering distorted conditions in power system," in Proc. Industry Applications Conference., 34th IAS Annu. Meeting,volume. 4, 1999, pp. 2167–2172.
[21] G. H. Jung et al., "DSP based control of high power static VAR compensator using novel vector product phase locked loop," in Proc. 27th Annu. IEEE Power Electronics Specialists Conference. (PESC'97), Baveno, Italy, 1996, pp. 238–243. [22] M. F. Lai and M. Nakano, "Special section on phase-locked loop techniques," IEEE Transactions on Industrial Electronics, volume. 43, pp. 607–608, December. 1996.
[22] Takashi Emura, Lei Wang, "A High-Resolution Interpolator for Incremental Encoders Based on the Quadrature PLL Method", IEEE Transactions On Industrial Electronics, Volume. 47, No. 1, February 2000.
[23] C. Zhan, C. Fitzer, V. K. Ramachandaramurthy, A. Arulampalam,M. Barnes, and N. Jenkins, "Software phase-locked loop applied to dynamic volumetage restore (DVR)," in Proc. IEEE Power Eng. Soc. Winter Meeting, 2001, volume. 3, pp. 1033–1038. [25] A.G. Phadke, "Synchronized phasor measurement in power systems," IEEE Computer Application in Power, volume. 6, pp. 10–15, April. 1993.

©IJRASET 2015: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)