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Comparison of Various Transformerless Full-bridge Topologies for Photovoltaic Grid -Tied Inverters

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Abstract— If there is no transformer is used in the single phase grid tied photovoltaic system, then the electrical connection live between the grid and the PV array. In this condition, the generated common mode voltage largely determines the leakage current. It flows through the parasitic capacitance, which is presented between the PV array and the ground. This leakage current can cause radiated interference effect, harmonics and losses. Neutral point clamped topologies are the efficient path to reduce the leakage current. In this paper, two basic switching cells, positive neutral point clamped cell and negative neutral point clamped cell are introduced to flesh NPC topologies and unipolar sinusoidal pulse width modulation(USPWM) technique is used for the inverter. Here two existing topologies such as optimized H5(OH5) and full bridge DC bypass (FB-DCBP) are explained and also compared with the proposed positive negative neutral point clamped (PN-NPC) topology. The simulation results show the common mode voltage, THD and leakage current.
Keywords — Transformer less inverters, grid, leakage current, common mode voltage, switching cells, photovoltaic system.

I. INTRODUCTION

The global energy demand of the world is proliferates every year. So the conventional energy sources are main provider of energy to the world. But these conventional energy sources are finite means non-renewable sources of energy and also these causes global warming and environmental pollution. Hence for accomplishing these higher energy demands non-conventional energy sources are most reliable, safe and lifetime available source of energy. There are several types of non-conventional energy sources such as solar, wind, hydropower, wind and geothermal energy. And these all are life time available, pollution free and more cost effective sources of energy. Among all these non-conventional energy sources, in solar power generation or photovoltaic (PV) generation the energy is generated by direct sun radiations falling at PV panels. Hence these generating units can easily be installed at any place near or within the city, terrace of houses, over the canals etc. due to this advantage and with the help of government incentives the use of PV generation is becoming more and more widespread all over the world. Before a line frequency or high frequency transformer is used to isolate the PV panels from the grid. This isolation transformer gives personal safety, reduces electromagnetic interference (EMI) noise and steps up and step downs the voltage levels in figure (1), but this line -frequency transformer increases the weight and high- frequency transformer needs more switching devices and conversion stages, thus reduces the overall system efficiency, performance, and reliability and increases cost, and also makes the system more complex.

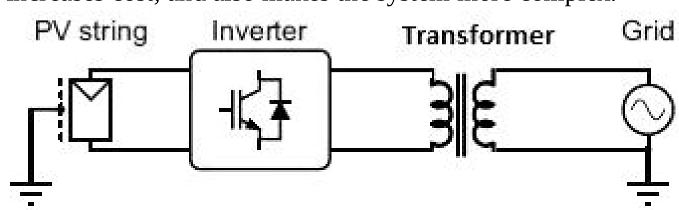

Fig.1.PV system when transformer is connected between inverter and grid

Volume 3 Issue VII, July 2015
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International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Hence many topologies use transformerless inverter for getting increased efficiency and reliability, reduced losses, cost and size. But when no transformer is used in a grid-connected photovoltaic (PV) system a common mode voltage between the PV panels and ground exist, which injects an additional ground current (common –mode currents) in the inverter/grid as shown in figure (2) Which increases the electromagnetic emissions, losses and harmonics in the system. The common mode voltage Vcm in the full bride topology is represented as

$$Vcm=0.5\ (V_{AN}+V_{BN})$$

Where V_{AN} is the voltage between terminals A and N and V_{BN} is the voltage between terminals B and N.

To eliminate the leakage currents effectively common mode voltage (V cm) should be constants in all modes of topologies. The topologies used to eliminate the leakage currents are Optimized H5 (OH5), Full Bridge DC Bypass (FB_DCBP) and Positive-negative neutral point clamped (PN-NPC)

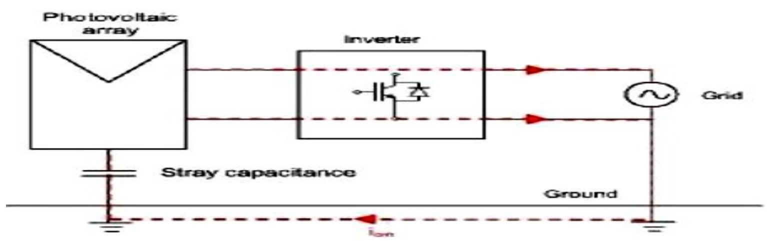

Fig.2.common mode currents in transformer less inverter

II. PV ARRAY

Photovoltaic array is used for transfer the solar energy into the electrical energy. PV cell is the basic unit of the photovoltaic generator. Combination of PV cells makes a module and modules together become PV array.

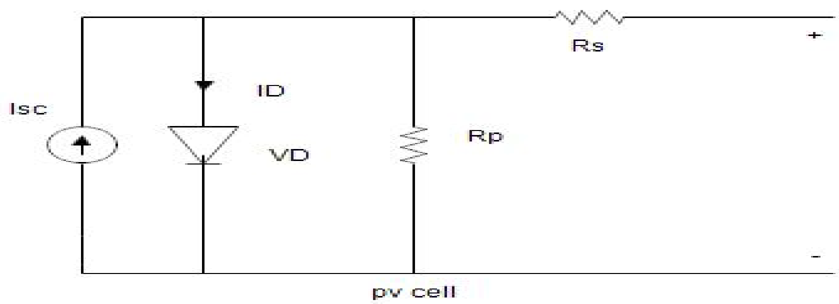

Fig.3. Circuit model of PV cell

Figure3. Shows circuit model of PV cell. Basically photovoltaic cell is a semiconductor diode whose PN junction is exposed to light and generates the charge carriers when the incidence of light on the cell that originate an electrical current. This diagram consists of a current source which is connected in parallel with a diode, series and parallel resistances are represents by Rs and Rp respectively. Total current I is composed of light generated current Ipv and the diode current Id.

Diode characteristics

$$I_d = I_{sat*}[\exp (v_d/v_t)-1] \quad (1)$$

Where

$I_{d=}$ diode current (A)

V_d= diode voltage (V)

www.ijraset.com Volume 3 Issue VII, July 2015
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International Journal for Research in Applied Science & Engineering Technology (IJRASET)

I_{sat}= diode saturation current (A)

V_T=K*T/q*Qd*Ncell*Nser (2)

V_T= temperature voltage

T=cell temperature (K)

K= Boltzmann constant=$1.3806e^{-23}$ $J.K^{-1}$

Q=electron charge=$1.6022e^{-19}$ C

Qd= diode quality factor

Ncell=number of series connected cells per module

Nser =number of series connected modules per string.

III.OPTIMIZED H5(OH5) TOPOLOGY

For leakage current elimination, it is required to eliminate the connection between PV array and load during the freewheeling modes.OH5 is mainly introduced to eliminate the leakage currents by making common mode voltage as half the supply voltage.OH5 topology and its firing pulses are as shown in figure4 (a) and 4(b).the current flow path in positive half cycle can be treated as Cdc1 (+) _ S5_S1_L1_Vg_L2_S4_Cdc2 (-), negative half cycle current path is Cdc1 (+) _S5_S3_L2_Vg_L1_S2_Cdc2 (-). Unfortunately still that problem persists while operating the switches S5 and S6 as shown in fig4 (a) which are short circuiting the input split capacitor Cdc1 as an alternative to provide a time gap between the gating signals of S5 and S6, which will lead to change in the common mode voltage and still induces leakage current. To eliminate this short circuit problem FB-DCBP topology is introduced.

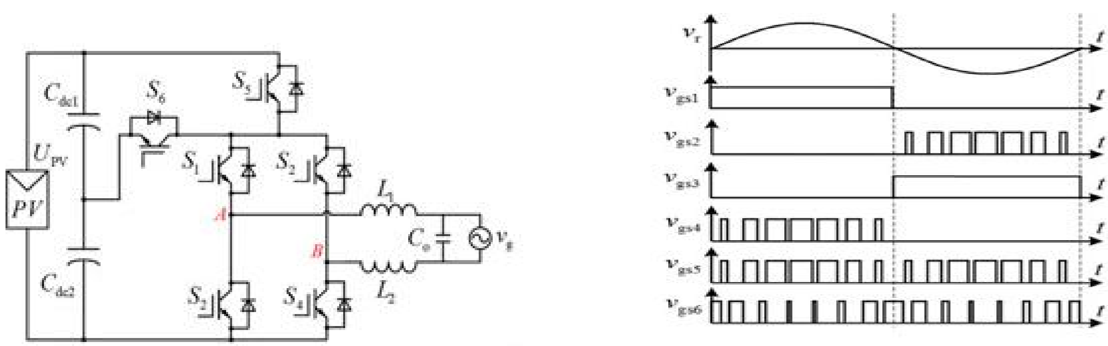


Fig.4. OH5 topology and its firing pulses

IV.FB-DCBP TOPOLOGY

The FB-DCBP topology and its firing pulses are as shown in figure5. This topology gives better operation compared to OH5 topology because freewheeling mode depends on switching speed of individual diodes. The current flow path in the positive half

Volume 3 Issue VII, July 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

cycle is Cdc1 (+) _S5_S1_L1_Vg_L2_S4_S6_Cdc2 (-), and negative half cycle is Cdc1 (+) _S5_S3_L2_Vg_L1_S2_Cdc2 (-). Here D1, D2 helps to form the path for inductor current during freewheeling modes. Turn on speed of diodes, decides suppression of leakage current but main problem with FB-DCBP is having more conduction losses as number of switches responsible for conduction in active mode is about four.

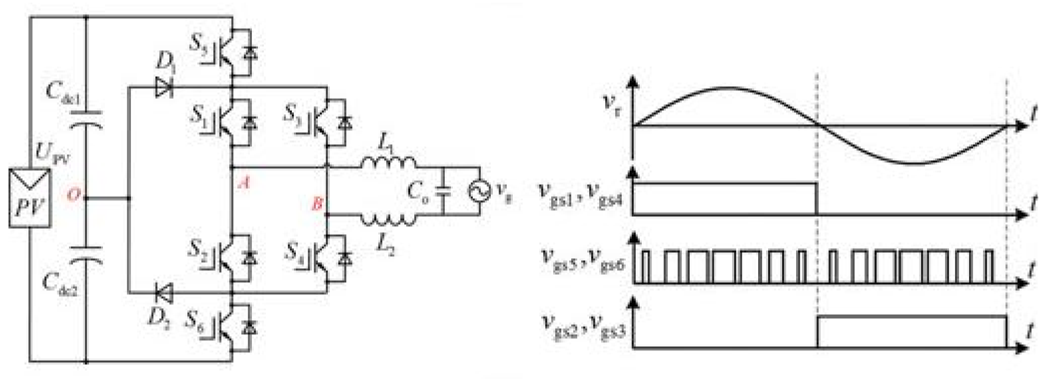


Fig.5. FB-DCBP topology and its firing pulses

V. PN-NPC TOPOLOGY

The PN-NPC model construction is based on the two basic NPC switching cells, those are positive neutral point clamped cell (P-NPCC) and negative neutral point clamped cell(N_NPCC) as shown in figure 6.

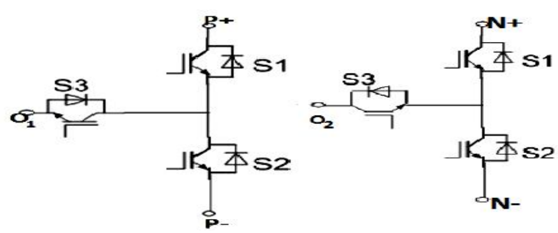


Fig.6.Positive neutral point clamped cell, negative neutral point clamped cell

A. Need For NPCC

To eliminate leakage current we can conclude some key points.

1) PV array should isolate from the load during freewheeling modes.
2) Making common mode voltage exactly half of input voltage by making use of other switches which indicates the necessity of another switch to clamp common mode voltage to our required level. This leads to the formation of neutral point clamping cell (NPCC). Which is having three switches, the middle switch is responsible for freewheeling mode and remaining two switches are responsible for active modes.

For satisfaction operation of PN-NPC, the following rules are should be followed.

Rule 1: The P_NPCC top end (P+) should be connected to positive terminal of source and bottom end (P-) is connected to its

Volume 3 Issue VII, July 2015
ISSN: 2321-9653

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

output filter inductor. Similarly the N-NPCC has its (N-) should be connected to negative terminal of source and (N-) is connected to output filter inductor.

Rule 2: To separate load from source and as well as to maintain required current path during freewheeling modes we need three switches so each leg should contain at least one NPCC.

Rule 3: Middle terminals should be connected to midpoint of the input split capacitors.

B. Modes Of Operation

The proposed PN-NPC topology and gate drive pulses are shown in figure7. Unity power factor is maintained when an inverter is tied to grid.one leg of PN-NPC is fitted with P-NPCC and second leg is fitted with N-NPCC to form required PN- NPCC. This arrangement can be observed in fig 7. There are four modes of operations.

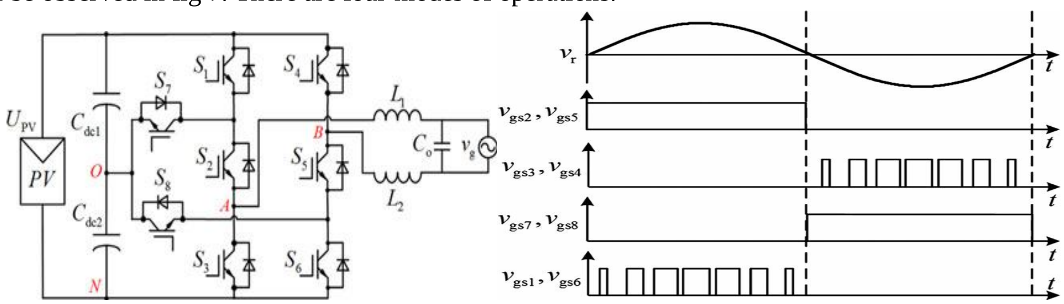


Fig .7.PN-NPC topology and its firing pulses

Mode1: this is the active mode in the positive half cycle and the current path flow is Cdc1 (+) _S1_S2_L1_Vg_L2_S5_S6_Cdc2 (-), here $V_{AN}=V_{IN}$ and $V_{BN}=0$ then $V_{CM}= (V_{AN}+V_{BN})/2=0.5V_{IN.}$

Mode 2: it is the freewheeling mode in the positive half cycle. Where middle switches S2 and S5 turns on and all other switches will turns off. Anti-parallel diodes of S7 and S8 will make required path for inductor current. The current path of this mode can be treated as O_ S7 (diode) _S2_L1_Vg_L2_S5_S8 (diode) _O.here $V_{AN}=0.5V_{IN}$, $VBN=0.5V_{IN}$ then $V_{CM}= (V_{AN}+V_{BN})/2=0.5V_{IN}$.

Mode 3: this is the active mode in the negative half cycle. The responsible switch for this mode are S3, S4, S7, S8 and current path is Cdc1 (+) _S4_L2_Vg_L1_S3_Cdc2 (-). S7 and S8 are being in on state but they won't carry any inductor current. Here $V_{AN}=0$, $V_{BN}=V_{IN}$ then $V_{CM}= (V_{AN}+V_{BN})/2=0.5V_{IN.}$

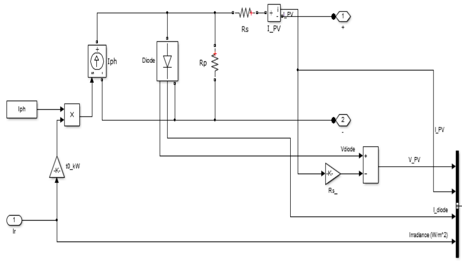
Mode 4: it is the freewheeling mode in the negative half cycle. Where S7 and S8 switches are turns on and remaining switches are turned off. Inductor current takes path of anti-parallel diodes of S2, S5. Then the current path can be treated as O_S8_S5 (diode) _L2_Vg_L1_S2 (diode) _S7_O. here $V_{AN}=0.5V_{IN}$ and $V_{BN}=0.5V_{IN}$ then $V_{CM}= (V_{AN}+V_{BN})/2=0.5V_{IN.}$

It is clearly verified from the above analysis that common mode voltage is half of the supply voltage.

VI. SIMULATION MODEL AND RESULTS

Unipolar sinusoidal pulse width modulation is used for all above circuits at a carrier frequency of 20 KHz and input voltage of 400v. The circuits are simulated using MATLAB and all simulation figures are shown with their respective outputs.

A. PV Array



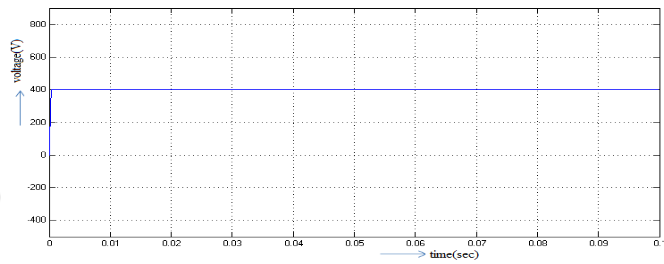


Fig.8 (a).Simulink model of PV Array fig .8(b). simulation output for PV array

B. OH5 Topology

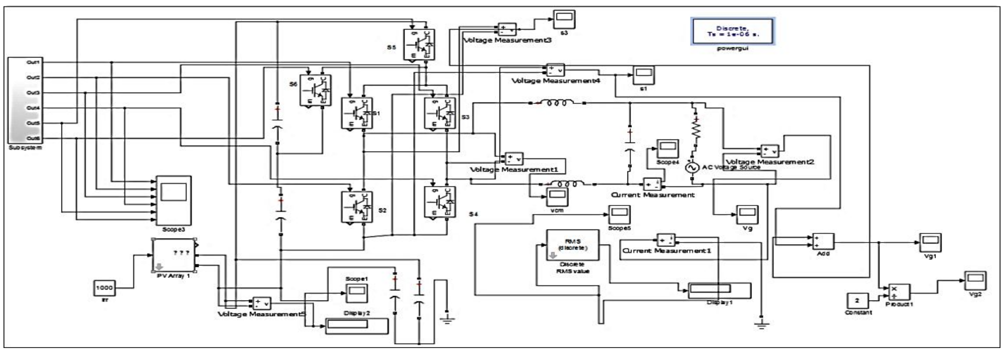


Fig. 9.simulink model of OH5 topology

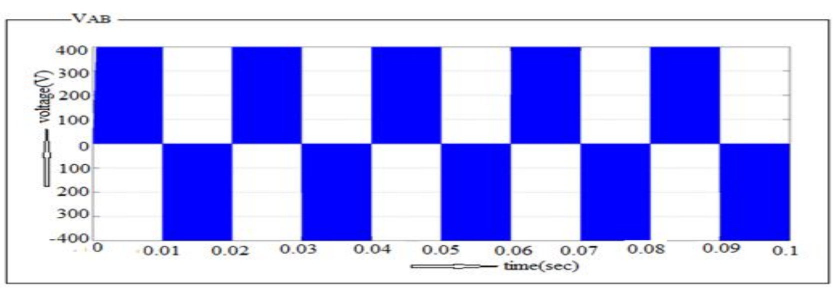


Fig.10. OH5 inverter output voltage

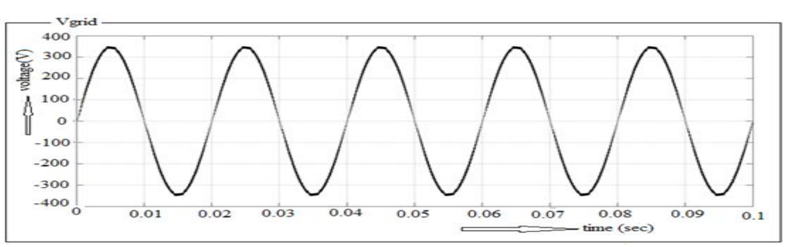


Fig.11. grid output voltage of OH5 topology

Volume 3 Issue VII, July 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

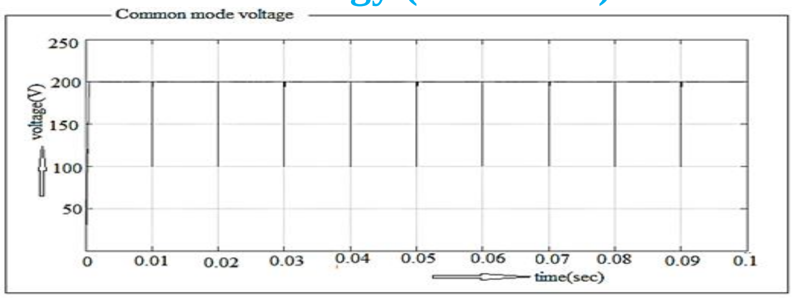


Fig.12. common mode voltage of OH5 topology

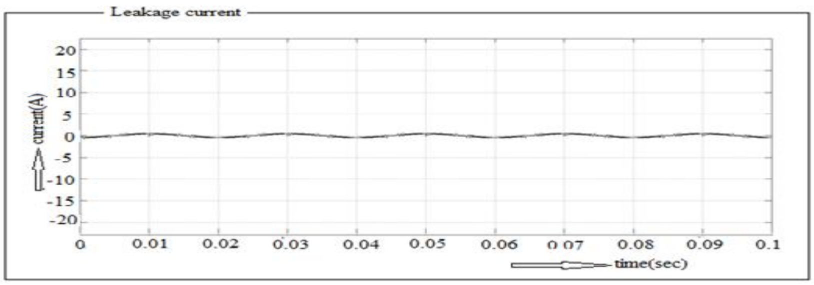


Fig.13. leakage current of OH5 topology

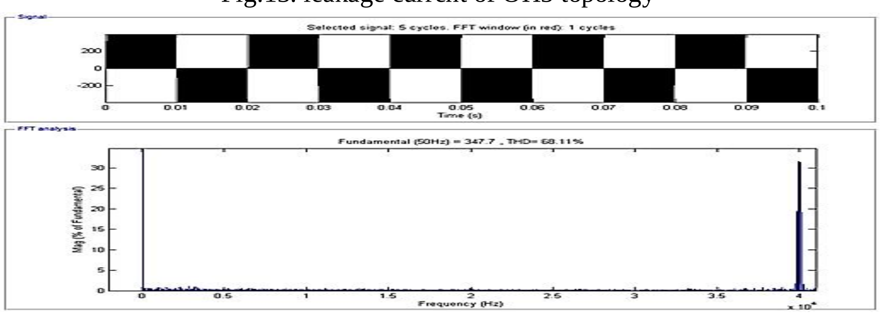


Fig.14. output voltage and %THD with FFT analysis before filter

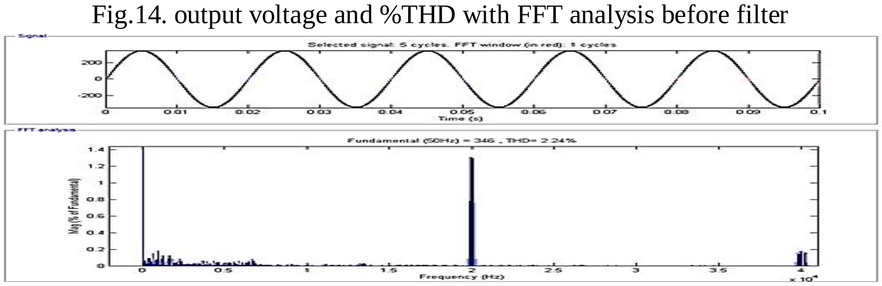


Fig.15. Output voltage and %THD with FFT analysis after filter

C. FB-DCBP Topology

Volume 3 Issue VII, July 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

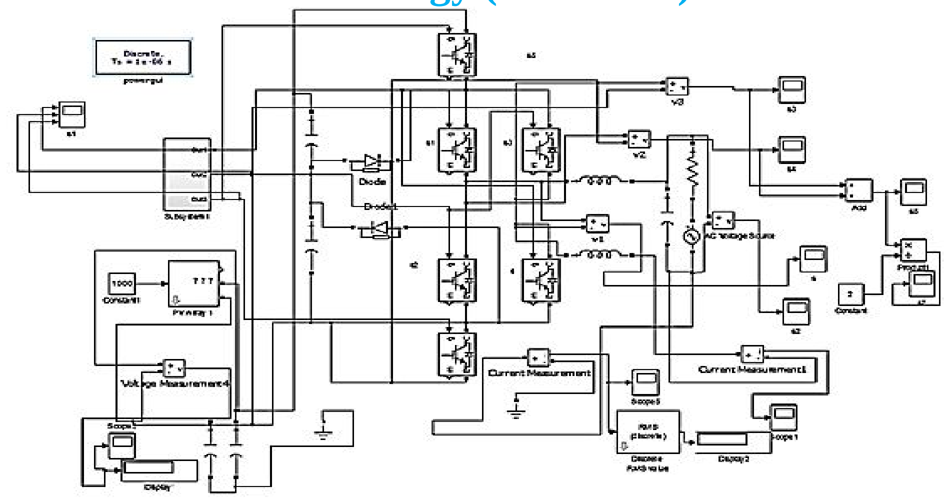


Fig.16. Simulink model of FB-DCBP topology

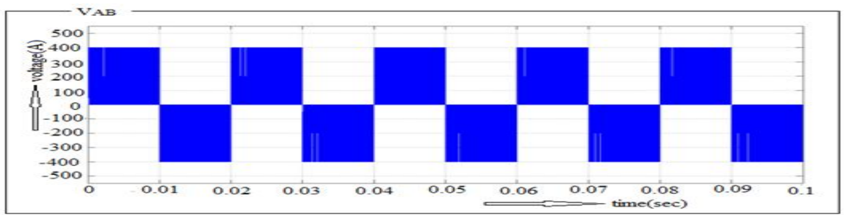


Fig.17.FB-DCBP inverter output voltage

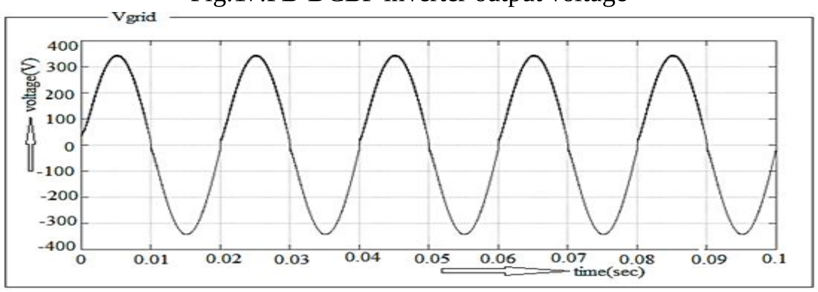


Fig.18.grid output voltage of FB-DCBP topology

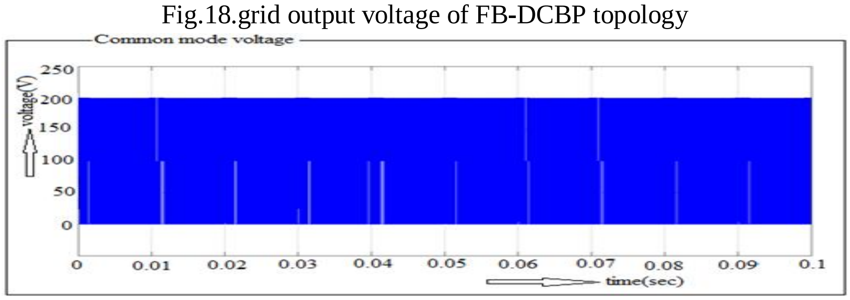


Fig.19. common mode voltage of FB_DCBP topology

Volume 3 Issue VII, July 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

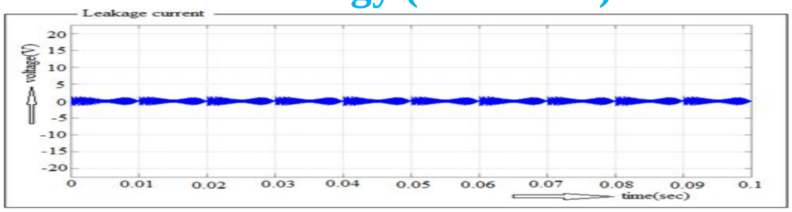


Fig.20. leakage current of B-DCBP topology

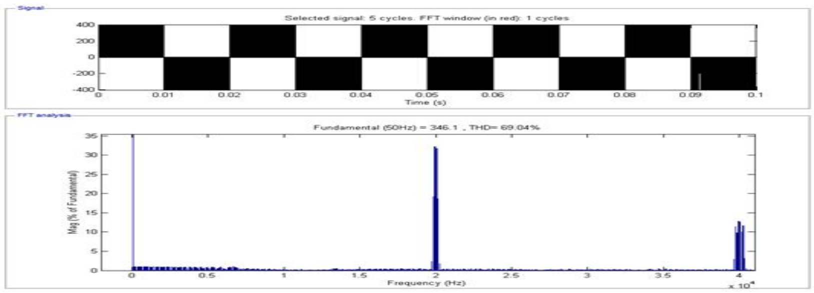


Fig.21 output voltage and %THD with FFT analysis before filter

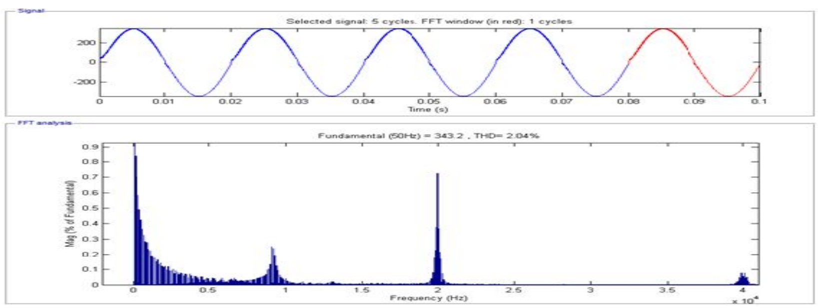


Fig.22. Output voltage and %THD with FFT analysis after filter

D. PN-NPC Topology

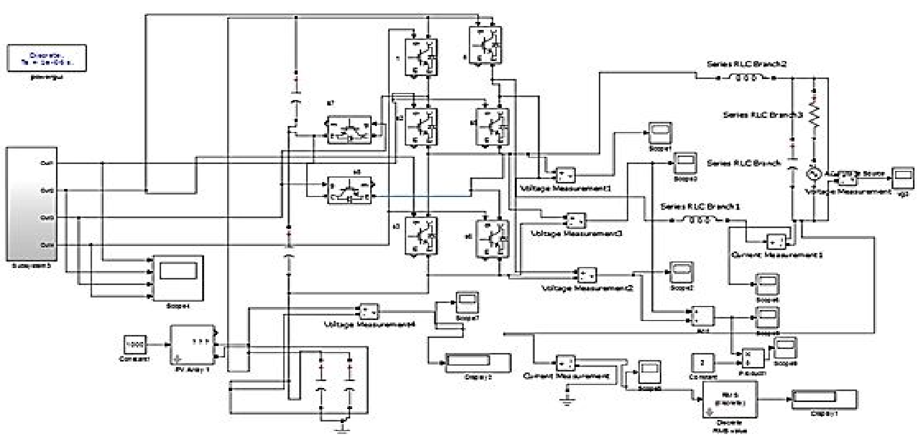


Fig.23.Simulink model of PN-NPC topology

Volume 3 Issue VII, July 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

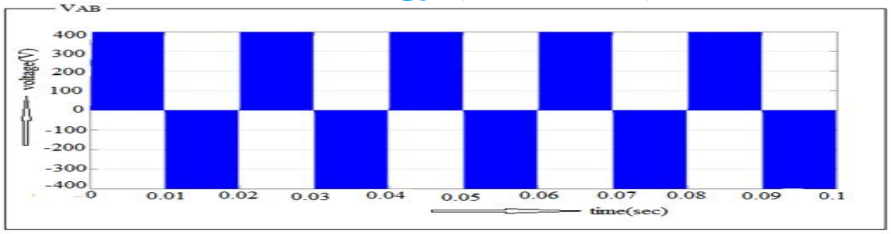


Fig.24.PN-NPC inverter output voltage

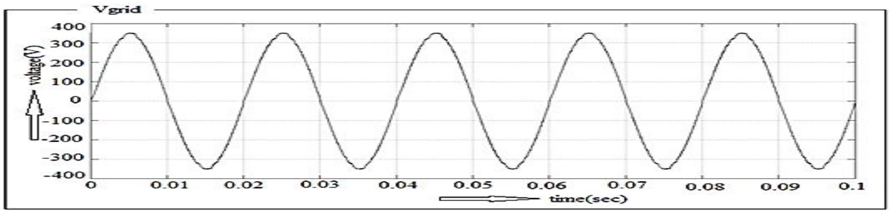


Fig.25.Grid output voltage of PN-NPC

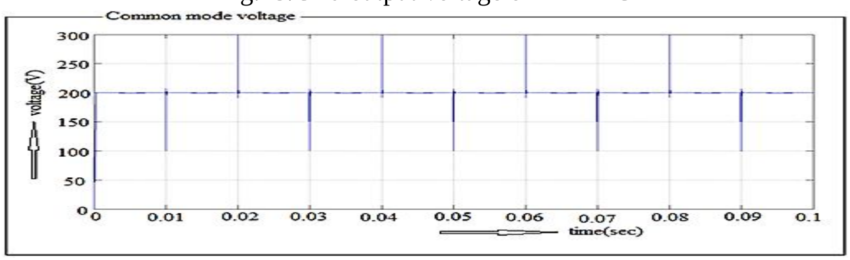


Fig.26.Common mode voltage of PN-NPC

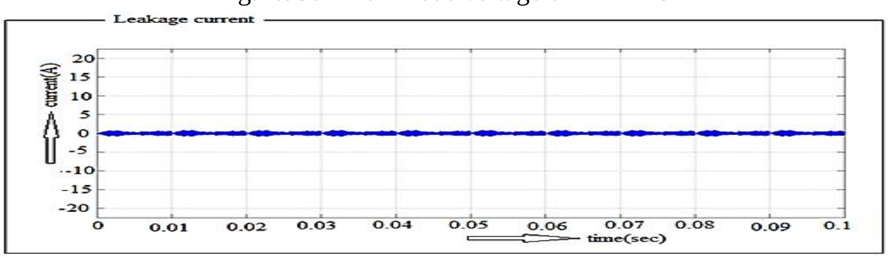


Fig.27.Leakage current of PN-NPC

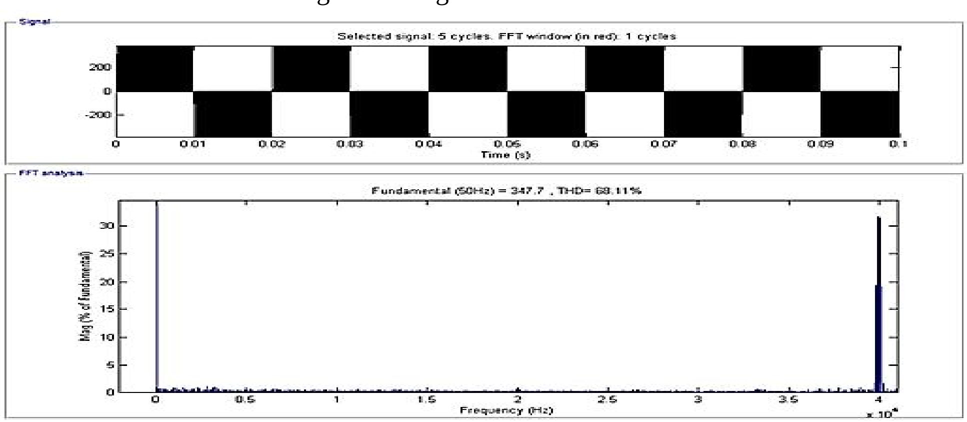


Fig.28.Output voltage and %THD with FFT analysis before filter-

Volume 3 Issue VII, July 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

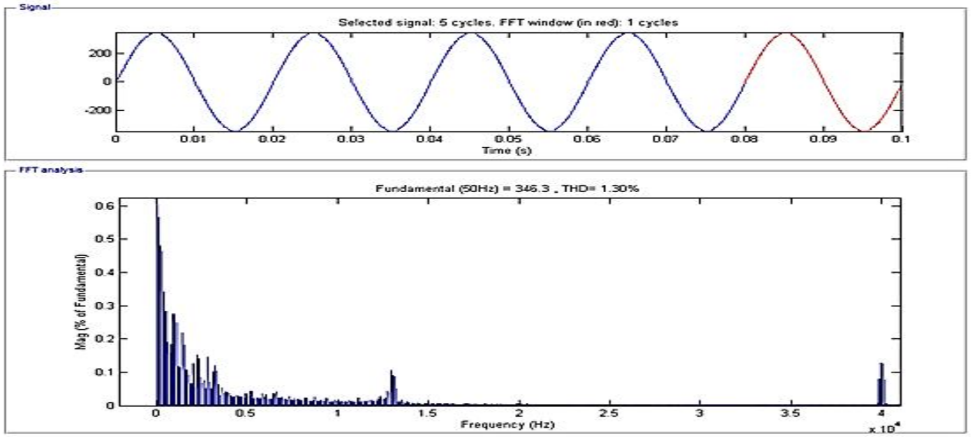


Fig.29.Output voltage and %THD with FFT analysis after filter

TABLE1
SIMULATION PARAMETERS

Parameter	Value
Rated power	1000w
Input voltage	380-700v
Switching frequency	20kHz
Filter inductorL1,L2	3mH
Filter capacitor	0.47µf
Grid voltage/frequency	230v/50Hz
PV parasitic capacitor Cpv1,Cpv2	0.1µf

VII. COMPARISION OF TOPOLOGIES

TABLEII
REQUIRED OUTPUTS OF TOPOLOGIES

Inverter output voltage		Grid output voltage		Leakage current(A)
Fundamental	%THD	fundamental	%THD	
347.7V	68.11	346V	2.24	0.2735
346.1V	69.04	343.2V	2.04	0.2258
347.7V	68.11	346.3V	1.30	0.2189

VIII. CONCLUSION

In this paper a new type of neutral point clamped inverter is introduced from deriving two basic switching cells. Furthermore the proposed topology yields better results compared to existing topologies. The comparisons of different topologies are validated by using MATLAB Simulink .THD using this topology is reduced than existing topologies and efficiency of this topology is also high. During all modes of operation the common mode voltage is constant and is equal to half of the supply voltage which leads to the excellent leakage current characteristics so it can be concluded that the proposed PN_NPC topology is best option for single phase inverters.

IX. ACKNOWLEDGMENT

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