iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 8 **Issue:** VI **Month of publication:** June 2020

DOI: http://doi.org/10.22214/ijraset.2020.6318

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VI June 2020- Available at www.ijraset.com

VLSI Architecture of Encoding using Sols Technique for Reducing Power in DSRC

K. Rathna Sree[1], P. Maheshwari[2], G. Raghavendra Reddy[3], P. Ravi Kumar Reddy[4]
[1, 2, 3, 4]*(BE) Department of Electronics and Communication Engineering, Matrusri Engineering college, Saidabad. Telangana*

Abstract: ***A convention, which is principally used for ITC, is the dedicated short-range communication (DSRC). DSRC is utilized in various applications and requires encoding techniques for secure transmission of the information. These encoding procedures are utilized to perform the error corrections and to improve the signal reliability. By joining various encodings which have comparative properties will prompt the improved territory streamlining and in mitigating the power consumption to the least. Thus, in this procedure we have attempted to join two distinct encodings in a single architecture. We have adopted SOLS technique to defeat the impediments that were faced earlier . The circuit acquired is a coordinated design of Flexible Macroblock Ordering and Manchester encoding to beat different downsides of conventional technique. Using SOLS strategy the equipment usage rate can be improved to 100%. This system will have lesser delay and area when contrasted with the current design. Using this delay and power consumption can be reduced in DSRC.***
Keywords: Encoding, DSRC, FMO, Manchester Encoder, SOLS.

I. INTRODUCTION

Vehicles use many remote advances to speak with different gadgets and one of the exact innovation is committed short-run correspondence (DSRC) [1], which is intended to help various applications dependent on vehicular report. DSRC is underneath dynamic advancement inside the United States and in various nations. For the transportation system dedicated short-range communication (DSRC) techniques are used. Utilizing this application numerous crashes can be forestalled and spare a great many lives as shown in the Figure 1. The automotive agency is jogging to develop this technology, to be used in automobile to automobile and automobile to side of the road verbal exchange. With the encoding data, a FM0 or Manchester encodings are used to decrease the quantity of mishaps [6].

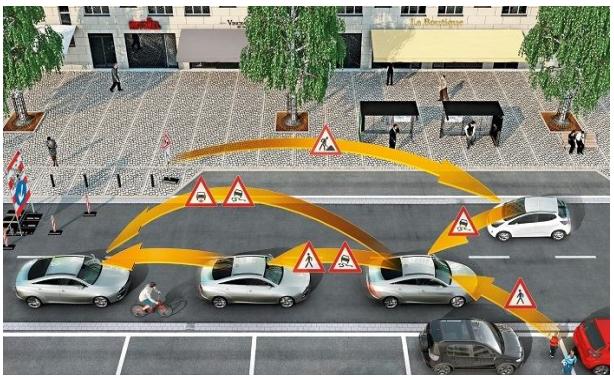


Fig.1 Vehicular networks based on DSRC

II. LITERATURE SURVEY

A mindful work has been occurring in this field of keen transportation and current car enterprises are dedicating significant measure of assets for research in this field. Since in regular daily existence the sharp transportation system has exquisite central focuses like trouble-free traffic, automobile prosperity and so forth. Wireless vehicular correspondence can possibly empower enormous variety of operations, the most significant of that are a group of security applications that can forestall crashes and spare a great many lives. The ampleness of this advancement is significantly dependent on pleasing standards for interoperability. Remembered for the conversation are the IEEE 802.11p amendment for remote access in vehicular conditions (WAVE), the IEEE 1609.2, 1609.3, and 1609.4 measures for Security, Network Services and Multi-Channel Operation, the SAE J2735 Message Set Dictionary, and the rising SAE J2945.1 Communication Minimum Performance Requirements standard. The following proposal shows how these norms concatenate to give a far-reaching answer.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VI June 2020- Available at www.ijraset.com

III. EXISTING SYSTEM

A. Manchester Encoding Technique

In the present days surely one of the most widely recognized information encoding procedures is Manchester. This is inferred with the XORing activity utilizing the Clock and X. The Manchester coding model is appeared in the beneath figure and is derived from:

$$X \oplus CLK \qquad [eq.1]$$

This coding provides the simplest method of combining the message signal to the information rate clock at the desirable end. The clock consistently consolidates a change inside one cycle, as similar to the Manchester code independent of what X is and shown within the Figure 2.

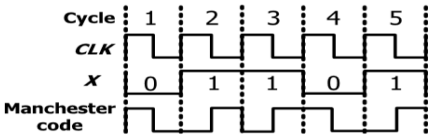


Fig.2. Illustration of Manchester coding example

B. FMO Encoding Technique

The encoding which might be a type of NRZ is FMO encoding. Flexible Macroblock Ordering is otherwise called Bi stage space encoding. The example is shown in Figure 3. The coding guideline of FM0 has the accompanying three principles:

1) The change is assigned among each FM0 code without considering the value of X.
2) In the event that X is 0, the FM0 has a progress among the cycle.
3) In the event that X is 1, no progress happens among the cycle.

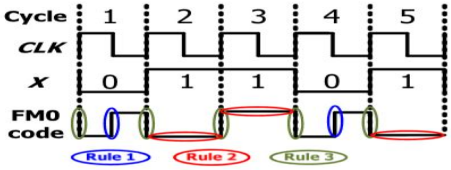


Fig.3 FM0 encoding example

C. State Code Principle Encodings

The management of gear plan for FM0 is not fundamental as that of Manchester. So the best way to deal with build up the hardware designing of FM0 encoding must lead with the FSM of FM0. A state code is independently doled out to each state, and each state code comprises of A and B. The hardware architecture of FM0 encoder has drawn from FSM. As per the coding guideline of FM0, the FSM of the FM0 is presented in Figure 4. The mark on the state advances shows the consistent estimation of the information arrangement to be encoded. For instance consider the state as S4, and its state code as 00 for An and B, separately. In the event that X is 0, the state-change must adhere to the two principles 1 and 2 so the state which will fulfill the two standards for the X 0 is S2 and if the X is 1, the state-progress should keep the two guidelines 1 and 3. The just one next-state which will fulfill the two guidelines for the X 1 is S1 and is as appeared in the underneath Figure 2.3. In this manner, the state progress of each state can be totally built [9].

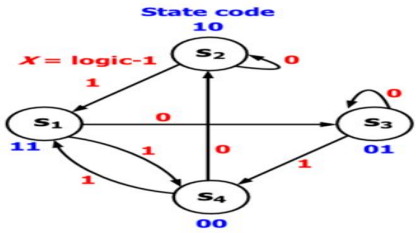


Fig.4 Illustration of FSM

The Boolean elements of A (t) and B (t) can be gotten as appeared:

$$A(t) = \overline{B(t-1)} \qquad [eq.2]$$

$$B(t) = X \oplus B(t\text{-}1) \qquad [eq.3]$$

D. Confinement Analysis on Hardware Utilization

From the conditions [eq.1] and [eq.4], the equipment engineering of both codes might be structured as appeared underneath. Manchester encoding depends upon just XORing activity of CLK and X. However, FM0 relies upon X as well as on the past condition of the FM0 code. The two flip-flops stores the state codes of the FM0 code. The MUX−1 is utilized for exchanging the A (t) and B (t) by choosing the clock signal. Both A (t) and B (t) are acknowledged by [eq.2] and [eq.3], separately. The assurance of which encoding is embraced depends upon the selection of mode bit through MUX−2, in which the mode 0 is for FM0 code, and the mode 1 is for Manchester code.

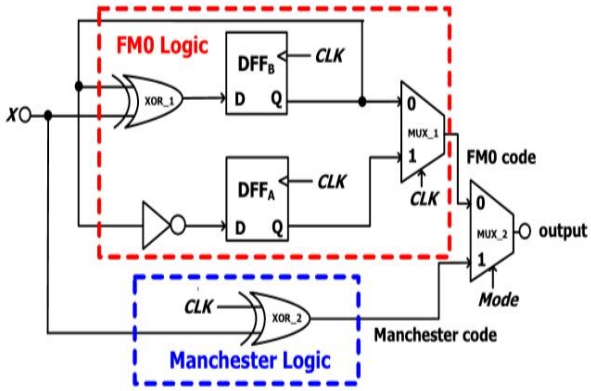


Fig.5 Combined layout using MUX technique

To assess the equipment use, the equipment usage rate (HUR) is characterized as HUR=$\frac{\text{Active Components}}{\text{Total components}} \times 100\%$ [eq.5]

The HUR of both encodings are given in the table underneath. Without SOLS strategy HUR is 57.1% and practically 50% of which get squandered. The coding systems of both encodings are distinctive to such an extent that they limit the plan of completely reusing the VLSI design of Manchester and FM0 encodings on a solitary equipment [12].

TABLE 1 HUR of Encodings

Encoding technique	Active segments / Total segments	HUR
FM0	6/7	85.7%
Manchester	2/7	28.5%
Average	4/7	57.1%

The coding-decent variety between these pair of codes seriously confines the possibility to structure a completely reused VLSI design. Because of these numerous issues, it is hard to utilize the MUX strategy.

E. Problems in the Existing System

In existing system we can perform both encoding operations like FM0 and Manchester operation by selecting the mode bit. The following problems have raised in the existed systems:

1) DC balance
2) The signal reliability enhancing
3) Propagation delay (due to the use of miller encoding)
4) Power consumption
5) Hardware utilization
6) Coding-Diversity

IV. PROPOSED SYSTEM

A. *Architecture Design Using SOLS Technique*

We are utilizing Similarity Oriented Logic Simplification Approach (SOLS) in this paper. This strategy is adopted to decrease the impediments and it is additionally used to progress the equipment use rate [12]. SOLS is likewise called as Similarity Oriented Boolean Simplification Technique (SOBS). The motivation behind SOLS procedure is to structure a completely reused VLSI design utilizing both of them adequately. The SOLS procedure is classed into following sections: Area-compact retiming and Balance logic operation sharing.

B. *Area-Compact Retiming*

This technology deals with the FMO encoder. It moves the equipment asset to decrease the quantity of transistors. The FM0 logic is plainly shown in the Fig.6. The layout shows the FMO rationale as in Mux approach in a rearranged rendition. Be that as it may, if we truly check the two Boolean limits doubtlessly the advancement of state code just reckons upon B(t-1) as opposed to both A(t-1) and B(t-1).

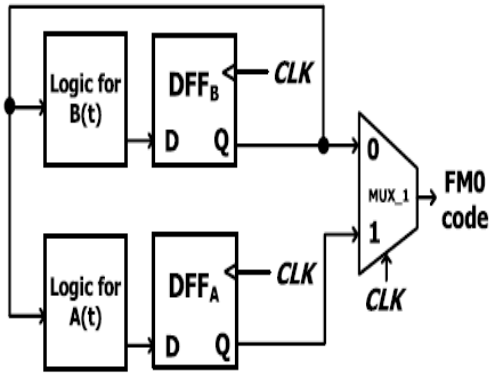


Fig.6 without Area-compact retiming

In this manner, the FM0 just requires a solitary piece flip-flop to store the past state code. Expelling the DFFA legitimately prompts non-synchronization amidst A (t) and B (t) and leads to the rationale deficiency of FM0 code. So to keep up a key good ways from this justification lack, the DFFB is moved soon after the MUX−1, as showed up in Fig. 7. The FM0 code is then again traded amidst A (t) and B (t) through the MUX−1 through the control indication of the clock. In layout , the Q of DFFB is legitimately refreshed from the rationale of B (t) with 1-cycle dormancy.

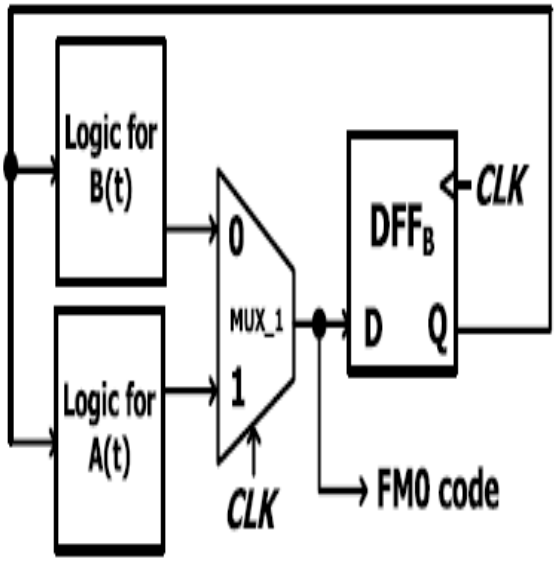


Fig.7 with Area-compact retiming

C. Balance Logic-Operation Sharing

This methodology manages the Manchester encoder. It productively joins FMO and Manchester encodings with the indistinguishable parts. As referred to already, the Manchester encoding will be gotten from X ⊕ clock.

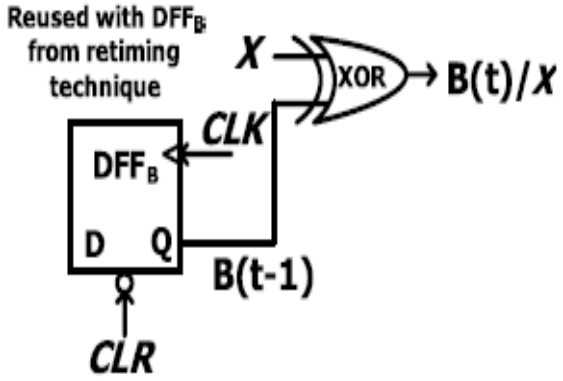


Fig.8 sharing of the reused DFFB

Thus it helps in improving the HUR. The clear is to reset the substance of DFFB to 0. The DFFB can be cleared to zero by method of initiating clear for Manchester. At the point when the FM0 code is embraced, the clear is in the end impaired and the B(t −1) can be obtained from DFFB.

D. Proposed Architecture

The VLSI design utilizing SOLS procedure is appeared in Fig. 9.

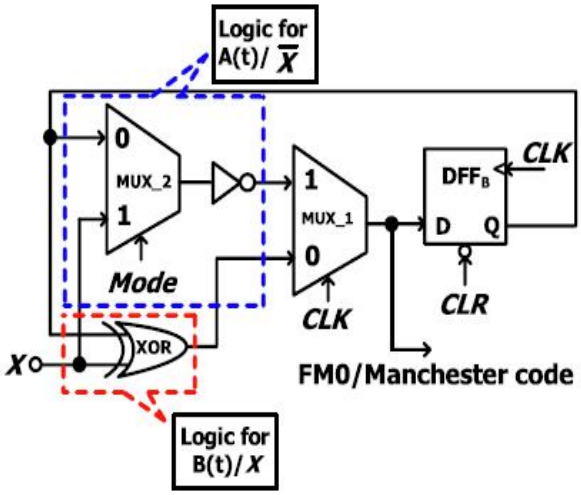


Fig.9 Unstable computation time between A (t) and B (t)

The rationale for A(t)/X just incorporates the MUX−2 and an inverter yet the rationale for B(t)/X joins a XOR gate. In the rationale for A(t)/X the calculation time of MUX−2 is indistinguishable from that of XOR in the rationale for B(t)/X . The rationale for A(t)/X further has an inverter in the arrangement of MUX−2 which prompts unbalance calculation time between A(t)/X and B(t)/X leading the glitch in MUX−1. To wipe out this unbalance calculation time, the design of the parity calculation time between A(t)/X and B(t)/X is appeared in Fig. 10. The XOR in the rationale for B(t)/X has been supplanted with the XNOR with an inverter, after which this inverter is imparted to that of the rationale for A(t)/X and this mutual inverter is moved in reverse to the yield of MUX−1. Along these lines the rationale calculation time between A(t)/X and B(t)/X is equalization to one another. For FMO code both the Mode and CLR bits ought to be zero for example Mode = 0, CLR = 0 and for Manchester code both the Mode and CLR bits ought to be one for example Mode = 1, CLR = 1., CLR = 0 and for Manchester code both the Mode and CLR bits should be one i.e. Mode = 1, CLR = 1.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VI June 2020- Available at www.ijraset.com

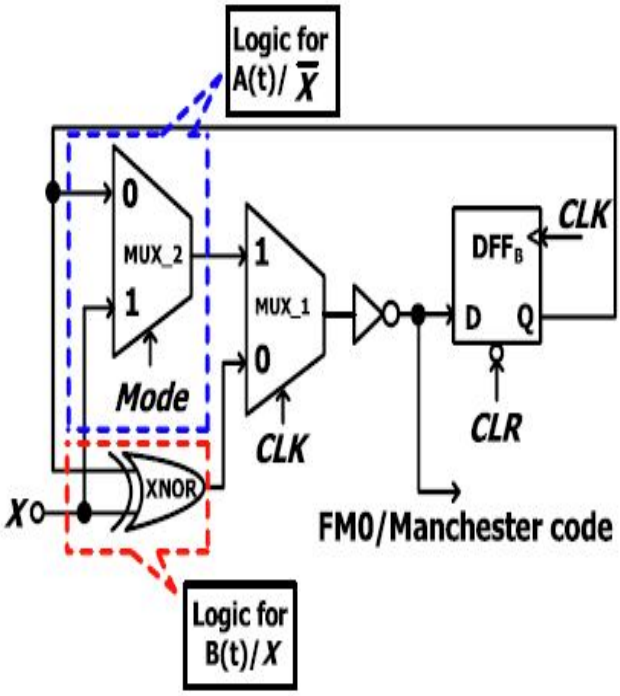


Fig.10 Stable computation time between A (t) and B (t)

E. Work Flow

How the coding calculation will be executed is appeared in the underneath figure. Firstly, the message signal received is sent through either of the encoding methods by choosing the mode bit. For mode bit 0 FMO method is utilized and for mode bit 1 Manchester procedure is utilized. With the aftereffects of those two unique strategies we can shape a condition or a Boolean capacity and looking at the similitudes between both the conditions it can still be reduced to a smaller version. Utilizing these conditions the design is structured and tested. If we get the desired results the operation can be stopped otherwise the reduction of the equations with other alternative methods are used and tested again.

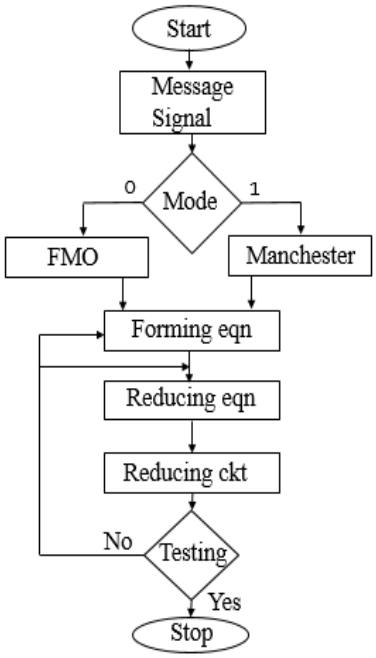


Fig.11 The flowchart of the working algorithm

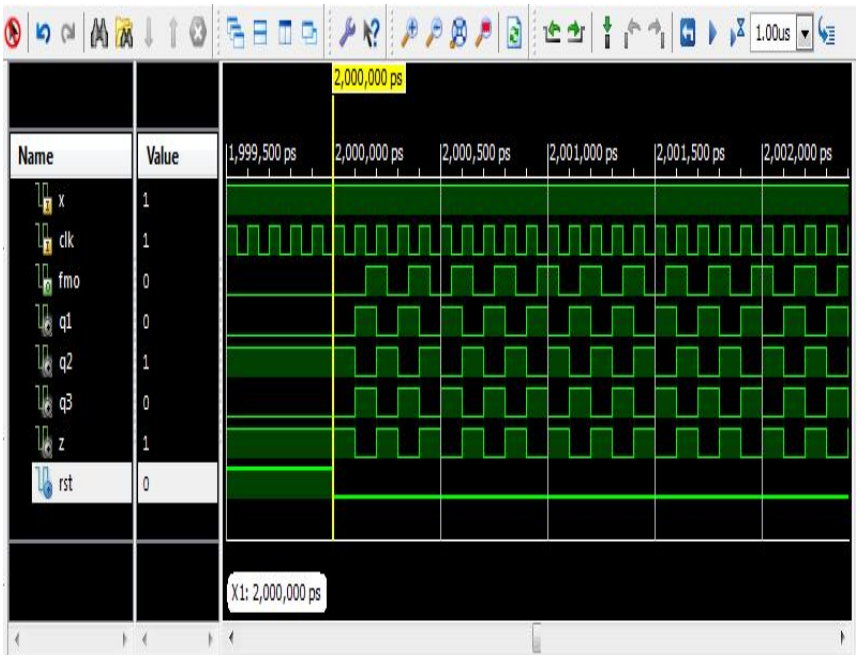
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VI June 2020- Available at www.ijraset.com

V. CONCLUSION

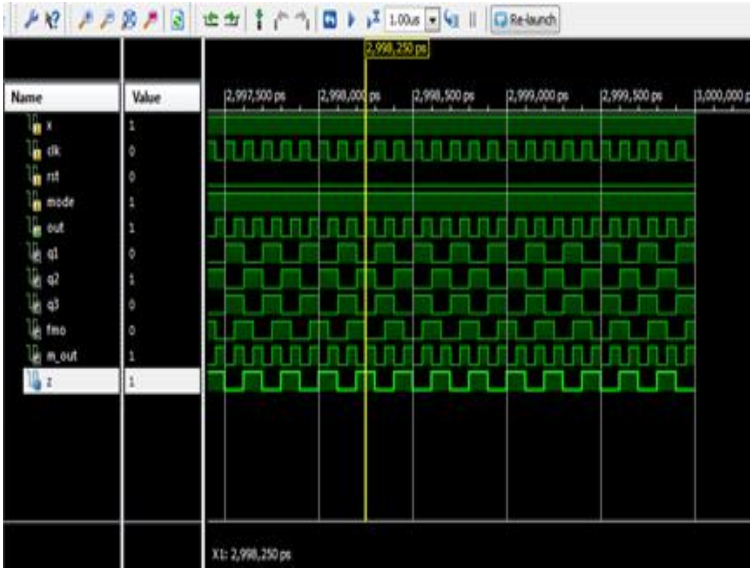
The design strategies of number of scholars exploit the present work and it presents a brief of it. The coding-assortment between two encodings causes the quandary on hardware usage of VLSI structure design. This confinement has been dispensed with utilizing likenesses in the FM0 encoding and Manchester encoding strategies along these lines improving the equipment usage rate. The SOLS method disposes of the restriction on equipment use by two center strategies. The Area-conservative retiming moves the equipment asset to downsize the transistors in this way force and postponement are diminished impressively. The equalization rationale activity sharing proficiently consolidates FM0 and Manchester encodings with the indistinguishable rationale segments because of this the region of the structure has been decreased. This found design of FM0 and Manchester coding exert help to the DSRC standards. The recreation conduct of completely reusable VLSI engineering of FM0 and Manchester encoding with Xilinx ISE 14.7 suite has been solidly approved the utilization of Verilog HDL language.

VI. SIMULATION RESULTS

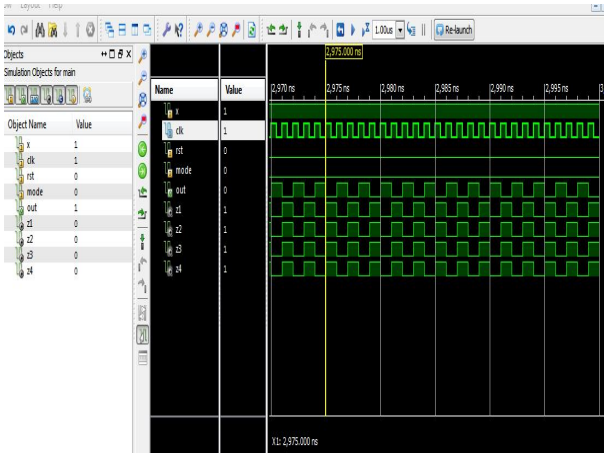
A. Simulation Waveform of FM0 Encoding



B. Simulation waveform for MUX Technique



C. Simulation Waveform for SOLS Technique When Mode is 0



D. Simulation Waveform for SOLS technique When Mode is 1

VII. VARIOUS PARAMETER CALCULATIONS

A. Synthesis report for Delay

```
=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.027ns (frequency: 493.340MHz)
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Delay:               2.027ns (Levels of Logic = 1)
  Source:            x3/q (FF)
  Destination:       x3/q (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: x3/q to x3/q
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             1   0.591   0.424  x3/q (x3/q)
     LUT4:I3->O           2   0.704   0.000  out1 (out_OBUF)
     FDR:D                    0.308          x3/q
    ----------------------------------------
    Total                     2.027ns (1.603ns logic, 0.424ns route)
                                      (79.1% logic, 20.9% route)

=========================================================================
```

Fig 12 Timing constraint using SOLS

B. Power Analysis report

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Static Power
Supply Power (mW)	33.59	0.00	33.59

Fig 13 Power supply summary with SOLS

C. Hardware Utilization Rate (HUR) with SOLS design

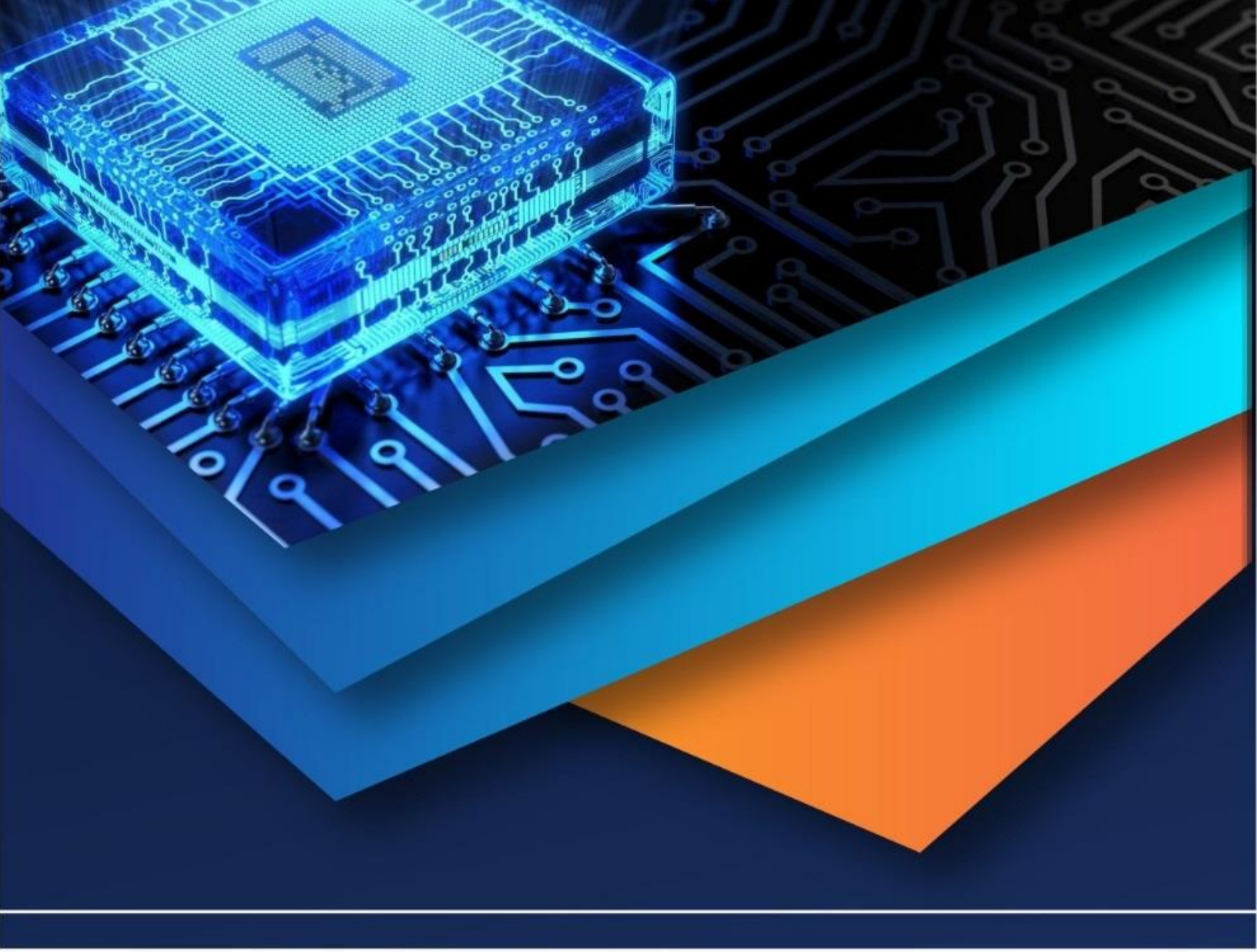
The Hardware Utilization Rate calculation adopting SOLS approach is as shown in the table 5.2 and also the comparison results of both the techniques are shown in the below table 2.

Table 2 Comparison results

PARAMETER	MUX	SOLS
HUR	57.1%	100%
Power	52mW	33.59mW
Delay	5.77ns	2.027ns

REFERENCES

[1] IEEE Std. 1609.3-2010, IEEE Stand for Wireless Access in Vehicular Environments-Networking Services , (2010) December.
[2] Dedicated short-range communications (DSRC) standards in the United States, by Kenney J. B, July (2011), Proc. IEEE, vol. 99, no. 7, pp. 1162–1182.
[3] Design of 5.9 GHz DSRC-based vehicular safety communication, IEEE Trans. Wireless Communication. Mag, October 2006 by Daniel .J, Taliwal .V, Meier. A, Holfelder .W, and Herrtwich .R, volume. 13, no. 5, pp. 36–43.
[4] A Manchester code generator running at 1 GHz, in Proc. IEEE, Int. Conf. Electron., Circuits System, by Benabes .P, Gauthier .A, and Oksman .J, December. 2003, volume 3, pp. 1156–1159.
[5] A 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz, in Proc. 16th Int. Conf. Syst., Signals Image Process, June. 2009, pp, by Karagounis .A, Polyzos .A, Kotsos .B, and Assimakis . N.
[6] VANET: Vehicular Applications and Inter-Networking Technologies, Wiley, Eds, 2010, by H. Hartenstein and K. Laberteaux.
[7] 'Simultaneous PTL buffer insertion and sizing for minimizing Elmore delay', (1998) in Proc. Int. Workshop Logic Synth., pp. 162 by Zhou H., and Aziz A.
[8] A Review of Manchester, Miller, and FM0 Encoding Techniques , Smart Computing Review, vol. 4, no. 6, pp.481-490 by Hemalatha.V, Srividhya.P, Lalitha .V, and Kathiravan .S, December (2014).
[9] High speed CMOS chip design for Manchester and Miller encoder, in Proc. Intel. Inf. Hiding Multimedia Signal Process by Y.C .Hung, Kuo.M.M, Tung.C.-K., and S.-H. Shieh, (2009).
[10] FSM based Manchester encoder for UHF RFID tag emulator, in Proc. Int. Conf. Computer., Communication. Network, December. 2008, by Khan .M. A, Sharma.M, and Brahmanandha .P.R.
[11] Top down design of joint MODEM and CODEC detection schemes for DSRC coded- FSK systems over high mobility fading channels, in Proc. Adv. Communication. Technol, by J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, January. 2013.
[12] Buffer minimization in pass transistor logic, IEEE Trans. Computer. Aided Des. Integr. Circuits Syst., vol. 20, no. 5, pp. 693–697, by H. Zhou and A. Aziz, May 2001.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY