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Verification of Universal Memory Controller with Memory using System Verilog

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Abstract: ***Functional verification mainly based on coverage driven constraint. The universal memory controller is aiming to advance the performance of the prevailing memory controllers through a complete integration of the all memory in addition of providing novel features. It mainly serves as one amongst the basic important feature that's lagging in most of memory controller that is power being consumed. The aim of the paper is to validate the design and to generate regression test cases in the test-bench in order to obtain 100% functional coverage using System Verilog (SV) and a typical code coverage.***

Keywords: *WISHBONE, SDRAM, FLASH*

I. INTRODUCTION

For any electronic device memory plays a major role in reading and writing data into it. For any data to be written or read into memory it requires a prominent element known as memory controller. The very important aspect of memory controllers is to equip reasonable interface and protocol between the host and the memories to efficiently handle data, maximize transfer speed, data integrity and information retention. For SoC(system on chip) having multiple memory many memory controllers may have to accessed for individual memory, Which will add on space in SoC. This design mainly overcome the problem confronted by existing memory controller by addition of novel features. This reduces power being consumed by the design. So, henceforth the design controlling multiple memories to be verified by generating the test cases.

II. UNIVERSAL MEMORY CONTROLLER

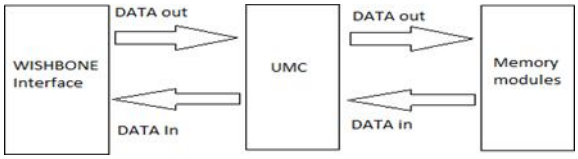

Fig. 1 Proposed Interface Of The Universal Memory Controller

As it can be seen in the Fig-1 the processor connects the controller through wishbone interface and memory module linked to the UMC(universal memory controller). These communicate
when memory requires a signal for particular operations and when request is generated by processor

A. Wishbone Interface

The wishbone interface is a portable IP(intellectual property) core, it is mainly used in semiconductor IP for flexible design methodology. Wishbone mainly possess great features like reusability, portability and trustworthiness for the system. This is can be done by creating a common interface amidst IP cores this results in faster time-to-market for the end user.

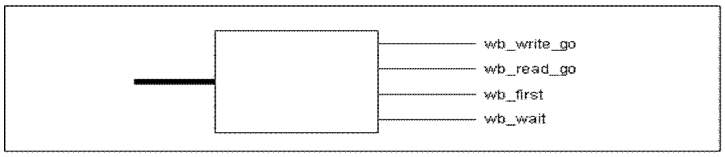

Fig. 2 WISHBONE Interface Block

It supports a 32bit bus width and does not support other bus width. The wishbone interface performs very simple decoding of wishbone signals wb_write_go represent a write cycle, while wb_read_go indicates a read cycle, wb_first denotes the initial transfer of a possible burst, and wb_wait clearly depicts wait state insertion on the wishbone bus.

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B. Universal Memory Controller (UMC)

The memory controller is a digital circuit which manage the flow of data going to and from the main memory. A memory controller can be a individual chip or integrated into another chip, such as being incorporated on the same die or as an core part of a microprocessor; in the other case, it is usually called an Integrated Memory Controller (IMC). A memory controller may also be termed as Memory Chip Controller (MCC) or a Memory Controller Unit (MCU).

The Memory Controller becomes prominent due to following features

1) 8 chip selects, each uniquely programmable
2) Burst transfer and Burst termination
3) Supports RMW(Read Modify Write) cycles
4) Dynamic bus sizing for reading from Asynchronous devices
5) Default boot sequence support
6) Supports power down mode
7) Up to 8*64MB memory size

UMC is sited amidst wishbone and memory module. These blocks are interlinked by wishbone interface, memory interface to the UMC.

C. Memory Modules

A memory module is a printed circuit board on which memory integrated circuits are mounted.

Various memory of which universal memory controller is verified are:

1) Flash Memory
2) Synchronous Dynamic Random Access Memory

III. VERIFICATION OF UMC

The process of evaluating correctness of design and to avoid surprises at a later time, to avoid a re-spin of the chip, to enter the market on time with good quality the verification plays a key role.

In the process of verification, modules are verified by driving the correct and an error input, in both cases need to observe the design whether it is behaving as expected,.

In verification, the exactness of the design under test (DUT) are mainly determined by creating testbench environment

Below is the functionality of the Testbench/Verification environment,

1) Generate stimulus
2) Apply stimulus to the DUT
3) Capture the response
4) Check for the correctness
5) Measure progress against the overall verification goals

Environment contain a generator (gen), Bus Functional Module (BFM), monitor, reference module, coverage, checker and scoreboard

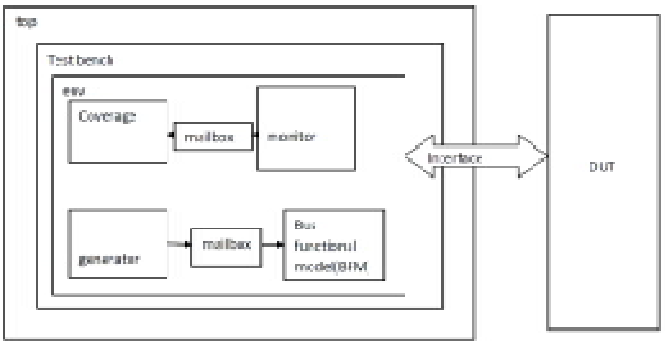

Fig. 3 Testbench environment of wishbone protocol

In Fig 4 Testbench environment of wishbone protocol depicts while in the creation of environment first we start with the top module, followed by creation of generator, bus functional module, monitor, checker, reference module, and interface

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IV. MEMORY INTERFACE TO UMC

A. SDRAM Module

Synchronous Dynamic Random Access Memory(SDRAM) are quicker than Asynchronous DRAM.As it is synchronous in nature changes in clock along with input side causes changes in output. SDRAM memory comprise of four banks, due to which transaction of data happens faster than any other memories

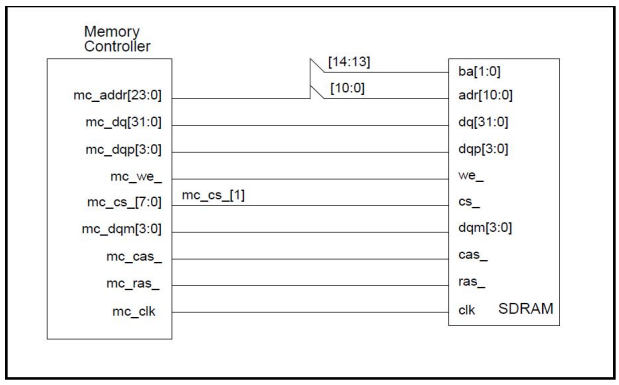

Fig . 4: Interface of SDRAM with Memory Controller

Fig 4:Pin diagram of memory controller and SDRAM both blocks are interfaced by memory interface shown in figure.
The data from memory controller is written to the memory of SDRAM in one address location and from same address location data is read back to the memory controller.

Fig. 4 SDRAM Read and Write

B. FLASH Module

Flash module is a non-volatile memory chip that can only be erased electrically and by reprogramming it. These are mainly accessed whenever the data needs to be stored for a longer interval of time.

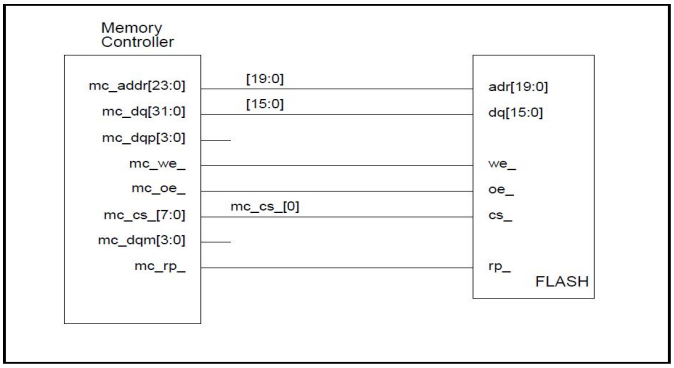

Fig -7: Interface of FLASH with Memory Controller

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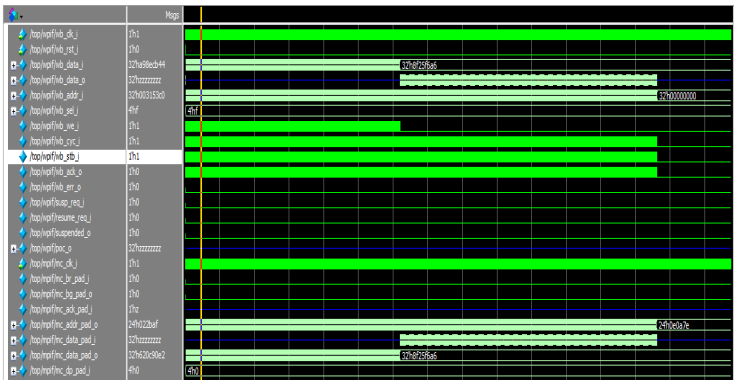

Fig. 8 Flash Readand Write

C. Functional Coverage

Functional coverage is code that observes execution of a test plan. As such, it is code we write to track whether important values, sets of values, or sequences of values that corresponds to design or interface requirements, features or boundary conditions has been exercised.

Functional coverage is important to any verification approach since it is one of the factors used to determine when testing is done. Specifically ,100%functional coverage indicates that all items in the test plan have been tested

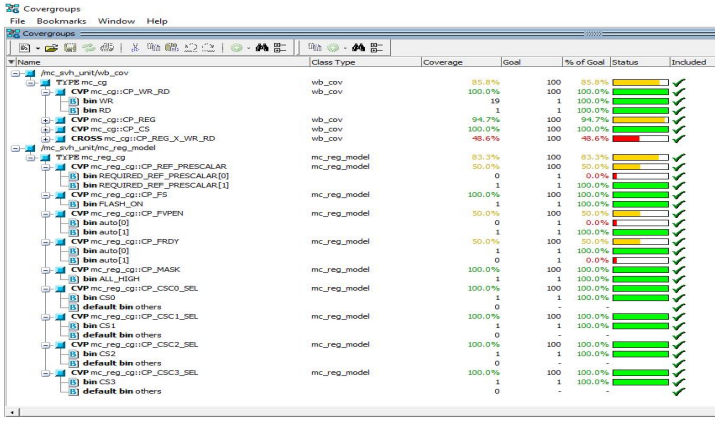

Fig. 9 Functional coverage report

D. Code Coverage

Code coverage tracks what lines of code or expressions in the code have been exercised. Normally there may be cases in which case statement or extra undocumented features in the design may not have not have exercised in normal hardware operation. So in order to either remove or exercise untested feature. So henceforth along with functional coverage its very important to make use of code coverage

Total Coverage:					22.75%	38.24%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	71	48	23	1	67.60%	**84.58%**
Statements	10437	4996	5441	1	47.86%	**47.86%**
Branches	7289	1871	5418	1	25.66%	**25.66%**
FEC Expressions	2100	323	1777	1	15.38%	**15.38%**
FEC Conditions	4117	169	3948	1	4.10%	**4.10%**
Toggles	23992	3497	20495	1	14.57%	**14.57%**
FSMs	295	83	212	1	28.13%	**33.76%**
States	66	29	37	1	43.93%	**43.93%**
Transitions	229	54	175	1	23.58%	**23.58%**
Assertions	10	8	2	1	80.00%	**80.00%**

Fig. 10 Code coverage report

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V. CONCLUSIONS

Memory is the integral part of any processer, comprising of various memory present on SoC. Instead of accessing multiple memory controller for different memory an individual or one memory controller been used called Universal Memory Controller(UMC). In this thesis, various memories possessing different characteristics is been verified. Waveform suggest that data being sent through wishbone and retrieved back to be same and multiple characteristics is been verified . Along with-it functional coverage of 100% is obtained which indicates all functionality of design is verified followed with its code coverage is done to verify all the cases are taken into account .

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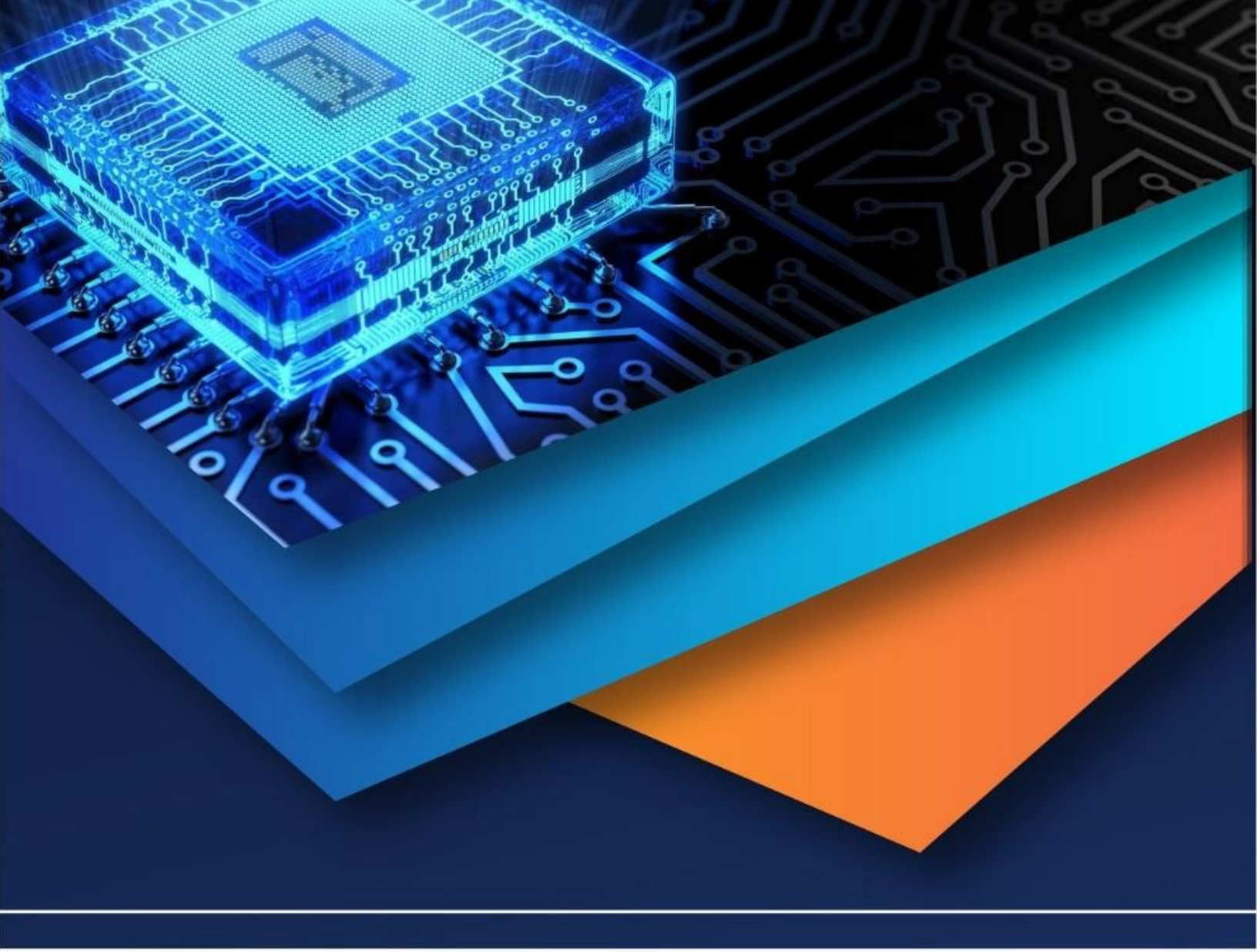

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