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Architecture Design and FPGA Code Development for ADC Module

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Abstract: ***High resolution ADCs play a vital role in designing a system for high end applications where the need for accuracy and preciseness plays a very important factor. In this work, we designed a system where this module will receive the temperature signal; the range of temperature signal varies from 0.0V to 10V dc. We write the necessary HDL code for the FPGA block for this module to read, write, sample and generate the timer pulse from the temperature signal received. In order to achieve a system with higher accuracy, the process of computation and updating of data is done every second. As the system calls for precise measurement it is required to have an ADC of 24-bits. We have written the necessary code and generated the output which shows the data being written on an ADC and after accepting the data how it is read in an ADC and the sampling is performed on the data which is read. In order to achieve the operation under a controlled environment the code for the timer pulse is generated.***

Keywords: FPGA, RTL Structure, ADCs, HDL

I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are silicon devices which are pre-fabricated and are programmed electrically to become any kind of digital circuit [1]. They have numerous advantages over a fixed function Application Specific Integrated Circuit (ASIC) technologies. ASCIs take a lot of time for fabrication and cost a lot of money for its fabrication, whereas FPGAs can be configured at a much faster rate and if any mistake occurs, it could be reconfigured back easily hence it is cost efficient compared to ASCIs. Thus this flexibility of an FPGA comes with a significant cost in area, power consumption and the delay. These disadvantages are caused from FPGA's programmable routing fabric which trades power, area and speed for quick fabrication. Even having such disadvantage, FPGA acts as an alternative for digital system implementation based on their low cost and fast turnaround [1]-[3]. As provided in the Moore's law the access to performance and scaling is given by FPGAs. With the progress of Moore's law, difficulties occurred due to the submicron processes making the design for ASIC very expensive and difficult. Because of such higher expense and a higher return on amount invested drives digital design toward FPGA implementation. A user must employ computer aided design (CAD) tools for FPGA designs. Due to the vast growth in the VLSI technology, it is possible for a designer to design a single chip with more than 100000 transistors. As a result of huge amount of transistors on a single chip, the design complexity increases hence, to verify these circuits on a breadboard was not possible. Hence for design and verification of VLSI digital circuits, computer aided techniques plays a very vital role. Programs to do automatic routing and placement of circuit layouts became very popular.

The designers felt a need to standardize a language for describing digital circuits. Thus Hardware Descriptive Languages (HDL) came into existence. To model the concurrency of processes found in hardware elements was made possible by the HDLs to the designers. A hardware description language (HDL) could be defined as language which is specifically written for describing the behavior and structure of electronic circuit. A hardware description language is written for a precise and correct simulation and analysis of an electronic circuit. One important difference between most programming languages and HDLs is that HDLs explicitly include the notion of time [4]. Especially when it comes to complex circuits, HDL plays an integral part for electronic design automation (EDA) systems such as application-specific integrated circuit, programmable logic devices and microprocessors [5].

The module which we developed would receive the temperature signal as an input to the system. The range of temperature signal is from 0.0v to 10V. The module has to compute the process of writing, reading, sampling from the temperature signal received.

In order to achieve a very high accuracy the process of computation and updating of signal is done in every second, it is required to have an ADC of 22 bits or more for such purpose. The analog signal is passed via an ADC which converts an analog signal to a digital signal which is connected to a FPGA block where the necessary HDL codes are written to perform necessary operations, which is followed by a DAC which converts the processed signal to corresponding analog signal.

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II. FUNCTIONAL REQUIREMENTS OF FPGA

A. FPGA should sample the ADC data and computation must be performed continuously

B. After every computation, FPGA should generate ADC convert signals initiating ADC to acquire data. ADC asserts a busy signal and FPGA should wait till the busy signal is de asserted by ADC. FPGA should initiate a read operation and complete the reading of ADC value.

C. The ADC read is to be done 24 consecutive times to acquire data from ADC to take the average sample values (24samples) if required for future computation. The reading of 24 data samples will be repeated continuously after specific time interval to get the new sample value of ADC data.

III.ARCHITECTURE OF RTL DESIGNFOR FPGA

The design is to be implemented using Verilog HDL as hardware design language. The main functional blocks to be implemented in FPGA are basic timer block, ADC read, ADC write and sampling blocks.

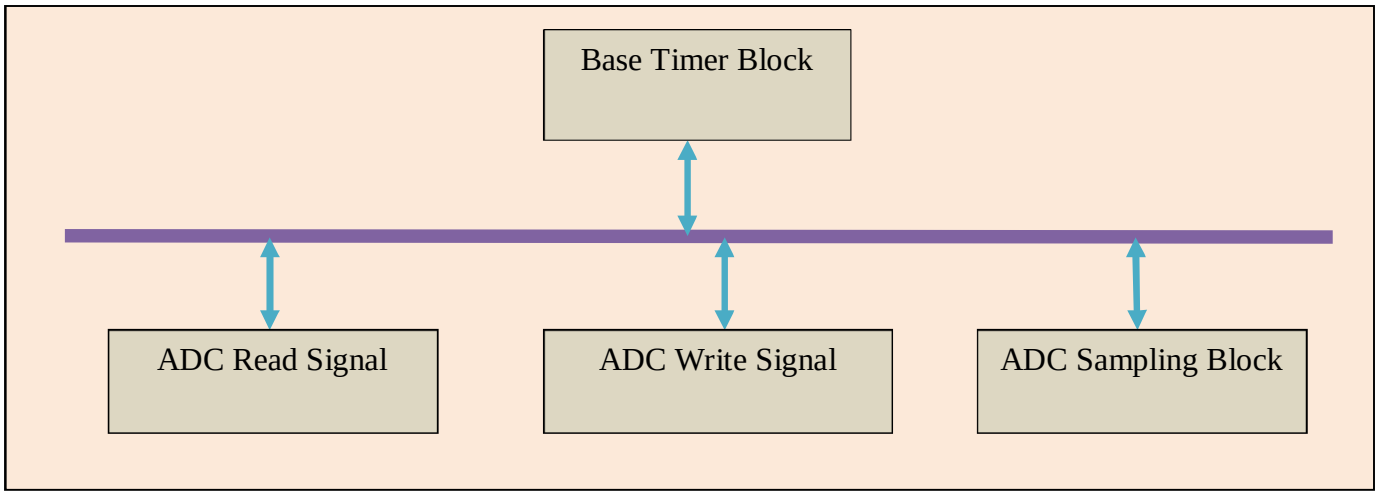


Fig. 1 RTL Design for FPGA

Fig. 1 shows the RTL design, these are the blocks for which the necessary codes would be written for executing the necessary operation. Each block signifies a specific function corresponding from the data read, data write, data sampling by an ADC.

IV. SYSTEM BLOCK DIAGRAM

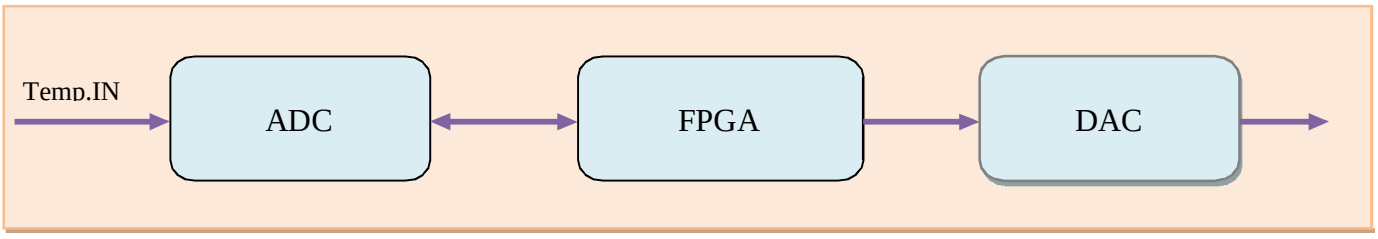


Fig. 2 Block Diagram for the System

Fig. 2 represents the block diagram for a system which consists of several hardware equipments namely being the ADC which converts the analog signal into necessary digital signal which are processed in a FPGA which is programmed to perform necessary functions. The processed digital signal from a FPGA is passed through a DAC which convert these digital signals to corresponding analog signal and is passed through for further operations. The input to an ADC is temperature signal which ranges from 0.0v to 10v dc. The output processed from the FPGA could be altered accordingly to the requirements mainly for high end applications which require for precise and accurate calculations of the signals.

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V. RESULTS AND DISCUSSIONS

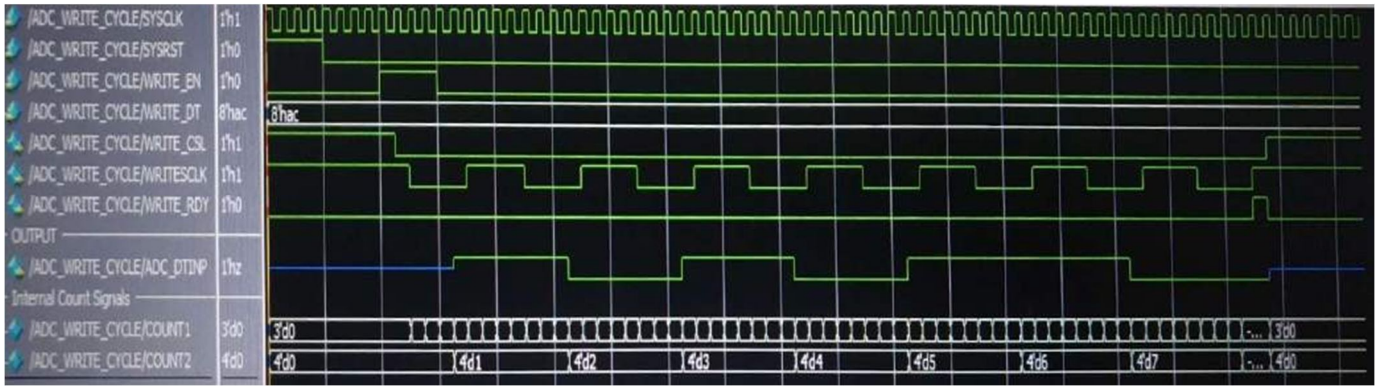


Fig. 3 Result for ADC Write Cycle

The system remains in an ideal state when the reset signal has a value 1. For the system to operate the reset signal should be set to a value 0. The input is a 8 bit signal having value “ac” which corresponds to an equivalent binary value of “1010 1100”. The system starts its operation as soon as an enable signal is triggered which is represented by “WRITE_EN” signal. As soon as the enable signal is triggered the operation begins and the output can be observed respectively “ADC_DTINP“ signal respectively. As soon as the operation is completed a ready signal represented by “WRITE_RDY“ is set to 1 indicating operation is completed .

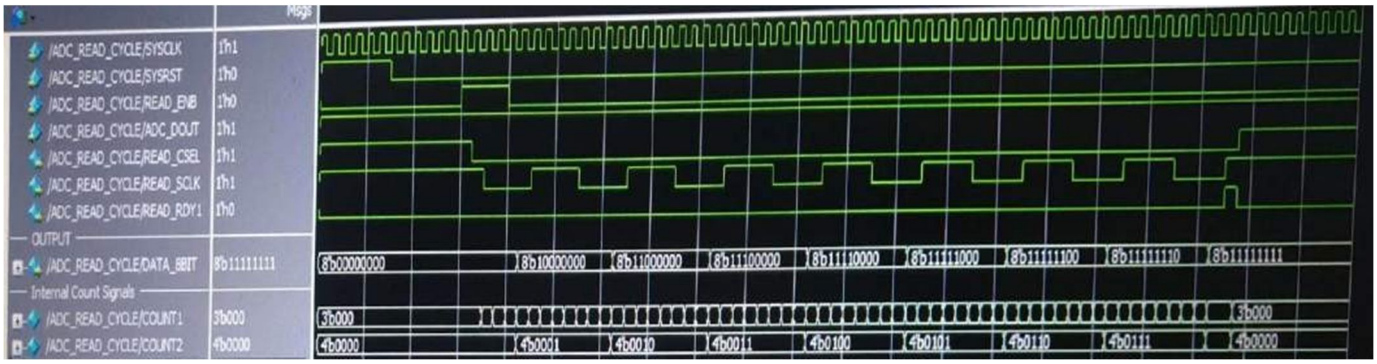


Fig. 4 Result for ADC Read Cycle

Fig.4 represents the result for the ADC read cycle, the system is under an ideal state when the reset is set to 1. The operation starts when the reset to 0 and an enable signal represented by “READ_ENB“ is triggered. “ADC_DOUT“ is set to 1 and we can observe the output represented by “DATA_8BIT“ starting from an intial value which was “00000000“ under ideal condition to “11111111“ at the end of execution. After the execution is completed a ready signal represented by “READ_RDY1“ triggers to 1.

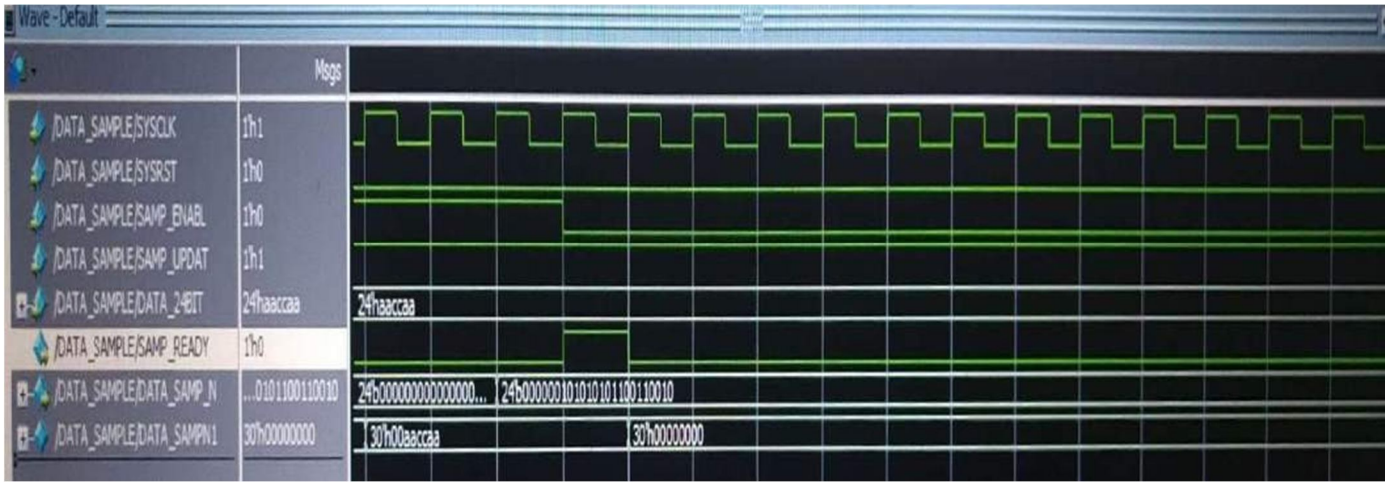


Fig. 5 Result for ADC Sampling Block

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Fig. 6 Result for Timer Pulse Generation

Fig. 6 shows the generation of a timer pulse signal which is a 10ms pulse generated from a 10MHz input signal. It is done for the controlled operation of the system.

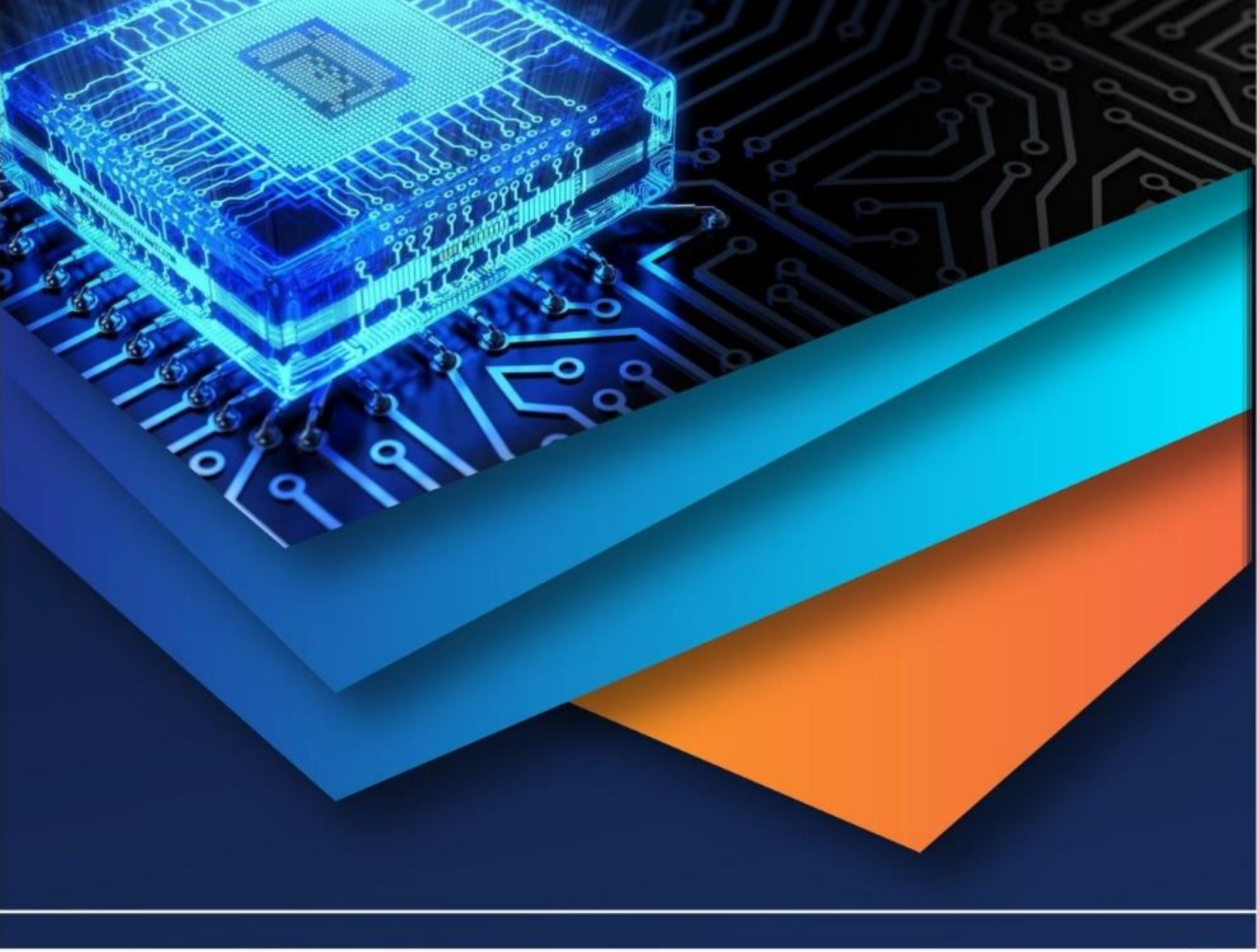
VI. CONCLUSION

We have designed a system and written necessary HDL code for an FPGA block for the ADC operations namely being ADC read, ADC write, ADC sampling. The timing pulse has been generated in order for a system to operate under a controlled environment. The results obtained are represented using pulses and the obtained results are checked and verified. This ADC operation plays a vital role when it comes for high end applications where the results to be obtained must be highly accurate and precise.

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