iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 8 **Issue:** VII **Month of publication:** July 2020

DOI: https://doi.org/10.22214/ijraset.2020.30027

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VII July 2020- Available at www.ijraset.com

Full Adder using Reversible Logic

Sonam Dixit
Student, Department of Electronics and Communication, PSIT College of Engineering, Kanpur, India

Abstract: ***Reversible logic gates are very popular among upcoming future computing technologies. In the field of quantum computing ,low power VLSI devise, nanotechnology, DNA computing optical computing , quantum-dot cellular automata reversible logic circuits have various applications which are helping the world to do their work more easily [3]. Despite them, Quantum computers are the another major application of reversible logic ,these are certain areas in which the quantum devices are essential, with less power dissipation and at ultra high speed these devices can be ideally operated, these devices must build from reversible logic components, such requirements and versatility of reversible logic makes the reversible logic as one of the most versatile area for the researchers to discover new devises based on it and bring a revolutionary change in the field of computing technologies and various other fields in which reversible logic is a better option to be used in the past few decades .In past few decades reversible logic has became the major source of designing the modern circuits which can be helpful in various devices. Along with space and power, the delay is one of the significant issues in VLSI design. Reversible logic is becoming a huge source of research day by day, having the area for research in the designing of the complementary metal oxide semiconductor field effect transistor with the small amount of power consumption. The design proposed in the paper of full Adder circuit is one of the example of such circuit which is implemented by using reversible logic gates and hence the design proposed in this paper operated as reversible full adder. With much lesser complexity in the terms of hardware and lesser efficiency in terms of undesired outputs , gate count and same input the proposed design is most reliable than the presented ones. The reversible logic gates provided us a drastic change in the operation of electronic devices by using of fast switching operation of the gate used in the designing of reversible logic structure. Finally we can say that from the above illustration the reliability of the proposed design is increased .***

Keyword: Reversible, Fredkin gate, full adder, delay.

I. INTRODUCTION

In the present era the reversible logic design is gaining more attention due to its zero energy dissipation as no energy is being lost and low power consumption as the power consumed by it is less. Under the ideal condition the power dissipation of reversible logic is zero [1]. The relation between input and output reversible circuits have a monotonic mapping , thus, the vector of the input stage can always reconstruct from the output stage vectors. Rolf Landauer, in 1961, stated that whenever we use a logically irreversible gate, we dissipate energy in the surrounding

INFORMATION LOSS=ENERGY LOSS

That is the loss of one bit of information dissipate KTln2 of energy in irreversible gate due to which the heat energy dissipated, which degrade the output and result in the drop of the duration of the component. therefore due to this loss of information certain adverse effect on components may occur. Whereas in the reversible gate, no information is lost, hence there is no adverse effect on components, which leads to improvement in energy efficiency improvements and performance. which results into a improved version of circuits.

The scientist Bennett has shown in 1970's that if the network permit the regeneration of the input by help of output then energy will not liberated from the system will not equal to KTln2[1]. The reversible logic consist of both frontend and backend. In Reversible logic the system follows the process of running both forward and backward. Therefore by computing backward we easily recover the earlier stage.

Reversible logic is the most convenient and efficient way of designing the circuits. Some important logic gates in reversible logic gate Feynman gate, double Feynman gate, Friedkin gate, Toffoli gate, Peres gate, etc. Reversible compute have certain uses in the field of computer security and low power CMOS, quantum Computer nanotechnology and many more [4]. It has a vast field of application. Reversible logic can be applied in the implementation of various technologies it is helpful in designing different kinds of circuit for different applications. These logic gates having the capability to store the information in them without any loss of data during the system processing. These gates also maintain the system integrity and makes the data confidential.

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VII July 2020- Available at www.ijraset.com

II. TERMINOLOGY USED

A. Reversible Logic Gate

It is not only advised us to showcase the outcomes for inputs but also advised incompatibility for maintaining the inputs from the results[1]. This logic suggests us to show the results for the inputs but also it provides the suggestion about the unusual condition between the inputs and outputs.

B. Garbage Output

for maintaining n to n mapping to an n*n gate, some outputs are not used. These unused outputs are said as garbage outputs. The garbage outputs should be as less as possible. Garbage output is the unused output the outputs which are not used in further calculations of desired output or not taken as a output. Garbage outputs are such kind of outputs which are neither used as an desired output nor as an input to the another gate[1].

C. Quantum Cost

Quantum cost is the total number of parent gate's costs present in the circuit. The quantum cost is understand by the sum of all costs of the gates inbuilt in the circuit basically the quantum refers to the packet (bundles) and its value is not more than the 4 integrated circuits (IC's) cost. This is because it provides the designing cost part of a initial gate. The results which should observe during the processing of gates not affected[9].

D. Flexibility

It is associated with collection of reversible logic gates, which performs various tasks .reversible logic gates have flexibility as they can perform different works in various fields of technology. The reversible logic has versatility of doing multitasks at a time so that many different kinds of work can be done successfully in very less time. Also the integrity of the system is maintained.

E. Gate Level

which associates the part of tasks in the designing, which is beneficial to receive the connection .Various different kinds of reversible logic gates are connected in a circuit in different levels which can perform variety of tasks according to the requirements are known as gate level. The gate level refers to the components of the design process also this gate level enable to establish the connection between the user and the equipment. Therefore the gate level act as a bridge between the circuit and outside world.

III. REVERSIBLE LOGIC GATE AND ITS PERFORMANCES

The gate has monotonic mapping between input and output vector; thus, the input can always reconstruct from the output , and vice versa and no information or energy lost is reversible logic gates [6].

A. Feynman Gate

Feymnan gate represented in fig 1 is also said as (C-NOT) gate. By using the combination of C-NOT gate any of the quantum circuit can stimulated. In Feynman gate, input and output order pair is given by L is corresponding to P and M corresponding to Q.
The output L is given as: L equals P

$L=P$ ----(1)

And the output M is given as: M equals to P xor Q

$M=P \oplus Q$.--(2)

Feynman gate can use as a copying gate. One is the Quantum cost of Feynman gate. The truth table is shown in table 1.

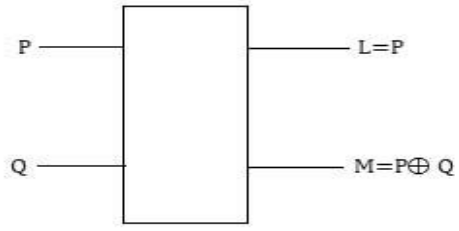


Fig1: Feynman Gate

©IJRASET: All Rights are Reserved

Table 1: Truth Table

P	Q	L	M
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. Double Feynman Gate

In Double Feynman gate as represented in fig 2 the outputs (L,M,N) are given corresponding to the inputs (P,Q,R).
In this the output L is given as: L equals P
L=P -----(3)
The output M is given as : M equals to P xor Q
M= P⊕Q -----(4)
The output N is given as: N equals to P xor R
N=P⊕R------(5)
The truth table for each possible condition is shown in table 2.

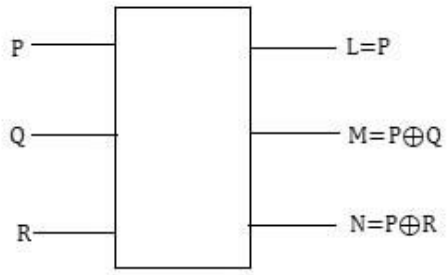


Fig2: Double Feynman Gate

TABLE 1: TRUTH TABLE

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VII July 2020- Available at www.ijraset.com

C. Toffoli Gate

Toffoli gate as represented in fig 3 is also said as (CCNOT) gate. It is a universal reversible gate that is any reversible circuit can be implemented with the help of this gate. In Toffoli gate, the outputs L,M and N are given corresponding to the inputs P,Q and R .

In this the Output L is given as: L equals P

L=P -----(6)

The output M is given as:

M equals Q.

M=Q -----(7)

And the output N is given as :N equals to the product of P with Q then xor with R

N=PQ⊕R. -----(8)

It have a quantum cost 5. The truth table for each possible condition is shown in fig 3.

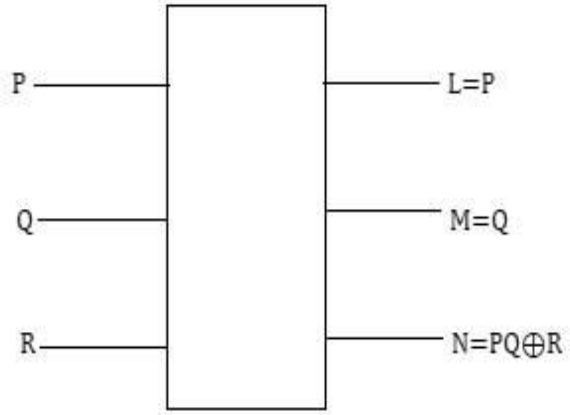


Fig3: Toffoli Gate

Table 3:Truth Table

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	0

©IJRASET: All Rights are Reserved

D. Fredkin Gate

Any logical or arithmetic operation can be performed easily by fredkin gate, this gate as represented in fig 4 is also said as (CSWAP) gate. In Fredkin gate, the outputs L, M and N are corresponding to inputs P, Q and R.

In this the output L is given as: L equals P

L=P -----(9)

The output M is given as: M equals to the product of P with Q and product of P with R and then xor of both the products

M=PQ⊕PR ------(10)

And the output N is given as : N equals to the product of negation P with R and product of P with Q and then xor of both the products

N=P'R⊕PQ ------(11)

It have a quantum cost 5. The truth table for each possible condition is shown in table 4.

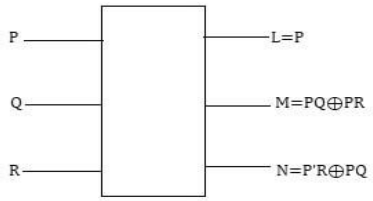


Fig4: Fredkin Gate

TABLE 4:TRUTH TABLE

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

E. Peres Gate

In Peres gate as represented in fig 5 , the outputs L,M and N are obtained by the inputs P,Q and R.

In this gate the output L is given as: L equals P

L=P ------(12)

The output M is given as: M equals to P xor Q

M=P⊕Q -----(13)

And the output N is given as: N equals to the product of P with Q , xor R.

N=PQ⊕R. ------(14)

It have a quantum cost 4. The truth table for each possible condition is shown in table 5.

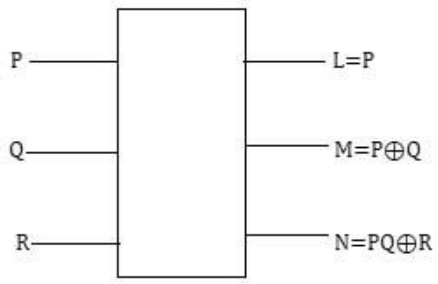


Fig5: Peres gate

©IJRASET: All Rights are Reserved

Table 5: Truth Table

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

F. TGS Gate

In TGS gate as represented in fig 6 , the output L, M, N and O is derived by the inputs P, Q ,R and S. This gate works on the principle of Boolean algebra.

hence the Output is L is given as: L equals P

L=P----(15)

The output M is given as: M equals to the xor of product of complement of P with Q, product of P , with R

M=P'Q⊕PR -----(16)

And the output N is given as: N is equals to the xor of product of complement of P with Q, product of P , with R ,xor with S.

N=P'Q⊕PR⊕S ----(17)

And the output O is given as: O is equals to the xor of product of P with Q, product of complement of P with R xor with S

O=PQ⊕P'R⊕S. -----(18)

The truth table for each possible condition is shown in table 6.

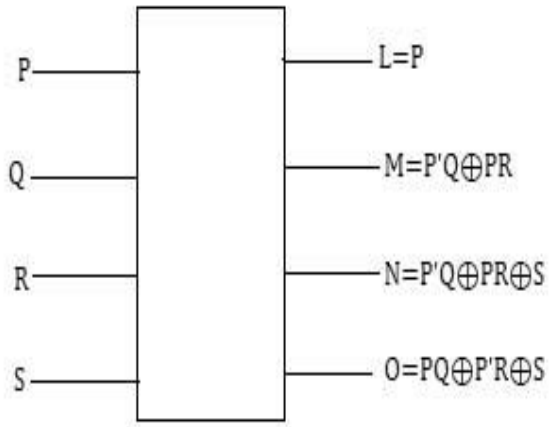


Fig6: TGS gate

©IJRASET: All Rights are Reserved

Table 6: Truth Table

P	Q	R	S	L	M	N	O
0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	1
0	1	1	0	0	0	1	1
0	1	1	1	0	0	0	1
1	0	0	0	1	1	0	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	0
1	1	1	1	1	0	0	0

G. Sayem Gate

In Sayem gate as represented in fig 7 the output L, M, N and O are expressed with the help of P,Q,R and S.

Hence the output is given as: L equals P

L=P -----(19)

The output M is given as: M equals to the product of complement of P with complement of R, then xor with complement of Q.

M=P'R'⊕Q'-------(20)

The output N is given as: N is equals to the xor of product of complement of P with complement of R, with Q, xor with complement of S

N=[P'R'⊕Q]⊕S' ------(21)

The output O is given as: O equals to the xor of product of complement of P with complement of R ,with complement of Q, multiply with S, xor of xor of product of P with Q ,with R

O=:[P'R'⊕Q']S⊕ [PQ⊕R]. ---(22)

The truth table for each possible condition is shown in table 7

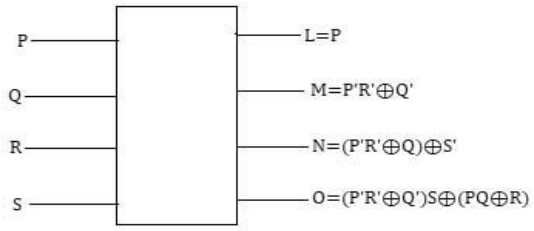


Fig7:Sayem gate

©IJRASET: All Rights are Reserved

Table7:Truth Table

P	Q	R	S	L	M	N	O
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	1

H. New Gate (NG)

It is a square of three reversible gate with certain complex operations. the gate input as represented in fig 8 is[P, Q, R] [7].

Hence the output L is given as: L equals P

L=P -----(23)

The output M is given as: the output M is equals to xor of product of P with Q, R

M=PQ⊕R ----(24)

And the output N is given as: The output N is equals to xor of product of P complement with R complement ,complement Q .

N=P'R'⊕Q'. ----(25)

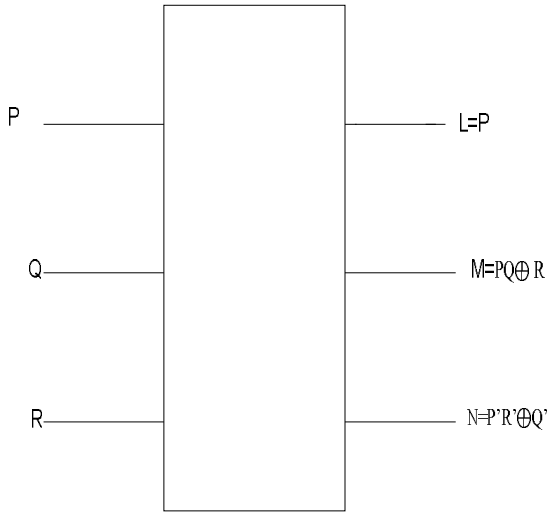


Fig 8: New gate

©IJRASET: All Rights are Reserved

IV. FULL ADDER

A Full adder as represented in fig 9 is define as a logical circuit that implements an addition operation on three one bit binary numbers as it takes two inputs, a carry-in, and produces the output as sum and carry out [2]. The addition of three binary digits which has three inputs and two outputs where Cin is the previous carry is performed by the full adder circuit [10] . In the proposed full adder, there are total three inputs [A,B] and Cin where Cin stands for carry input, which generates the sum =[A⊕B⊕Cin], carry=[(A⊕B)Cin⊕AB] [5] . The full adder circuit contain eight combinations of three bits input .

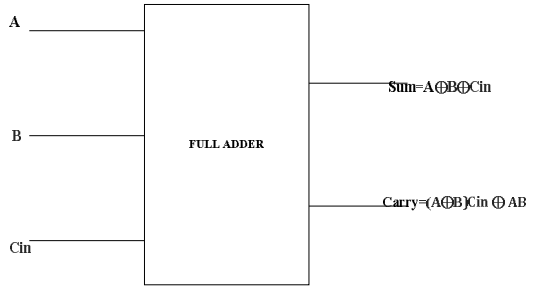
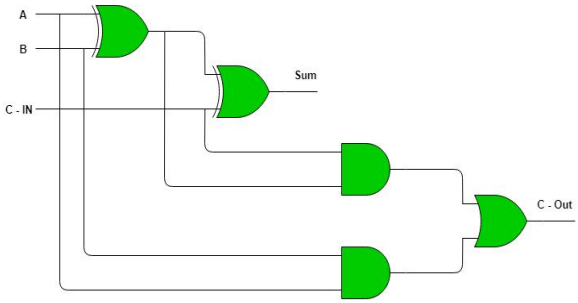


Fig 9: full adder



Hence in this logically irreversible full adder, there is a dissipation of energy, which provides the reduction in one bit of input or data to prevent this dissipation of energy a reversible full adder design proposed which is several times better than the existing full adder circuit in every field.

V. REVERSIBLE FULL ADDER

A. Proposed Design 1

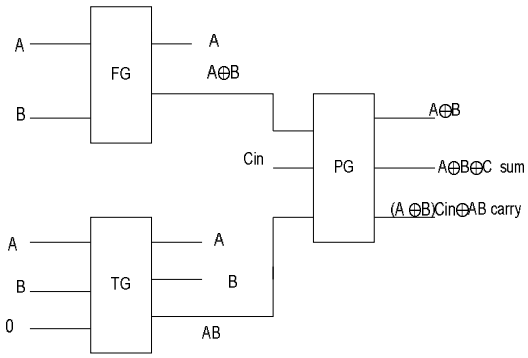
The proposed full adder implemented using Peres gate, Feynman gate, Toffoli gate. This adder has garbage output four, and the cost of quantized bit is 10.proposed circuit is the most reliable one as it has less quantum cost, garbage output, and delay. The proposed design is much competent and convenient than presented ones. In this presented reversible full adder there total three inputs [A,B] and (Cin) where Cin is a carry input, which generates the sum of inputs as:

Sum is given as : xor of A,B and Cin

sum=[A⊕ B⊕ Cin]

carry is given as: xor of(A,B)then multiplication with xor of Cin , product of A,B.

carry=[(A⊕B)Cin⊕AB].



Design 1: Reversible Full Adder

©IJRASET: All Rights are Reserved

B. Proposed Design 2

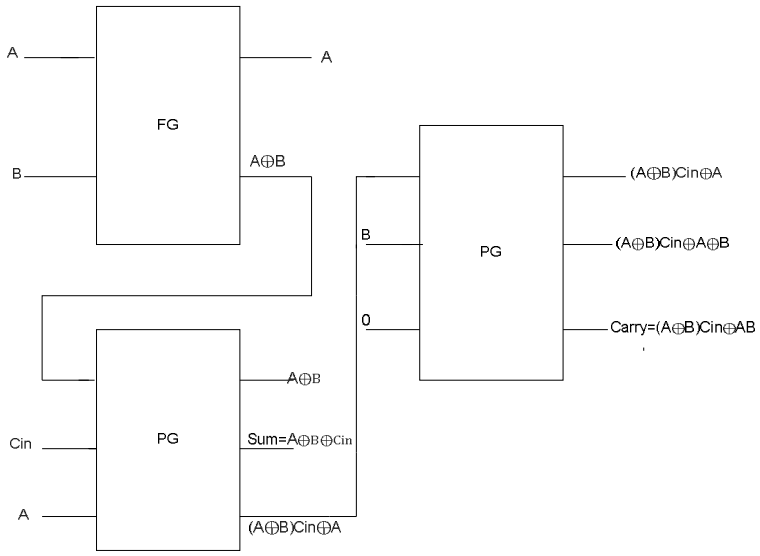
The proposed full adder implemented using Peres gate, Feyman gate .this adder has garbage output five, and the cost of quantized bit is 9.proposed circuit is the most reliable one as it has less quantum cost, garbage output, and delay. The another proposed design is also much efficient and convenient than the existing ones. In this presented reversible full adder there are total three inputs [A,B] and (Cin) where Cin is a carry input, which generates the sum of inputs as:

Sum is given as : xor of A,B and Cin

sum=[A⊕ B⊕ Cin]

carry is given as :xor of(A,B)then multiplication with xor of Cin , product of A,B.

carry=[(A⊕B) Cin⊕AB].



Design 2: Reversible Full Adder

VI. RESULT

As in the paper [8], the proposed full adder has a quantum cost of 28 and garbage output 7. In comparison to that paper, the reversible Full adder successfully implemented here using the Toffil gate, Peres gate, Feynman gate having input (A, B, C), and the desired output sum=A⊕B⊕Cin, carry=(A⊕ B)Cin⊕AB .Having quantum cost. Having quantum cost ten and garbage output four which is much less than the other discussed paper, so it is much better than the full adder implemented in paper[8].

The comparison is shown below:

	Existing design[8]	Proposed design 1	Proposed design 2
No.of gates used	9	3	3
Quantum cost	28	10	9
Garbage output	7	4	5

VII. CONCLUSION

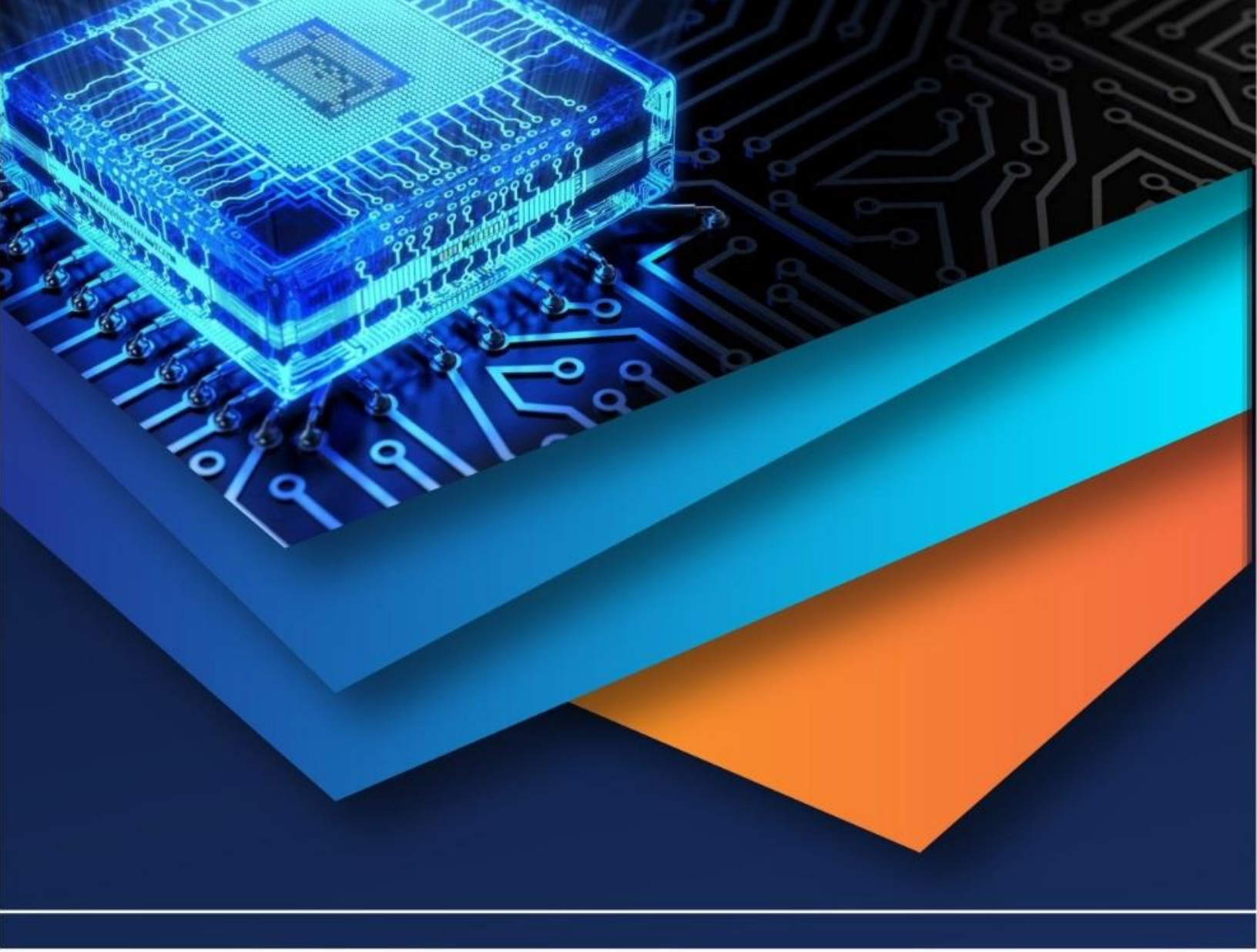
The major aim of this paper is to design a full adder using reversible logic as it is more relay able than a normal adder. The proposed circuit design in such a manner that it is more efficient. The improved adder has less garbage output, quantum cost, and delay. Using such circuits can be helpful in terms of cost reduction of the circuit as well as in terms of saving the power. Such circuits are dissipation free. using such circuits in the implementation of any technology is more convenient and reliable. These reversible logic gates played a vital role in the designing of various electronic equipments. These equipments have the capability of doing multitask at a time without any deviation from the desired result. The reversible logic gates is eventually most efficient for the designing of various electronic circuits rather than the basic logic gates.

©IJRASET: All Rights are Reserved

REFERENCES

[1] Prashant .R.Yelekar, Prof. Sujata S. Chiwande, " Introduction to Reversible Logic Gates & its Application" 2nd National Conference on Information and Communication Technology (NCICT) 2011 .
[2] Parminder Kaur ,Balwinder singh Dhaliwal," Design of Fault Tolearnt Full Adder/Subtarctor Using Reversible Gates" International Conference on Computer Communication and Informatics (ICCCI -2012), Jan. 10 – 12, 2012.
[3] Divyansh Mathur, Arti Saxena, Abneesh Saxena," Arithmetic and Logic Unit Designing Using Reversible Logic Gate" International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-1, Issue-6, January 2013.
[4] Rakhi Saha, Sambita Dalal," A Novel Reversible Combinational Circuit Design for Low Power Computation" IEEE Power, Communication and Information Technology Conference (PCITC) 2015.
[5] Gowthami P, RVS Satyanarayana "Design of Digital Adder Using Reversible Logic" Gowthami P Int. Journal of Engineering Research and Applications ISSN: 2248-9622, Vol. 6, Issue 2, (Part - 1) , pp.53-57 February 2016.
[6] Umesh Kumar,Lavisha Sahu, Uma Sharma," Performance Evaluation of Reversible Logic Gates"IEEE 978-1-5090-5515-9/16/2016
[7] Gopi Chand Naguboina, K.Anusudha," Design And Synthesis Of Combinational Circuits Using Reversible Decoder In Xilinx" IEEE International Conference on Computer, Communication, and Signal Processing (ICCSP-2017).
[8] Ruqaiya Khanam Abdul Rahman Pushpam,"Review on Reversible Logic Circuits and its Application" International Conference on Computing, Communication and Automation (ICCCA2017)
[9] Joyati Mondal , Debesh K. Das, "Design for Testability Technique of Reversible Logic Circuits Based on Exclusive Testing" IEEE 26th Asian Test Symposium 2017.
[10] Dr. B. Balaji , M.Aditya , Dr.Erigela Radhamma, Dr.Venkatrami Reddy, Dr.Y Naresh "Full adder\subtractor using reversible logic"International Journal of Pure and Applied Mathematics Volume 120 ,437-446 April 6, 2018.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)