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Multilevel Inverter Topology with Self-Balancing Voltage and Modularity in Design

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Abstract: ***Multilevel inverters have already gained high popularity among research teams as well as in production of high and medium-voltage applications for industrial purposes over the period of twenty years. Moreover, multilevel inverters are able to generate switched waveforms with reduced levels of harmonic sag compared to a conventional converter. Recent increased interest in multilevel inverters is due to their ability to generate high quality output waveforms at lower switching frequencies; the multilevel topology used in dynamic voltage restorer works towards the reduction of the total harmonic distortion counting all of the losses at the output end. This paper provides a new topology for the modulation in the multilevel inverter using switched capacitor. The self-balancing capability for the capacitor voltage and the SC connected in parallel so as to provide the voltage setup. The methodology presented works towards minimizing the THD by implementing the 9 level MLI and comparing the same to the other level in terms of distortion. The factors like cost are also considered in the design for which half bridge is being used.***

Index Terms: Multilevel Inverter; H-Bridge; Self-Balancing; Topology; Diode; Capacitor; Modulation.

I. INTRODUCTION

Multilevel inverters have become popular in medium and high voltage power industry during recent years. Sustainable energy sources such as fuel cells, photovoltaic and wind can be broadly interacted with a multilevel converter system [1]. The fundamental principle of multilevel converter is that ac waveforms is synthesized from numerous levels of voltage, generated by isolated dc sources or bank of capacitors. This concept is inherited from the converter topology introduced by Baker [2]. A lot of multilevel converter topologies have been suggested over the last decades. Likewise, unique modulation schemes and novel converter topologies are invented. This

literature review is divided into four parts. First, the three topologies of multilevel converters are covered in the literature review: the neutral-point-clamped converter (NPC), Cascade H-Bridge (CHB) and flying capacitor converter (FC).

Second part discusses modulation techniques such as apace vector pulse width modulation and sinusoidal pulse width modulation (SPWM). Lastly, the implementations of multilevel converters in industrial applications used in such fields as renewable energy systems with utility interface and industrial medium-voltage motor drives.

Multilevel inverter are majorly used in the application where the high voltage is required and also over the system which are working over the renewable sources for power generation, HVDC systems, and in many of the energy transmission systems. In 1981, Nabae[3] used the multilevel word for three level inverter and beyond the work the levels were further elaborated to many more levels. The defined inverters are the combination of the several components working parallel like semiconductor, capacitors, PV arrays, DC sources, etc. For the successful execution of the MLI various topologies are defined from which the Neutral point clamped and flying capacitor are majorly used in the real time applications, where the staircase waveform is generated by connecting the capacitors and switches. In the case when the different or multiple DC sources like solar cells are incorporated in the system cascaded H-bridge topology is being used [4].

The accessible work gives the depiction belonging to multilevel inverter along reference to many features regarding inverter. The segment below delivers the exact particulars provided within the section II showcase the fundamentals belonging to multilevel inverter, however the particular segment number III made out regarding many employed topologies belonging to multilevel inverter, Section IV describes about the various controller policies regarding these multilevel inverter, Section V arrangements along self-balancing considering voltage within multilevel inverter, Segment V regarding the different research implemented within ground extent along with Section VI arranges the work finished.

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II. MULTILEVEL INVERTER TOPOLOGIES

Normally, the listed were the three known along with traditional topologies belonging to multilevel inverter. Given are as same shown below

1) Flying capacitor (FC) or capacitor clamped
2) Neutral point clamped (NPC) or diode clamped
3) Cascaded H-bridge (CHB)

Within the current scenario, researchers made overwhelmed multilevel inverter tour's difficulty through switches preparation that actually assisted inside manufacture belonging to totally new diversity considering topologies: hybridized cascaded H-bridge (HCHB) multilevel inverter , active stated NPC (ANPC) multilevel inverter, switched series/parallel sources, modular multilevel converter (MMC), two-level power modules (HBTPM)-based multilevel inverter.

A. Neutral Point Clamped Multilevel Inverter

The known type of this is called as Neutral point clamped (NPC) inverter which was earlier initiated within the year through Nabae et al. [5]. That was being taken into account with primary being denoted as kind of multilevel inverters, called denoted as 3-level NPC.

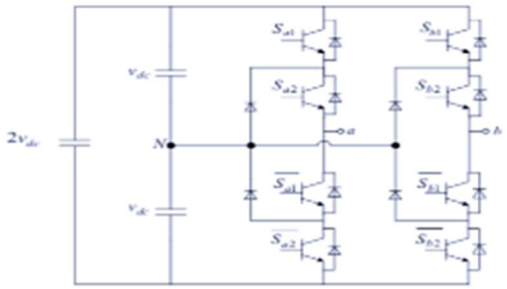

Fig. 1 Neutral point clamped multilevel inverter

B. Flying Capacitor Multilevel Inverter

Within mid-1990s, Meynard along with Foch [6] in addition Lavieville et al. [7] presented flying capacitor (FC) inverter that is being taken in the form of additional alteration belonging to multilevel inverter topology. The base corresponding with implicated inverter considered to be consumption that of particular capacitors. Which are being made through merging up a chain capacitors clamped switching cell? Few voltages were being also changed and altered within their electrical devices by the aid of capacitors.
The swapping conditions inside FC inverter were being same to NPC inverter. But, clamping diodes were not being required for this kind of topology belonging to multilevel inverter. The compensations considering these inverters do pursue and correspondingly have idleness of swapping inside the level made resulted into harmonizing FC.

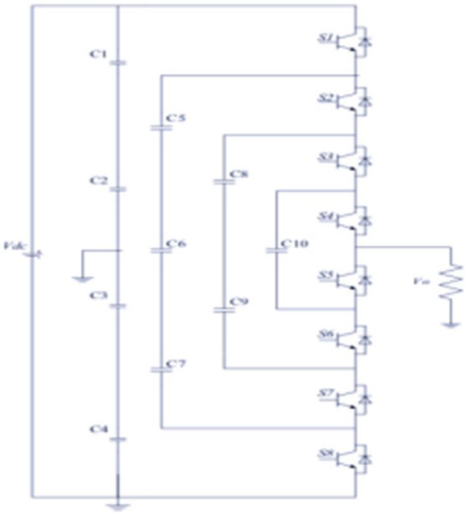

Fig. 2 Flying capacitor multilevel inverter

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C. Cascaded H-Bridge Multilevel Inverter

Within the mid belonging to that of 1970s, Baker and Bannister [8] labelled the principal flagrant belonging to converter topology that probably grabbed capability for manufacturing multilevel voltages through the source of numerous DC voltage. Working within this kind of topology, a chain that of considering one level inverter that meant to be related plus associated whole as one. The route of CHB kind of multilevel inverters mostly patterned along with eight switches comprising most of the five stages that of considering inverter. Every kind of resource belonging to DC was being related along the conforming H-bridge creating five exclusive voltage productions.

D. Active NPC Multilevel Inverter

Fresh name taken for the multilevel inverter within terminology as active clamped (ANPC) multilevel inverter has been showcased Bruckner et al. [9]. It was being introduced along with main throwback intuition and willing kind of overwhelming insufficient plus jagged harms which has been truly shared among outer also the inner switched by the location and placing up to some kind of power switches leaving those that are simple diodes.

The 9-level of ANPC multilevel converter belong and actually the true mixture of NPC along with FC inverter topologies. The count of those considering of two-level inverter within this kind of setting could be gained through the formula using (n-1) / 2, in which n considering inverter productivity stages.

E. Hybridised Cascaded H-Bridge Multilevel Inverter

A latest brand arrangement belonging to multilevel inverter was obtainable through Odeh along with Nnadi [10] considered so far as follows hybridised cascaded H-bridge (HCHB) multilevel inverter. Figure 7 truly depicts a 9-stage HCHB multilevel inverter along two DC response voltages. Within this thoughtful belonging to inverter topology, nine stages that of considering voltages against single cycle were being only if through intersecting comprising both 5-level hybrid inverters. This type of topology is same as that of kind of CHB topology.

Within comparing with the old fashioned CHB inverter, the present count of those particular elements utilized within that sort of topology which are being mostly minimized taking along same kind of result voltage phase.

The main limitation of this topology is that it cannot be used in the applications where high voltages are required.

F. Modular Multilevel Converter

There is another new classification of the multilevel inverter, named as modular multilevel converter (MMC) was presented by Lesnicar and Marquardt in [11].

A solitary cell belonging to MMC establishes belonging to two switches along one complementary capacitor. H-bridge inverter that was being called as $n = 2c + 1$, in which n considered to be inverter result stages along with c characterizes.

G. Switched Series /Parallel Sources-based Multilevel Inverter

Hinago and Koizumi [12] proposed multilevel inverter which consists of DC sources that could be switches in parallel and in series along with the H-bridge. This topology is referred as switched series/parallel foundations (SSPS)-based multilevel inverter. Mainly considered as evolving out the comparable stages belonging to productivity in the form of CHB, the analogous count of those foundations is being made compulsory through the help of SSPS inverter however would be much little in amount containing switches. The type of topology described above belonging to 9-level SSPS multilevel inverter along four input DC resources were being totally relied upon only the two of required segments First segments comprise of switched sources along with outputs bus voltage $v_{bus(t)}$ along with the additional segment manufactures negative along with positive cycles belonging to voltage $v_{bus(t)}$ for nourishing AC load. The four sources which are V_{dc1} to V_{dc4} and power switches S_1 to S_9 consist in the first part while power switches Q_1 to Q_4 consist in the second part.

H. H-Bridge and Two-level Modules-based Multilevel Inverter

Suroso along with Noguchi [13] termed a single introduced topology belonging to multilevel inverter called with the name defined as H-bridge along with the other two-level power modules (HBTPM) multilevel inverter. However, 9- level topology inverter along those of inputs of only four DC resources V_{dc1} till V_{dc4}. The so called terminals taken along little capacities belonging to resources were being interrelated along aid considering power switches. These were both segments considering topology; first comprising polarity generation (Q_1 till Q_4) along with second considered is level generation (S_1 till S_6).

However, the pattern used is actually very easy and normal because that could be observed in case of little constrained potentials belonging to different stages combination on every bus end.

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III. LITERATURE REVIEW

In this paper [14], author have reviewed various inverters for the conversion of the Dc to AC as capacitor clamped multilevel inverter, a cascaded H-bridge multilevel inverter and a hybrid multilevel inverter. In the work the author stated that the multilevel inverter can be efficiently used for the applications working with single phase or even on the 3 phase related applications. The study stated that the lowed value of the THD can be considered using the lowest components of the cascaded H-bridge inverter and also have the advantage in implementing the same and also for the configuration making.

In this paper [15], presented a single phase cascaded H-bridge converter for the power grids working with PV systems. On the basis of the maximum power point the power entering into the grid can be tracked properly and also the system considers the reduction in the systems working frequency and the reliability of the system is enhanced.

In this paper [16], author presented a neutral point clamped three-level inverter topology. The discussed type of inverter are sufficient to match the sinusoidal with the generated voltage at the voltage, the system also works towards the reduction of the THD in the waveform of the output voltage generated. Switch pulses are generated using the space vector modulation technique in the designed inverter. The major capability of the multilevel inverter is that it can generate the sufficient voltage at output end with low THD which actually reduces the requirement of the filters in the complete process.

In this paper [17], author presented a novel configuration technique for the conversion of the energy to the electrical energy. In the proposed technique two different inverters connected in the system transformer and the secondary winding is connected with the grid using the filters.

The failure rate for the devices connected in the system is reduced by reduction in the voltage of the DC bus which also offers the flexibility, in the system the low rated switches are also selected for lowering the voltage stress.

In this paper [18], author presented a novel H-bridge hybrid multilevel inverter where fewer switches are connected with H-bridges inverters by solar array voltage source connected in parallel. In the proposed methodology the number of output voltage is increased and also reduces the total harmonic distortion for the output voltage waveform.

In this paper [19], author presented a 5-level hybrid cascaded multilevel inverter having PWM technique, where the number of switches are reduced and also reduces the losses at switches. IN the proposed topology six different switches are used with two capacitors and also equipped with two asymmetric voltage sources. In the work multi carrier PWN technique is being used which works to generate the voltage at 5 different levels. This proposed circuit has THD-13.96% for a five level output voltage waveform.

IV. PROBLEM STATEMENT

In this work the work done by Y.C. Fong et al. (2018)[20], is extended, "***A Novel Switched-capacitor Multilevel Inverter Offering Modularity in Design***", author in the work proposed a novel design for the multilevel inverter topology which presents modularity in the design of the complete system.

In the system is equipped with SC technique in parallel and is having the capability of self-balancing the voltage and for the step up capability. As the voltage stress defined for the capacitors and switches is limited for which the SCMLI can be better selection for the modularization of the low voltage solar cells, so as to design a scalable multilevel inverter with reduced cost. In the proposed methodology the major focus towards the cost optimization and switching for which the half bridging devices are used and also switching angle is decided on dynamically and also works for the elimination of the harmonics which are low to improve the voltage supply.

V. RESEARCH METHODOLOGY

The stated methodology comprises considering SC units, Triple half bridge front end, half bridge back end attaching towards end SC unit load. Given is formal stating of entire of parts utilized in launched technique.

The proposed SCMLI consists of:

A. A triple-half-bridge front-end connecting to the DC voltage source,
B. SC units,
C. A half-bridge back-end connecting to the last SC unit and the load.

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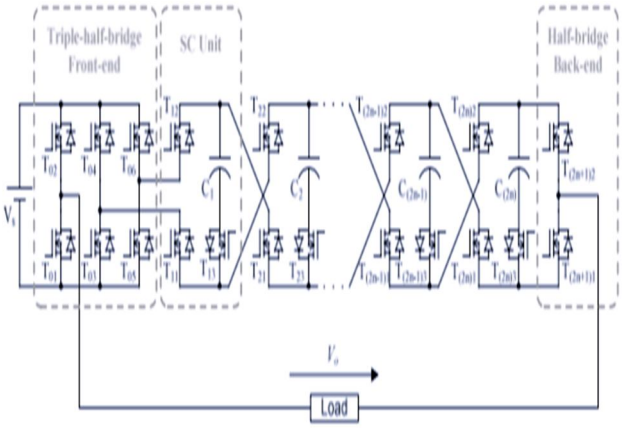

Fig. 3 Block diagram showing the proposed methodology.

In the proposed work works for two problems as under:

1) *Level Balancing:* In the previous work the process is independent for number of levels and voltage at input and output part is limited to specific part for which in the proposed work the multilevel topology is having an extra half-bridge is integrated which actually is being used to adjust the voltage of the other switches using the self-balancing technique. The connected DC buses of the half-bridge didn't consider any amount energy while running. As it works like the amount of power generated in first half cycle is consumed in next half cycle and similarly the half-bridge DC bus are charged equally in next coming cycle. Hence at the end of the process the DC bus voltage is remains unchanged after completion of process. The above defined process unchanged for any type of the system working as MLI and also because of independency in the power ratio of the MLI. In the MLI there are all four modes of operation and the every phase of the inverter can be any of the defined four modes. In the case when the even level of voltage is generated with positive or negative polarity the LDN is over crossed. In the case of the generation of the odd voltage level, the LDN remains the part of the complete process. Over the positive part of the half cycle the voltage level can be added with the other voltage levels generated by the inverter and can be better picked to understand the equivalent circuit to the above described. In cases when the negative odd level of voltage is required to be generated, the positive LDN voltage will be added to the negative voltage of rest of the inverter considering the addition algebraically. The level doubling actually will help it considering the lowest THD at the final voltage outcome.
2) *Switching Angle:* Switching angle actually defines the THD for the output voltage and the switching angle should be defined in a way that the THD is as low as possible. The final waveform generated by the EPM method is just very similar to the triangle shaped waveform, hence to generate better results different methods like [5] Half Phase Method (HEPM) are in consideration, using the defined technique the THD can be reduced to an minimum level and can have the formatted waveform at the output end.

VI. RESULT AND DISCUSSION

In this work 11 level MLI is implemented in Matlab 15, reason to make it for 11 Level is to reduce the distortion of the process which actually is the different in the ideal wave to the output voltage wave generated. For switching, IGBT (Insulated Gate Bipolar Transistor) is being used and also are represented in the implementation snaps shown in the below section. The novelty in the mechanism is all about the usage of the PWM technique for generating smooth outcomes. The discussed technique is simulated in MATLAB 15 using Simulink for efficient connection making.

For the validation of the different processing's in the defined methodology an ideal 11 level MLI working on 36V voltage source and four different 1000 µF SC units working over 400Hz and also having minimum THD [21] is implemented. In the validation the voltage of capacitor, voltage stress of different connected switches having load of 25Ω-10mH is used. Various selected gate drivers signals are used to simulate the output waveform, using the current, voltage and also the voltage of the switches. The results depicts the high voltage and current approx. 144V and 4A while keeping the voltage stress to of the switches T_{11} to T_{23} was about 72V. Since the load was inductive ($\varphi \approx 45°$) in the simulation model, the voltage ripples increased with SC number i. The simulated voltage ripples of the capacitors were varied from around 1.06V to 2.2V.

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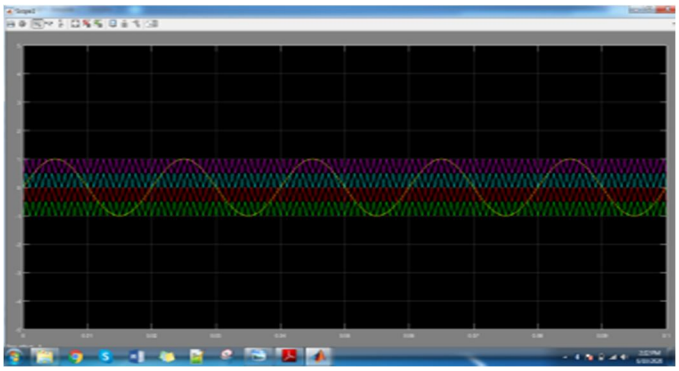

Fig. 4 Snapshot 1.

The above snap shows the input voltage pulse for 5 level MLI, where the different colored waves show the input voltage for different level in the MLI. The wave shown in the middle of the snap is an ideal sinusoidal wave form which is used for further comparison purpose considering the output voltage for same level MLI.

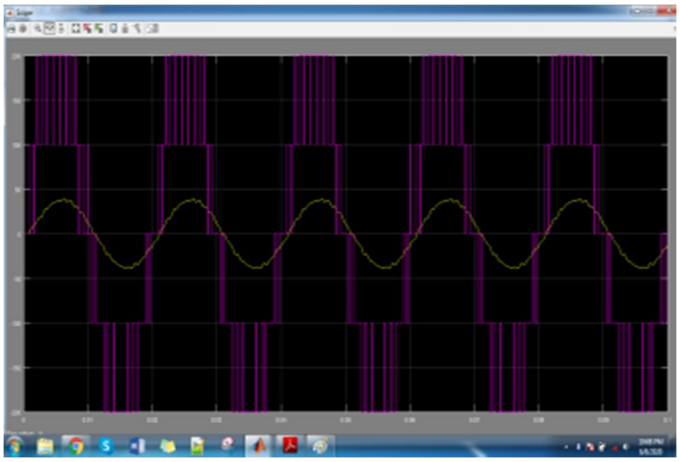

Fig. 5 Snapshot 2.

The snap above shows the output voltage waveform which actually shows some distortion as compared to the previous input voltage wave form. The colored blocks represent the discrete levels or values of the output voltage generated by the 5 level MLI. As the distortion between the input and output voltage can be clearly considered from the above two shown images. The output voltage in the case of 5 Level MLI is having distortion of 27.15%.

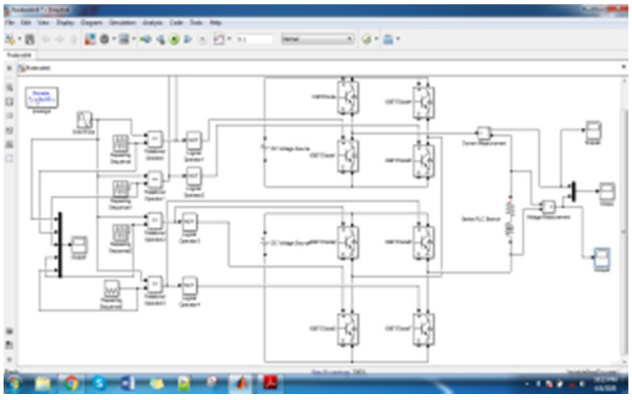

Fig. 6 Snapshot 3.

The figure above shows the circuit diagram for 5 Level MLI with several connected components like power GUI which is used for the computation of the output here is THD, the diagram also shows connected logical operators and relational operators just to transfer the input towards the IGBT gate terminals for switching. Ammeter is also used for measuring the flowing current in the circuit. Voltmeter is also being used to measure the voltage in the circuit.

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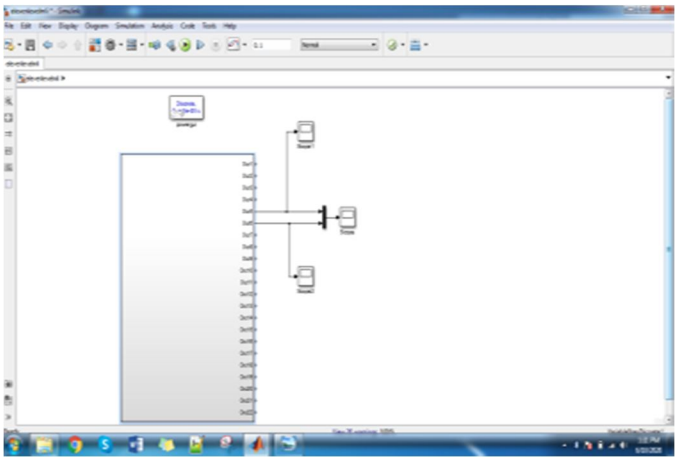

Fig. 7 Snapshot 4.

Figure above shows the working model of the 11 level MLI with several connected components like power GUI used for the computation of THD, scope for generating calculated outcomes. The major part of the model is the subsystem which is shown under with all of the components making the model work towards the outcome.

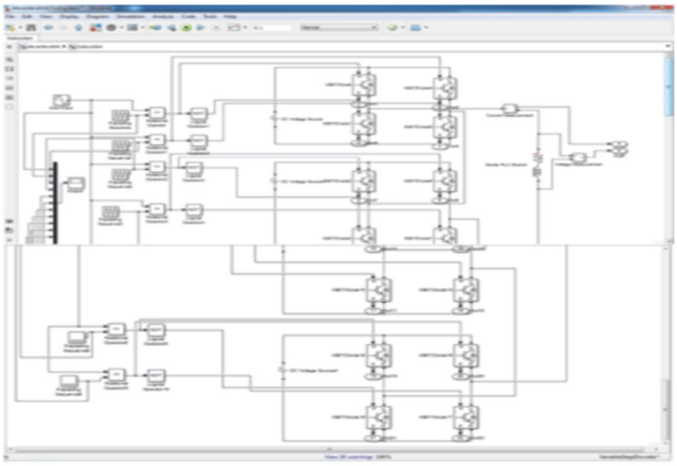

Fig. 7 Snapshot 5.

The figure above is the representation of the subsystem of the 11 level MLI.

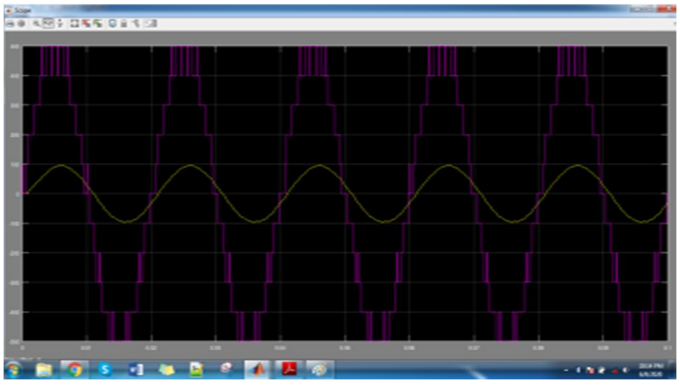

Fig. 8 Snapshot 6.

Figure depicts the different outputs of the all 11 levels of the MLI and wave in the yellow color is the sinusoidal wave form having distortion with respect to the input wave form submitted and the distortion computation is shown in the below image.

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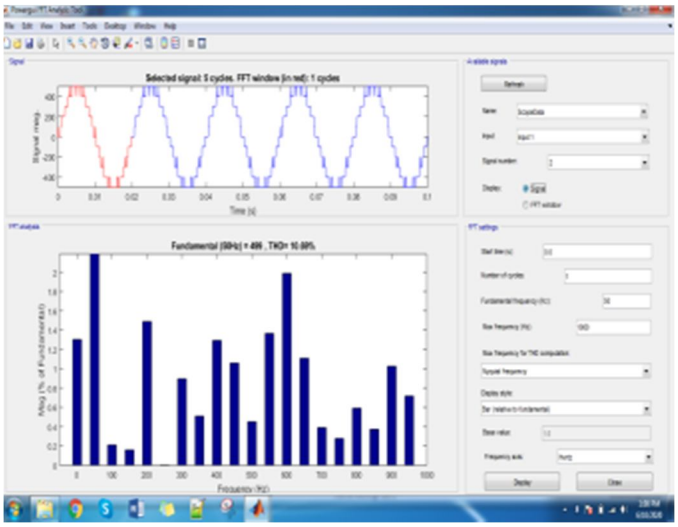

Figure 4.7: Snapshot 7.

FFT for the computation of the THD, as can be seen the output voltage in the case of 11 Level MLI is having distortion of 10.69% and is less as compared other MLI and inverter models.

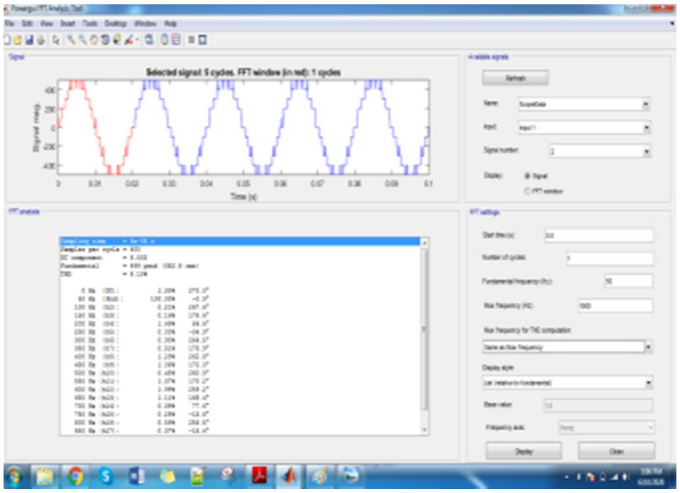

Figure 4.8: Snapshot 8.

The above figure the comparison of the THD using the maximum frequency range where the THD is showing some changes in the THD or can be considered as the improved results as in the previous case the fundamental range for frequency is being used. So as to validate the results for the proposed methodology the MLI is simulated using the MATLAB/Simulink. On the basis of the results it can be stated well that the proposed MLI is favorable for application where high level input voltage is being required like of 400-Hz and also for some more systems working on few kilohertz.

VII. CONCLUSION

With the advancement and development of various industries and sectors at international as well as domestic levels, demands for high energy converters are continuously increasing. It can be said that the multilevel inverters are continued to gain popularity and importance for the applications of low as well as high power.

The proposed methodology is implanted with 1000 µF SC modules over 11 level MLI. The voltage of the capacitor and waveform at the output are evaluated over the differentiating frequencies and loading conditions. On the basis of the simulation results it can be well stated that the system higher voltage output capabilities with reduction in the voltage ripples at the capacitors. The ideal voltage waveform which is generated on ideal working conditions is compared with output generated and shows that the charging rates of the capacitor is limited by the ESR of the capacitors and the parasitic resistance and inductance of the circuit layout. This would limit the maximum operating frequency of the SCMLI. The presented technique for multilevel inverter can be further considered for real time results and also can be further considered further level to enhance the competency of the output voltage.

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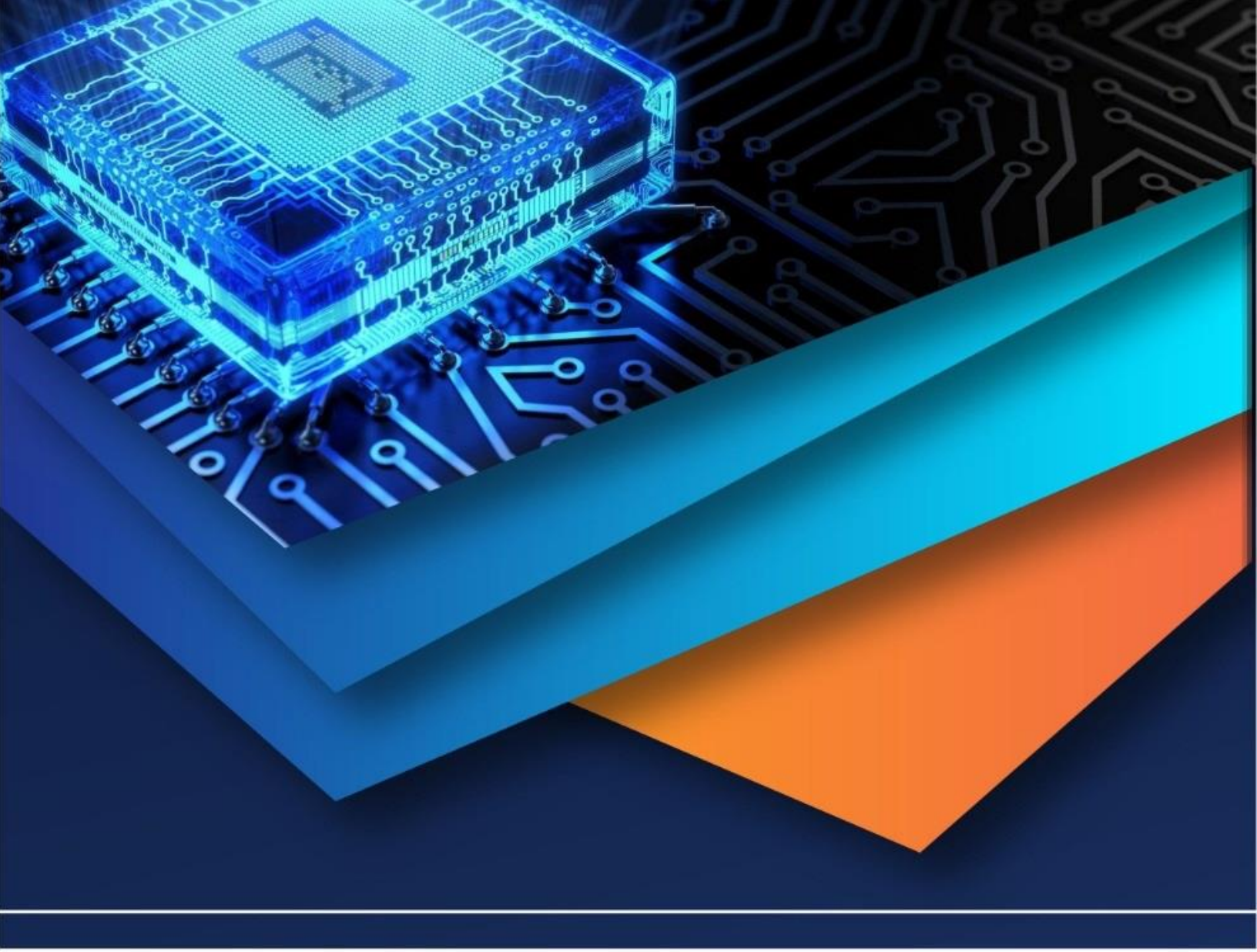

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