iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 8 **Issue:** VII **Month of publication:** July 2020

DOI: https://doi.org/10.22214/ijraset.2020.30252

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VII July 2020- Available at www.ijraset.com

Ternary CAM Memory Design using MOS Transistors

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Abstract: ***Ternary content addressable memory (TCAM) is a high performance search engine which accesses the data based on its contents in a single clock cycle. To reduce the power consumption of the TCAM cell when we search the data. Most memory devices store and retrieve data by addressing specific memory location. As a result this path often becomes the limiting factor for the systems that rely on fast memory access. In this paper to design six transistors based SRAM design with eight transistors of two side self gating TCAM and to design four transistors using transmission gate logic function of XOR based TCAM. This design is to increase the matched line search process and to reduce the overall dynamic power consumption level of TCAM array design. Our proposed work is to design CMOS based RAM and Ternary CAM memory architecture. This design is used to find matched line data effectively and to reduce the leakage power level for match line searching process. To design transmission gate logic for matched line searching process. This process is to apply the TCAM cell architecture and to reduce the dynamic power consumption. Our work is to analysis the data store and search, data matching operation and to maintain the input voltage level then to optimize the Vdd to ground power leakage level. This system is used to identify the input data and search data then to manage the data matching level to improve the matched line data searching process. Proposed system is to consume less power and also reduce the leakage power level and less area consumption. This system is to require less external voltage sources. This system is no need to register element separately.***

Keywords: Content Addressable Memory(CAM), Ternary CAM, XOR type CAM cell, Static Random Access Memory (SRAM), Low Power.

I. INTRODUCTION

Content addressable memory (CAM) is an application specific memory that allows entire contents to be searched within a single clock cycle. CAM is a special type of computer memory used in very high speed searching applications [1]. An efficient hardware solution to perform table lookup is the ternary content addressable memory (TCAM). A TCAM can be used as a co-processor for the network processing unit to load the table lookup task. Ternary content addressable memory is a hardware based parallel lookup table with bit level masking capability. A special logic unit named multiple match resolver is required to resolve the best candidate if more than one words indicate a “match”. They are attractive for applications such as packet forwarding and classification in network routers [4]. The main contribution of this work is divided in two parts: (i) Reduction in match line sensing energy and (ii) static power reduction techniques. The match line sensing energy is reduced by employing (i) positive feedback match line sense amplifier (MLSA), (ii) low capacitance comparison logic and (iii) low power match line segmentation techniques [3].

TCAM memory which is combined with RAM memory design called hybrid memory to enhance the performance level while searching data from memory. In this paper we implement the new form of hybrid memory design of RAM with TCAM in renaming and recovering the data [2]. Ternary content addressable memory is a hardware search engine that is much faster than modified algorithmic approaches for search intensive applications. By this we can search required address for single clock period. With the help of TCAM architecture we can optimize the page allocation in RAM [5].

Binary CAM (BCAM) is the simplest type of TCAM which uses data search words consisting entirely of 1s and 0s [1]. Ternary TCAM (TCAM) allows a third matching state of "X" or "don't care" for one or more bits in the stored data word thus adding flexibility to the search [2]. For example a ternary CAM might have a stored word of "10XX0" which will match any of the four search words "10000", "10010", "10100" or "10110". Additional state is implemented by adding a mask bit such as care or don’t cares bit to every memory cell. Binary CAM perform exact match searches. Ternary CAM allows don’t cares act as wildcards during a search and are particularly attractive for implementing longest prefix match searches in routing tables[3].

Standard computer memory such as random access memory in which the user supplies a memory address and the RAM returns the data word stored at that address. TCAM is designed such that the user supplies a data word and the TCAM searches its entire memory to see if that data word is stored anywhere in it [2].

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ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue VII July 2020- Available at www.ijraset.com

Sense amplifier is part of the read circuitry that is used when data is read from the memory its role is to sense the low power signals from a bit line (BL) that represents a data bit 1 or 0 stored in a memory cell and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory [2]. Modern sense amplifier circuit consists of two to six usually four transistors [7]. Sense amplifiers for core memory sometimes contained thirteen transistors. There is one sense amplifier for each column of memory cells are usually hundreds or thousands of identical sense amplifiers are used.

In this paper TCAM refers to binary CAM (BCAM) with don't care [2]. The CAM array is divided into several equally sized sub blocks which can be activated independently. For a previously trained network and given an input tag the classifier only uses a small portion of the tag and predicts very few sub blocks of the TCAM to be activated. Once the sub blocks are activated the tag is compared against the few entries in them while keeping the rest deactivated and thus lowers the dynamic energy dissipation and reduces power consumption.

II. PROPOSED SYSTEM ARCHITECTURE

In proposed system the content addressable memory is a XOR logic gate based cell design [2]. Data matching process is used in the match line sense amplifier (MLSA). The proposed system can do a fast match line (ML) selection process. In this paper first of all the system design of 6T based static random access memory (SRAM) CMOS design [Fig.4]. This design is to store the single bit value. This design consists of two inverter cross connection is used to maintain the given input data. Then the system design of 8T based XOR Ternary CAM design [Fig.2]. It consists of selection line (SL) and the bit line (BL) to control the TCAM cell. This process used to find the address bit location. Then the scan based enable process is to find the TCAM cell array result. The XOR gate function to match the SRAM data and TCAM data and to invert the activation result. The match line process is to check the CAM data register. The clock function is to control the output matched line row then it will get the content address effectively. If the write line is set to '1', then to get the data in cross inverter circuit connection. This process is used to find the address bit location and to check the address level and apply the evaluation logic function.

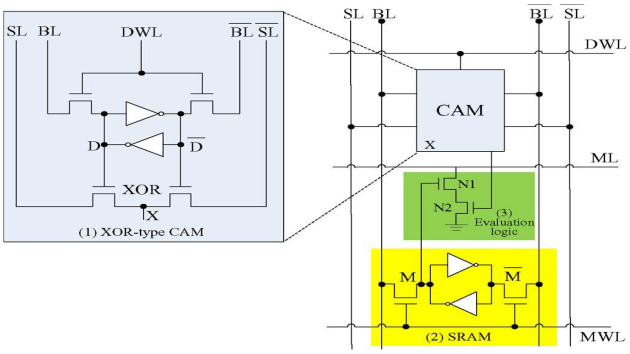


Fig. 2 XOR type Single CAM cell

The scan based enable process is to find the TCAM cell array result and to apply the CAM and RAM data. The XOR gate function to match the SRAM data and TCAM data and to invert the activation result [2]. To check the all the row CAM data to data register input data bit then to activate the match line function.

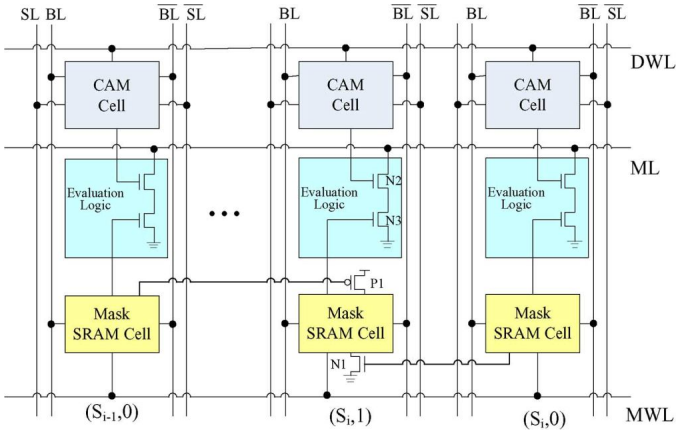


Fig. 3 Two-Side Self-Gating Ternary CAM array

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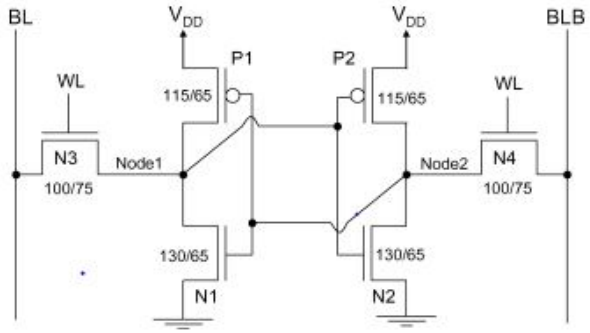


Fig. 4 Proposed circuit of 6T based SRAM

The match line process is to check the CAM data register and RAM data register value. The clock function is to control the output matched line row and to get the content address [4]. This matched line process is mainly focused by the TCAM cell array input data storage [5]. The final output is to identify the content address effectively and to increase the ML check process time. Then to consider the power consumption level and to check the match line delay time also. Area consumption is depends on optimization of MOS transistors count level. Sparse clustered networks uses content addressable memories [7].

III. SINGLE TERNARY CAM CELL

TCAM cell includes mainly three components. First one is the CAM cell next is the mask cell and last the evaluation logic. Fig. 5 shows a typical schematic of a single ternary CAM cell. One of the main features of TCAM is that it can store three states “0”, “1” and “X”. But in binary CAM it can store only two states “0” and “1”. The mask bit (M) and stored data (D) inside the CAM cell determines the state of the CAM cell. If M = 0 there is always a match without considering the search data and if M = 1 then it will be a normal match based on the search data and stored data.

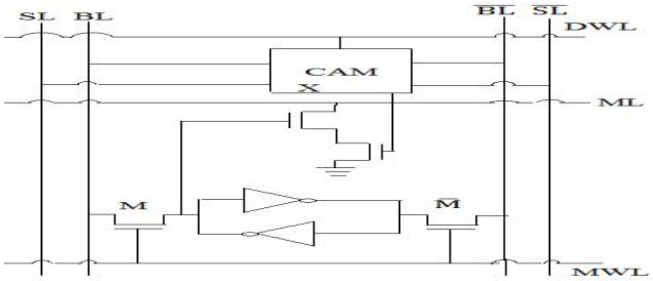


Fig.5 Schematic of a 4T-Ternary CAM cell

IV. RESULT ANALYSIS

Proposed system is implemented using TANNER version 13.0 back-end EDA tool is used for simulation. S-Edit (Schematic Entry), W-Edit (Waveform view and analysis) and T-Spice (Tanner Spice) is used for circuit simulation.

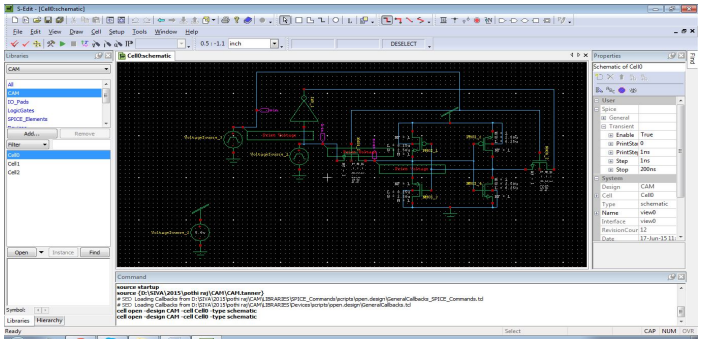


Fig. 6 Schematic entry of 6T based SRAM design

Fig.6 represented as schematic entry of six transistors based Static RAM design using S-Edit of TANNER version 13.0 simulators.

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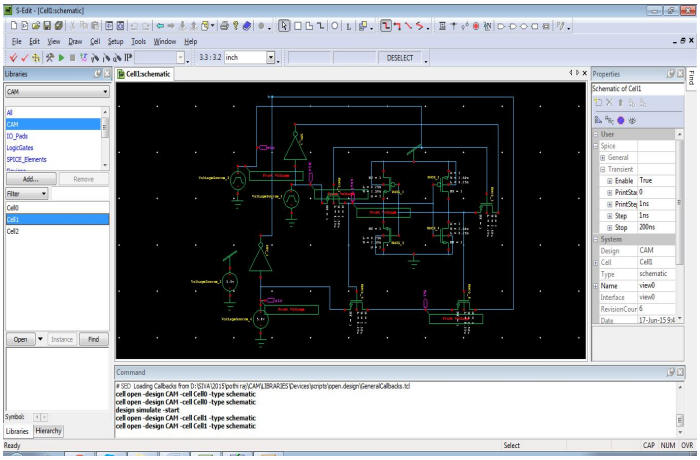


Fig. 7 Schematic entry of 8T based Ternary CAM design

Fig.7 denoted as schematic entry of eight transistors based single TCAM cell design using S-Edit of TANNER version 13.0 simulators.

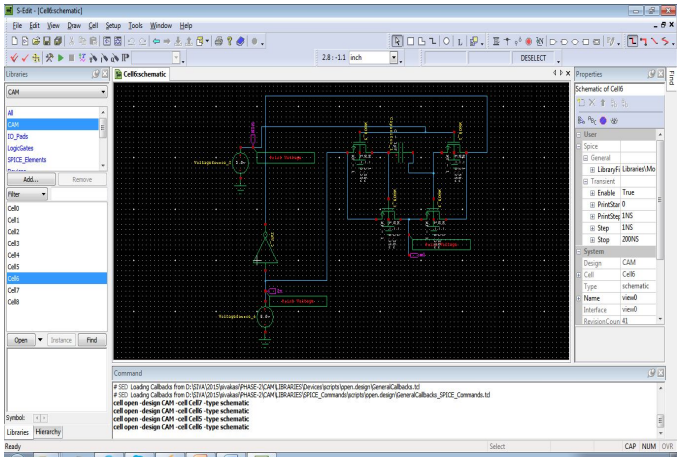


Fig. 8 Schematic entry of 4T based Ternary CAM design

Fig.8 represented as schematic entry of four transistors based single TCAM cell design using S-Edit of TANNER version 13.0 simulators.

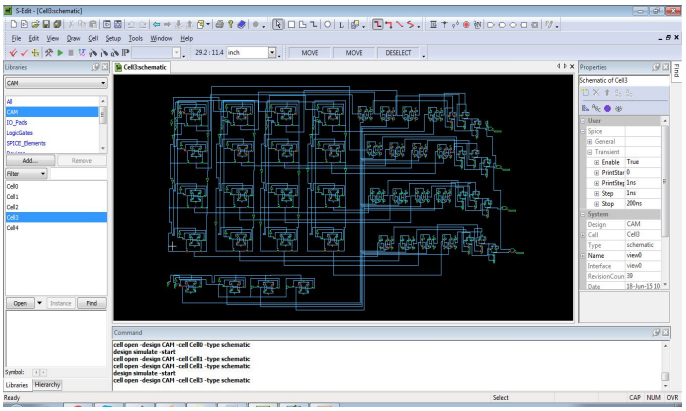


Fig. 9 Schematic entries of 4x4 TCAM cells with MLSA

Fig.9 concluded as a schematic design of 4x4 TCAM cell with match line sense amplifier and scan based enable function using S-Edit of TANNER version 13.0 simulators.

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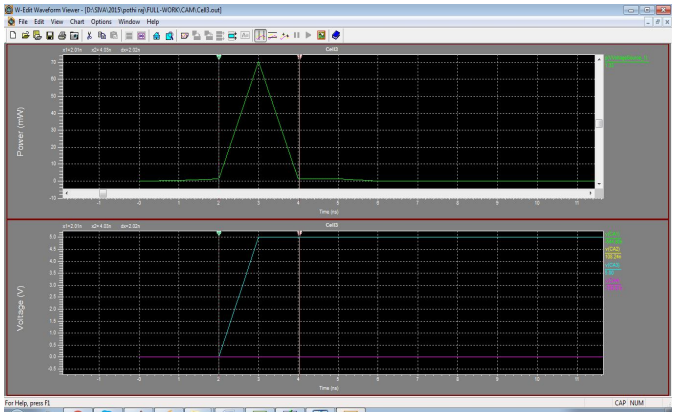


Fig.10 Power consumption of 4x4TCAM cell (8T based)

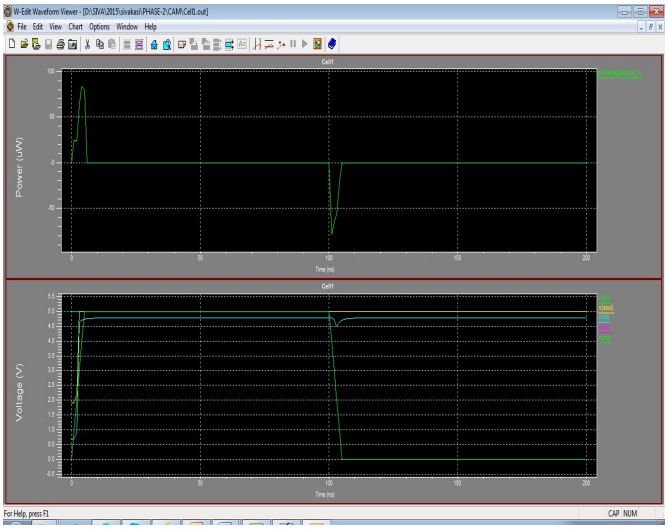


Fig.11 Power consumption of 4x4TCAM cell (4T based)

Fig.10 and Fig.11 concluded as a power consumption of 4x4 TCAM cell of 8T and 4T based TCAM respectively using T-SPICE and W-Edit of TANNER version 13.0 simulator.

V. PERFORMANCE COMPARISION

Simulation parameters	Single TCAM Cell	Single TCAM cell	4x4 TCAM array	4x4 TCAM array
Supply Voltage	5V	5V	5V	5V
Power consumption	70µW	540pW	70mW	17mW
Area consumption	200 µm^2	100 µm^2	100 mm^2	78.5 mm^2
Optimization of transistor count level	8	4	400	314

From the comparison table itself we can see the significant reduction in number of transistors, power consumption and area consumption.

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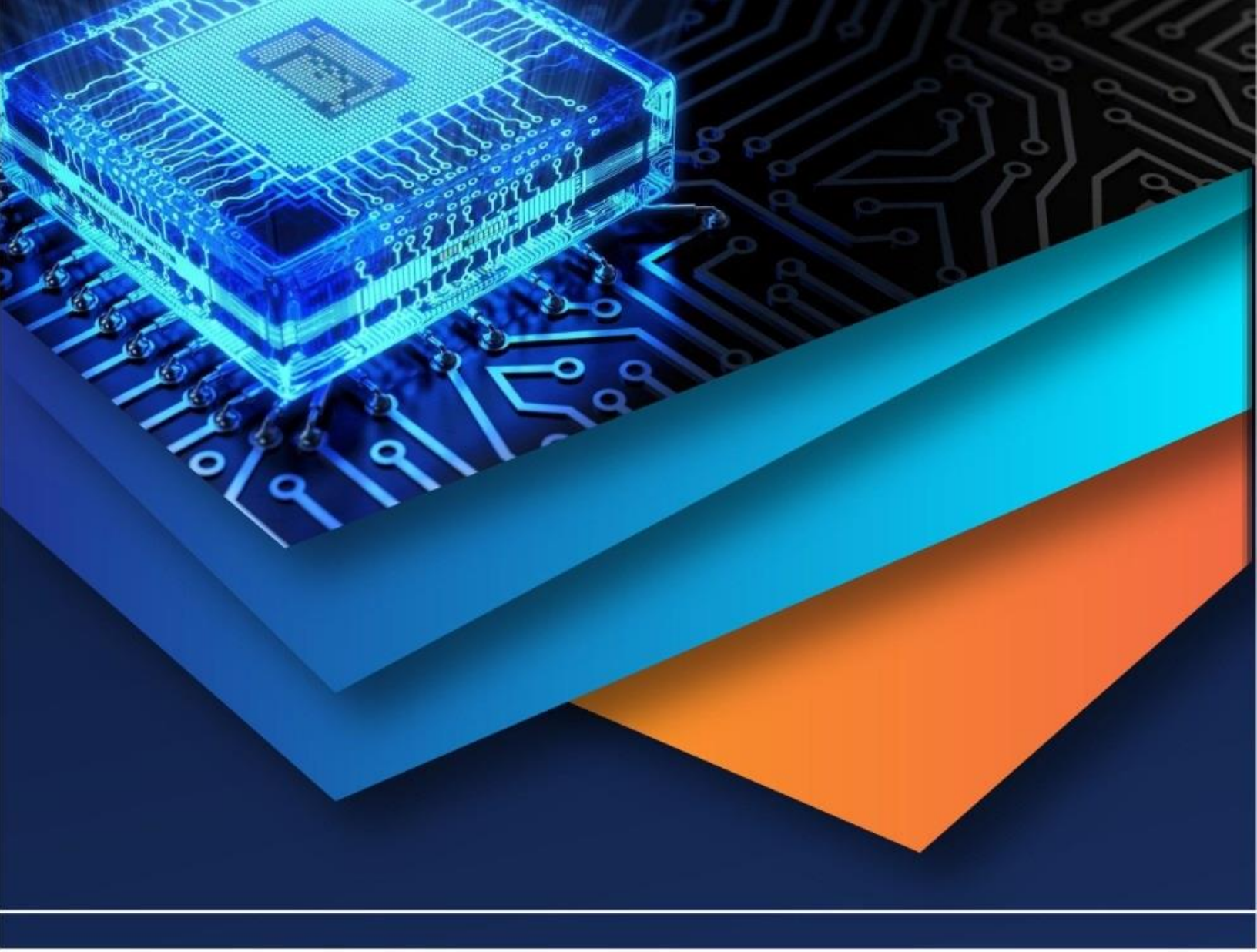
VI. CONCLUSION

In this paper design of XOR based content addressable memory (CAM) has been presented. It is a very low power Ternary content addressable memory (TCAM) cell. Ternary content addressable memory (TCAM) is suitable for low power applications where frequent and parallel look-up operations are required [2]. In a conventional TCAM array each entry consists of a tag that if matched with the input points to the location of a data word in a static random access memory (SRAM) block. The actual data of interest are stored in the SRAM and a tag is simply a reference to it. Therefore when it is required to search for the data in the SRAM it suffices to search for its corresponding tag. Consequently the tag may be shorter than the SRAM data and would require fewer bit comparisons. Simple and fast updates can be achieved without retraining the network entirely. Depending on the application non uniform inputs may result in higher power consumption but does not affect the accuracy of the final result. NOR type architecture was also implemented in the same process technology.

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