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Averaged Modeling of Zeta Converters Operating in Continuous Conduction Mode for LED Lighting System

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Abstract: This Paper is mainly based on State space Analysis based modelling of Zeta Converter for Dynamic stability analysis and to prove the need of Controller Design. Zeta Converter model is derived using the transfer function using the input and output of the converter. Zeta Converter is a dc dc converter that consists of four passive components and it can be used to improve the quality of supply at AC mains by improving the power factor. It can work in both Buck and Boost modes of operation. Cuk and Sepic Converters are also available in the same group but Zeta has its own advantages as there is Input to Output DC Insulation and Continuous output Current. There is an issue of Complex equations in the analysis of Zeta converter therefore a new method based on mathematical modelling is applied to solve these complex equations. As per the Controller need and Dynamic stability analysis .A model based PI controller is designed for the Zeta converter and the analysis results are presented below to verify the accuracy of the achieved model and model based controller. It is found to be a very important tool in power factor Correction.

Keywords: Continuous Conduction Mode (CCM), Zeta DC-DC Converter, Diode Bridge Rectifier (DBR), LED Lamp Driver,

I. INTRODUCTION

Zeta converter based power supply is proposed for LED light with universal input voltage. In proposed LED driver, power factor corrected (PFC) AC-DC AC mains current and helps in improving the input power factor to the desired level as per the limits given by various international standards like IEC-61000-3-2 class D requirement. The circuit maintains constant output lamp voltage to achieve stable operation of LED driver for retrofit applications. Since PFC converter is operated at high switching frequency of 50 kHz, it reduces the weight and size of passive components like inductor and capacitor. A most popular technique known as PWM dimming is to be used to drive multiple LED lamps for universal voltage applications**.** The schematic circuit diagram of proposed LED driver is shown below in Figure. Here an uncontrolled diode rectifier (DBR) is arranged after input supply to generate pulsating DC signal that goes into PFC Zeta converter as input signal. This converter generates a DC output voltage which is compared with the reference voltage and generates the error signal that works as input signal for PI controller again. To generate the PWM pulses, the output of PI controller is compared with saw tooth wave of suitable frequency at 50 kHz. The PWM pulse with repeating frequency f_s and conduction duty D drives to switch M which is a p-channel power MOSFET device. The switching period is $T=1/f_s$ so the switch-on period is DT and switch-off period is (1-D) T. when the switch M turned off, the current flows through the free-wheeling diode D and descends for whole switching –off period (1-D) T. In continuous mode, current I_o does not become zero before switch M turned on but current becomes zero before switch M turned on again in discontinuous mode.

A. Mathematical Analysis of Zeta Converter

The small signal averaged state-space method is a either simple circuits or complex structures [18, 19]. By using mathematical analysis and effort, this method is helpful to achieve linear averaged time-invariant models and its derived final result. Procedure proposed by researchers [18, 19] is adapted here to obtain such models and to solve to our problem. The schematic diagram of Zeta converter is shown in Figure 1

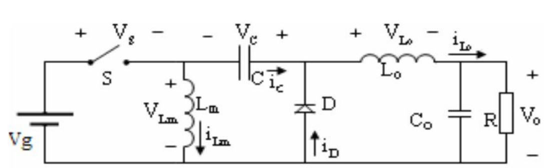

Figure: 1

The model has the mathematical description of the real system behavior which is required to check the stability of that system. Here starting point is the extraction of state equation by using Kirchhoff's voltage and current laws for two operating modes of switch. First mode is when the switch is in on state and the diode is off, and the second mode is that the switch is off and the diode is on. All extracted state equation are obtained in first order and reduce the complexity of the equations and ease the analysis because these equations are calculated in nodes and loops in the presence of one passive element. Waveform of zeta converter is shown in figure: 2

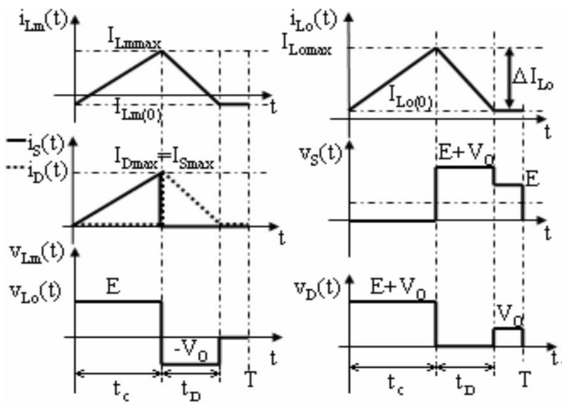

Figure: 2 Zeta converter waveforms.

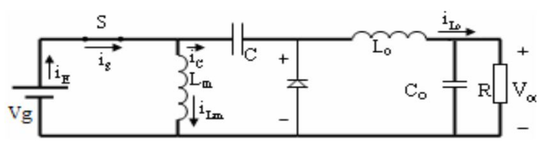

Figure: 1 (a) ON STATE

When the switch is closed for DT interval, then the differential equations for the circuit shown in Figure 1 (a) are as follows:

$$L_m \frac{di_{Lm}}{dt} = v_g \quad (1)$$

$$L_0 \frac{di_{L0}}{dt} = v_g + v_c - v_o \quad (2)$$

$$C \frac{dv_C}{dt} = -i_{Lo} \quad (3)$$

$$v_o = v_{C0} \quad (4)$$

$$C_0 \frac{dv_C}{dt} = i_{L0} - \frac{v_o}{R} \quad (5)$$

Substituting equation (4) in equation (5), the following equation is achieved:

$$C_0 \frac{dv_o}{dt} = i_{L0} - \frac{v_o}{R} \quad (6)$$

Suppose;

$$x_1 = i_{Lm}$$

$$x_2 = i_{L0}$$

$$x_3 = v_C$$

$$x_4 = v_{C0}$$

The above equations can be written in state space matrix form as below,

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1/L_0 & -1/L_0 \\ 0 & -1/C & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/RC_0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 1/L_m \\ 1/L_0 \\ 0 \\ 0 \end{bmatrix} v_g \quad (7)$$

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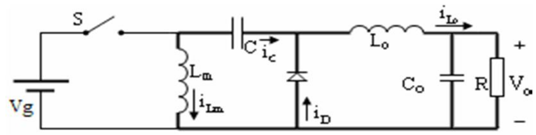

Figure: 1 (b) OFF STATE

The differential equations for the circuit shown in Figure 1 (b), when the switch is open for (1-D)T interval are as follows;

$$L_m \frac{di_{Lm}}{dt} = -v_C \quad (8)$$

$$L_0 \frac{di_{L0}}{dt} = -v_{C0} \quad (9)$$

$$C \frac{dv_C}{dt} = -i_{Lm} \quad (10)$$

$$v_o = v_{C0} \quad (11)$$

$$C_0 \frac{dv_{C0}}{dt} = i_{L0} - \frac{v_o}{R} \quad (12)$$

Substituting equation (11) in equation (12), the following equation is achieved:

$$C_0 \frac{dv_o}{dt} = i_{L0} - \frac{v_o}{R} \quad (13)$$

The above equation can be written in state space matrix form as,

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_m & 0 \\ 0 & 0 & 0 & -1/L_m \\ 1/C & 0 & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/RC_0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g \quad (14)$$

From Equation (7) and (14), the state equation matrices are given as

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1/L_0 & -1/L_0 \\ 0 & -1/C & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/RC_0 \end{bmatrix}, A_2 = \begin{bmatrix} 0 & 0 & -1/L_m & 0 \\ 0 & 0 & 0 & -1/L_0 \\ 1/C & 0 & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/RC_0 \end{bmatrix}, B_1 = \begin{bmatrix} 1/L_m \\ 1/L_0 \\ 0 \\ 0 \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (15)$$

The state-space average equilibrium matrixes are calculated as

$$A = DA_1 + (1-D)A_2 = \begin{bmatrix} 0 & 0 & (D-1)/L_m & 0 \\ 0 & 0 & D/L_m & -1/L_0 \\ (1-D)/C & -D/C & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/RC_0 \end{bmatrix} (16)$$

$$B = DB_1 + (1-D)B_2 = \begin{bmatrix} D/L_m \\ D/L_0 \\ 0 \\ 0 \end{bmatrix} (17)$$

To build a small signal ac model at an operating point, the duty ratio is considered as

$$d(t) = D + \hat{d}(t) = D + d_m sin\omega t \qquad (18)$$

Where D and d_m are the constant and $d_m << D$

The small signal ac model can be given by the following state equation

$$d\dot{x}(t)/dt = A\hat{x}(t) + B\hat{v}(t) + \{(A_1 - A_2)X + (B_1 - B_2)V\}\hat{d}(t) \qquad (19)$$

The small signal ac state space equation is given as

$$\begin{bmatrix} d\hat{i}_{Lm}(t)/dt \\ d\hat{i}_{L0}(t)/dt \\ d\hat{v}_C(t)/dt \\ d\hat{v}_{C0}(t)/dt \end{bmatrix} = \begin{bmatrix} 0 & 0 & (D-1)/L_m & 0 \\ 0 & 0 & D/L_m & -1/L_0 \\ (1-D)/C & -D/C & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/RC_0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lm} \\ \hat{i}_{L0} \\ \hat{v}_C \\ \hat{v}_{C0} \end{bmatrix} + \begin{bmatrix} D/L_m \\ D/L_0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_g(t) + \left\{ \begin{bmatrix} 0 & 0 & 1/L_m & 0 \\ 0 & 0 & 1/L_0 & 0 \\ -1/C & -1/C & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{Lm} \\ I_{L0} \\ V_C \\ V_{C0} \end{bmatrix} + \begin{bmatrix} 1/L \\ 1/L_0 \\ 0 \\ 0 \end{bmatrix} Vg \right\} \hat{d}(t) \quad (20)$$

After taking the Laplace transform and simplification of equation (20), the equation can be written as

$$s\hat{I}_{Lm}(s) = \frac{(D-1)\hat{V}_C(s)}{L_m} + \frac{D\hat{V}_g(s)}{L_m} + \frac{V_C\hat{d}(s)}{L_m} + \frac{V_g\hat{d}(s)}{L_m} \quad (21)$$

$$s\hat{I}_{L0}(s) = \frac{D\hat{V}_C(s)}{L_m} - \frac{\hat{V}_{C0}(s)}{L_0} + \frac{D\hat{V}_g(s)}{L_0} + \frac{V_C\hat{d}(s)}{L_0} + \frac{V_g\hat{d}(s)}{L_0} \quad (22)$$

$$s\hat{V}_C(s) = \frac{(1-D)\hat{I}_{Lm}(s)}{C} - \frac{D\hat{I}_{L0}(s)}{C} + \frac{(I_{Lm} + I_{L0})\hat{d}(s)}{C} \quad (23)$$

$$s\hat{V}_{C0}(s) = \frac{\hat{I}_{L0}(s)}{C_0} - \frac{\hat{V}_{C0}(s)}{RC_0} \quad (24)$$

After solving equation 1, 2, 3 and 4, Laplace of output voltage can be written as below;

$$\hat{V}_{C0}(s) = \frac{\left(RL_0D^2(1-D) + RL_mD(1-D)^2 + RL_m{}^2CDs^2\right)\hat{V}_g(s) + \left(\left(RDL_0(1-D) + RL_m(1-D)^2 + RCL_m{}^2s^2\right)(V_C+V_g) - RDL_mL_0\left(I_m + I_{L_0}\right)s\right)d(s)}{RL_m{}^2L_0CC_0s^4 + L_m{}^2L_0Cs^3 + RL_m\left(L_mC + L_0C_0(D^2-D+1)\right)s^2 + L_mL_0(D^2-D+1)s + RL_m(1-D)^2} \quad (25)$$

$$G_{vd}(s) = \left|\frac{\hat{V}_{dc}(s)}{\hat{d}(s)}\right|_{\hat{V}_g(s)=0}$$

$$= \frac{\left(RDL_0(1-D) + RL_m(1-D)^2 + RCL_m{}^2s^2\right)(V_C + V_g) - RDL_mL_0\left(I_{L_m} + I_{L_0}\right)s}{RL_m{}^2L_0CC_0s^4 + L_m{}^2L_0Cs^3 + RL_m\left(L_mC + L_0C_0(D^2-D+1)\right)s^2 + L_mL_0(D^2-D+1)s + RL_m(1-D)^2}$$

Where, $G_{vd}(s)$ is the control-to-output transfer function of the Zeta converter.

B. Proposed topology of PFC Zeta converter based LED Driver

The schematic circuit diagram of proposed LED driver is shown below in Figure 1. Here an uncontrolled diode rectifier (UBR) is arranged after input supply to generate pulsating DC signal that goes into PFC Zeta converter as input signal. This converter generates a DC output voltage which is compared with the reference voltage and generates the error signal that works as input signal for PI controller again. To generate the PWM pulses, the output of PI controller is compared with saw tooth wave of suitable frequency at 60 kHz. The PWM pulse with repeating frequency f_s and conduction duty D drives to switch M which is a p-channel power MOSFET device. In this paper, the switching period is $T=1/f_s$ so the switch-on period is DT and switch-off period is (1-D) T. when the switch M turned off, the current flows through the free-wheeling diode D and descends for whole switching –off period (1-D)T. In continuous mode, current I_o does not become zero before switch M turned on but current becomes zero before switch M turned on again in discontinuous mode.

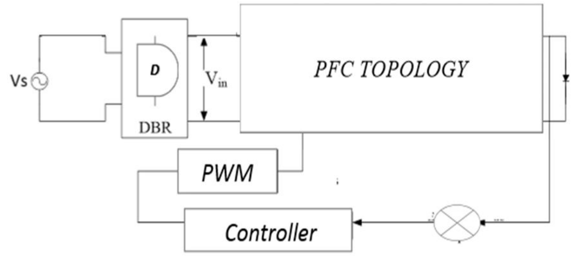

Figure: 3 PFC Zeta converter based LED Driver

C. Design and Analysis of Proposed PFC Zeta converter based LED Driver

To design and estimate the proposed topology of LED driver, few considerations have taken those are mention below;

1) All the components of proposed LED driver have considered as ideal components.
2) For maintaining the input voltage constant in one switching cycle, the switching frequency has selected much higher than AC mains frequency.
3) LED lamp has considered as a pure resistor during steady state operation and at the time of starting it considered as an open circuit.
4) DC link capacitor is considered as high enough so that In one switching cycle the DC link voltage can be maintained constant for a wide variation of input AC mains

The analysis and design of PFC Zeta converter is presented in continuous conduction mode (CCM) of operation and calculation of components is mention below.

For a Zeta converter operating in CCM, the duty cycle is defined as below

$$D \leq \frac{V_{dc}}{V_{in} + V_{dc}} \quad (a)$$

The critical value of inductance Lm and L0 is determined by allowing the change in peak-to-peak ripple current to be 100% of the average output current. The critical value of inductances Lm and L0 are defined as,

$$L_{m(crit)} = L_{0(crit)} = \frac{(1 - D_{min})V_{dc}}{2 f_s I_o} \quad (b)$$

The coupling capacitor (C) is designed on the basis of its ripple voltage contents. The voltage across coupling capacitor is equal to the peak value of the input voltage. It's important to design the capacitor C and its value can be expressed as below,

$$C = \frac{I_o D_{min}}{f_s \, \Delta V_c} \quad (c)$$

To maintain DC output constant voltage with less value of ripple contents, the output DC link capacitor C_0 must have enough high capacitance and must supply a continuous load current at high switching frequency. The value of capacitor C_0 is expressed as below

$$C_0 \geq \frac{I_o}{2\omega \, \Delta V_{C0}} \quad (d)$$

where, V_{in} is the maximum value of AC mains input voltage, V_{dc} is DC link output voltage, I_o is average output current, D is duty cycle, f_s is switching frequency of the active switch, ΔV_c is the ripple voltage of coupling capacitor C and ΔV_{c0} is the ripple voltage of DC link output capacitor C_0. At switching frequency f_s of 60 kHz, input of 220volt (rms) and DC link output of 60volt, the calculated value of parameters and components from equations a,b,c,d is mention below,

Maximum value of coupling capacitor voltage (V_c) = V_{in} (rms) $\sqrt{2}$
ΔV_c = 10% of V_c = 31.11volt
ΔV_{c0} = 8% of V_{dc} = 4.8volt
Minimum value of duty cycle for AC mains voltage of 270volt = 0.17
Maximum value of duty cycle for AC mains voltage of 90volt = 0.40
Selected duty cycle = .233
Average load current I_o = 0.4 Amp
Critical value of inductor L_m = 0.958 mH (selected as 40mH)
Critical value of inductor L_0 = 0.958 mH (selected as 40mH)

Coupling capacitor C = 49.93 nF
Output capacitor C_0 = 132 µF (selected as 833 µF)
V_{OSC}=4.5Volt
$V_{ref} = 1.05V$ (From IC datasheet)
The transfer function of the pulse-width modulator is estimated as

$$G_{dc}(s) = \left|\frac{\hat{d}(s)}{\hat{V}_{dc}(s)}\right| = \frac{1}{V_{OSC}} \quad (27)$$

For the rated ac input voltage of 220V, from equation (26) and (27), the loop transfer function of the Zeta converter $G_o(s)$ is estimated as

$$G_o(s) = G_{vd}(s)G_{dc}(s)H(s) = G_{vd}(s) * \frac{1}{V_{OSC}} * \frac{V_{ref}}{V_{dc}}$$

$$G_o(s) = \frac{1.814 * 10^{-6}\, s^2 - 8.67 * 10^{-3}\, s + 697}{3.054 * 10^{-11}\, s^4 + 2.444 * 10^{-10}\, s^3 + 1.256 * 10^{-2}\, s^2 + 0.1005\, s + 1} \quad (28)$$

D. Control Scheme for Zeta converter

Here a PI controller and pulse width modulator is used to control this converter and maintain the output voltage constant. System uses voltage control scheme and sends pulse to power switch (M).

1) *PI Controller:* It is a voltage controller which senses the output DC voltage (V_{dc}) and compares with reference voltage (V_r) to generate error voltage signal (V_e).

$$V_e = V_r - V_{dc}$$

The output of PI voltage regulator at n^{th} sampling instant can be given as,
$I_c(n) = I_c(n-1) + K_p\{V_e(n) - V_e(n-1)\} + K_i V_e(n)$
Where, K_p and K_i are the proportional and integral gains.

2) *PWM signal Generation:* To reduce current harmonics and to get unity power factor, the input supply current must follow the shape of input voltage. PWM signal is generated by comparing output of PI controller and fixed frequency carrier wave and works as gate input signal for power MOSFET switch of the PFC Zeta converter.

If $K_c * I_c(n) >$ carrier signal, then M=1 else M = 0.

E. Design and Analysis of PI Controller

A PI controller is designed for the stability of the Zeta converter in closed loop control. Figure-4 shows the schematic circuit of that PI controller network and the transfer function of the this network is defined as,

$$G_c(s) = \frac{(1 + sR_1C_3)}{sR_2[(C_3 + C_4) + sR_1C_3C_4]} \quad (29)$$

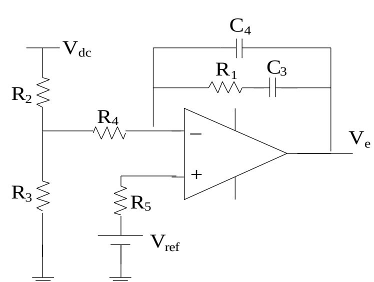

Figure: 4

From Zeta converter based LED driver, the value of $L_1 = L_2 = 40mH$, $C_2 = 833\mu F$, $f_s = 60kHz$, $V_{dc} = 60V$, V_{OSC}=4.5Volt, $V_{ref} = 1.05V$ (from IC datasheet), $\Delta V_{ovp} = 3V$(from IC datasheet), BW = 20Hz are taken to get the values of different components of PI controller network.

$$R_2 = \Delta V_{ovp}/3\mu A = 100k\Omega \quad (30)$$

$$R_3 = \frac{R_2 V_{ref}}{V_{dc} - V_{ref}} \quad (31)$$

$$R_1 = \frac{R_3 V_{ref}}{V_{osc} - V_{ref}} \quad (32)$$

$$f_0 = \frac{1}{2\pi\sqrt{L_2 C_2}} \quad (33)$$

$$f_z = .75 f_0 Hz \quad (34)$$

$$C_3 = \frac{1}{2\pi R_1 f_z} \quad (35)$$

$$C_4 = \frac{1}{2\pi(R_2 \| R_3)BW} \quad (36)$$

After putting values of components in equation (29), the transfer function of PI controller can be expressed as

$$G_c(s) = \frac{7.6 \times 10^{-3}s + 1}{3.45 \times 10^{-3}s^2 + 1.86s} \quad (37)$$

F. Stability Analysis of zeta converter based LED driver

The stability analysis of CCM Zeta converter based LED driver is carried out using small-signal state space model. The state space model of the Zeta converter is developed considering that the diode, active switch, PFC buck inductor and dc link capacitor are considered ideal. Figure 1 shows the basic diagram of the Zeta converter and equation 38 shows the transfer function of open loop system. After drawing the Bode diagram in figure-5, gain margin of 21.3dB and phase margin of 2.05deg was found which is not acceptable for stability of a practical system.

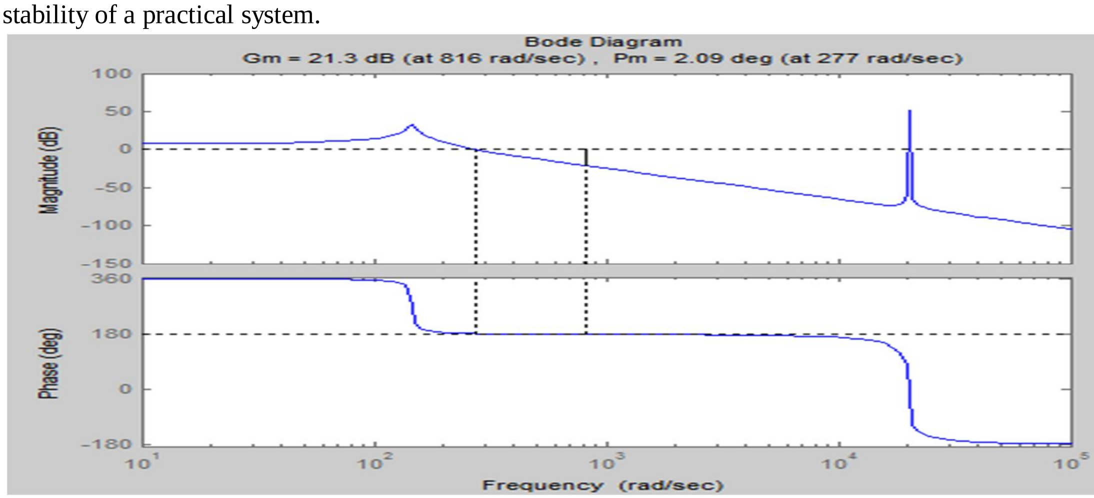

Figure: 5

Hence, it is required to increases the phase margin by more than 45^0 for the stability of the converter in closed loop system. Here a designed PI controller has been selected with transfer function $G_c(s)$ shown in equation (37). Closed loop transfer function with compensated network can be written as below

$$C(s) = G_o(s)G_c(s) \quad (38)$$

Now for equation (38), Bode is shown in Figure -6 which is clearly indicating the stability of system with gain margin of 13.7dB and phase margin of 90.4 deg.

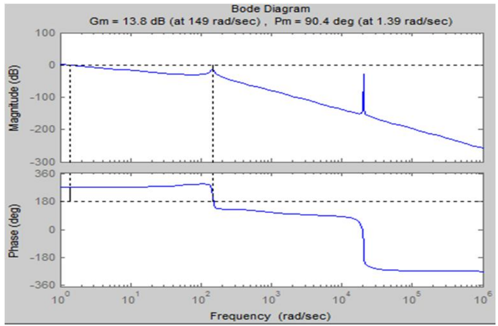

Figure: 6

G. MATLAB Model of Proposed Zeta converter based LED Driver

The model of the proposed PFC Zeta converter based LED driver is developed in MATLAB/Simulink and it is shown in Figure 6 under normal running condition in which the lamp is considered as a resistor at high frequency.

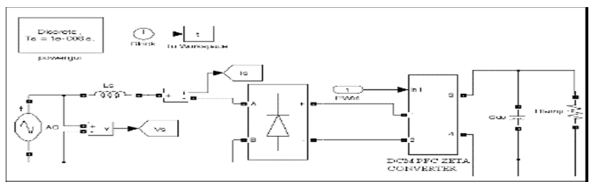

Figure: 7 Model of Proposed LED driver

The topology based on PFC Zeta converter is modeled in the MATLAB-Simulink toolbox where Proportional Integral (PI) controller where voltage follower technique is used to operate it in continuous condition mode (CCM). The switching frequency is 60 kHz to generate PWM pulses which works as gate input to on the solid state power switch. The designed values of the Zeta converter components obtained from equations (1)-(4) are selected appropriately to obtain better power quality improvement at universal input AC mains. These component values along with PI controller gain parameters are provided in Appendix.

II. CONCLUSIONS

In this paper, modelling and analyzing of the Zeta converter operating in continuous conduction mode were presented. Application of the proposed based on averaging modelling method for extracting associated transfer functions and modellingadcdc Zeta converter was investigated. In this process, for modelling the average and small signal linearization techniques were employed. Extracting the final transfer functions from initial state space equations were described step by step. Application of averagingmodelling's rule helps to solve the high order complex equations simply. The presented method deals with the equations with more state variables as well. In this paper, the transfer functions from input to output and control to output were o btained. Then, by using the proposed method the poles, zeros, root□locus plot and Bode diagrams were extracted and the achieved frequency response was analyzed. Finally, the efficiency of the proposed tuned PI controller as a model based technique to design a proper control system is shown. The proposed control system employs the PI controller with a special adjustment for proper setting of the control responses.

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BIOGRABHY ABOUT AUTHOR

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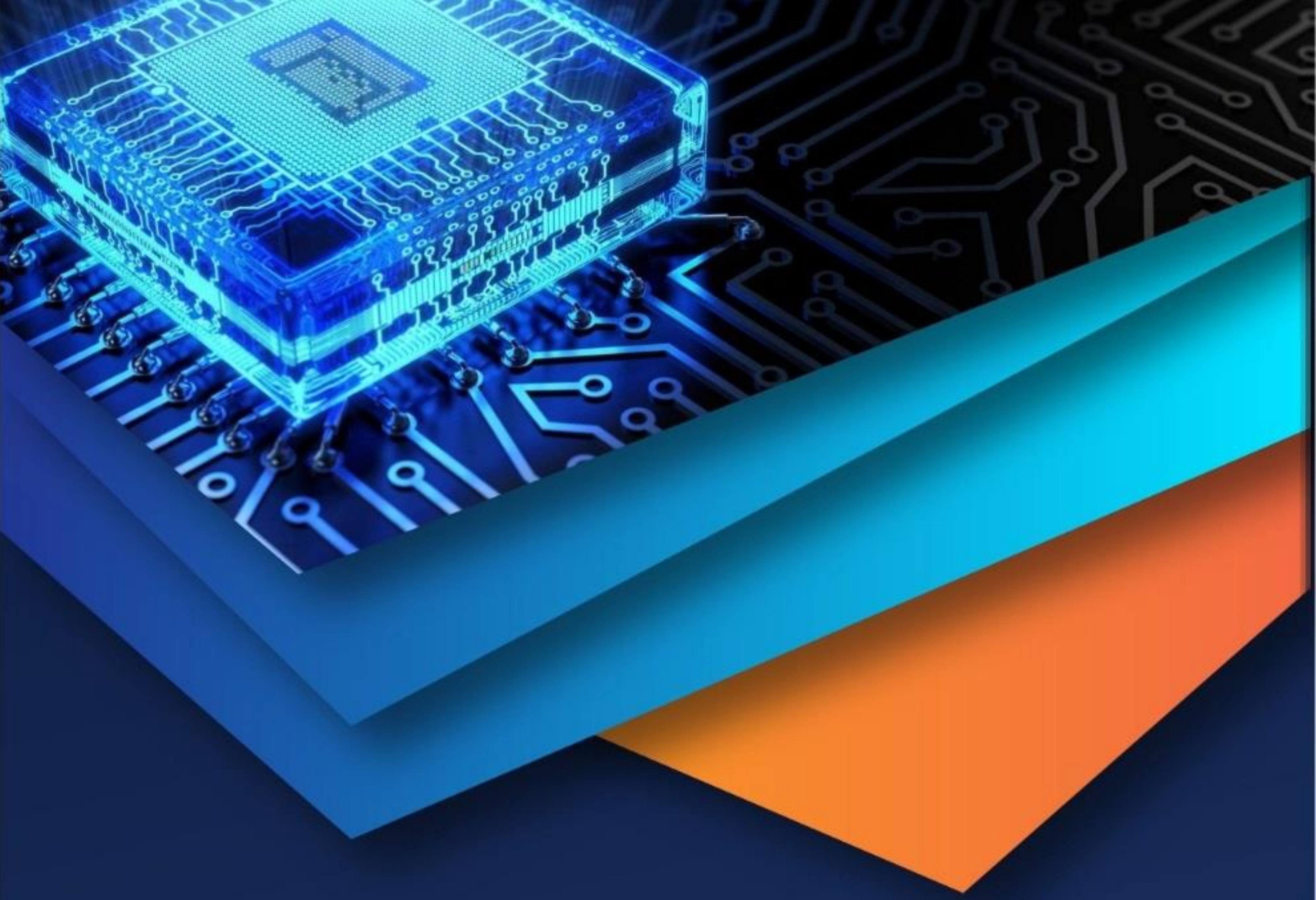

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