iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 8 **Issue:** IX **Month of publication:** September 2020

DOI: https://doi.org/10.22214/ijraset.2020.31307

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue IX Sep 2020- Available at www.ijraset.com

Implementation of Time Efficient VLSI Design using Kogge Stone Adder

K. Aishwarya Sindhuja[1], S. K. Binu Siva Singh[2]
[1]*PG Scholar,* [2]*Assistant Professor, Department of VLSI Design, Jeppiaar Engineering College,Chennai-600119*

Abstract: ***In this paper, an efficient parallel processing architecture using Least mean square (LMS) adaptive filter based on Distributed arithmetic (DA). The DA based LMS adaptive filter requires look up tables (LUTs) for filtering and weight updating operations. In this scheme the LUT size is reduced to half by using the Offset Binary Coding (OBC) technique, where the combinations of filter weights and input samples is given to the filter is done by Multiply and Accumulation (MAC) process. The accumulation of the combinational inputs process is done by Kogge Stone Adder(Parallel Prefix Adder)instead of using Carry Select Adder and also the usage of gates in the circuit design is get reduced and this can achieve the less area Consumption of the proposed system. Here in the proposed system Offset binary coding technique reduces the LUT size by half comparing with the Non-OBC technique. The algorithm is written in Verilog HDL and tested on Xilinx 14.7 ISE and the algorithm is implemented in FPGA Vertex 5.***

Keywords: ***Kogge Stone Adder, Offset Binar Coding, Least mean square, Digital signal processing, Multiply and Accumulate, Distributed arithmetic, Lookup table, Finite impulse response.***

I. INTRODUCTION

Most movable electronic devices like cellular phones, personal digital assistants, and hearing aids need digital signal process (DSP) for prime performance. because of the inflated demand of the implementation of refined DSP algorithms, low price styles, i.e., low space and power price, square measure required to form these hand-held devices tiny with sensible performance. numerous varieties of DSP operations square measure used in follow. Filtering is one amongst the foremost wide used signal process operations. For FIR filters, output y(n) may be a linear convolution of weights w(n) and inputs x(n) adaptative square measure wide utilized in many digital signal process applications. The finite impulse response (FIR) adaptative whose weights square measure updated by the noted least mean sq. (LMS) algorithmic program is that the most popularly used adaptative filter not solely because of its simplicity however conjointly because of its satisfactory convergence performance. The direct type type on the forward path of the FIR filter ends up in an extended essential path because of Associate in Nursing dot product computation to get to get output. Therefore, once the input features a high rate, it's necessary to scale back the essential path of the structure so the essential path couldn't exceed the sampling amount. Since general purpose multipliers need need chip space, alternate ways of implementing multiplication square measure usually used, significantly once the coefficients values square measure better known before implementation. Distributed arithmetic (DA) is a technique to implement convolution number less, wherever the waterproof operations square measure replaced by a series of LUT access and summations. Techniques, like memory decomposition and Offset Binary committal to writing (OBC) will scale back the LUT size, which might otherwise increase exponentially with the filter length for typical prosecuting attorney. However, in many applications such as echo cancelation and system identification, coefficient adaptation is needed. This adaptation makes it challenging to implement DA based adaptive filters with low cost due to the necessity of updating LUTs. Several approaches have been developed for DA based adaptive filters, i.e., from the point of view of reducing logic complexity.

It has been noted that, nobody has mentioned the issues of space and power consumptions of public prosecutor based mostly LMS reconciling reconciling once LUT decomposition is applied actuated by the works, a non rotten LUT design is planned supported storing the OBC mixtures of input samples and weightage units. The essential goal of the system is to reduced the scale of search table and to realize high potency by the Offset Binary cryptography Technique.

II. METHODLOGY

The main theme of this planned system is LUT size is reduced to half by exploitation the Offset binary committal to writing (OBC) technique, once the combos of filter weights and input samples is given to the filter that is known as as Multiply and Accumulation (MAC) method. The orders of filter will increase the potency of the system adjustive is extensively utilized in noise and echo cancellation, system identification, channel estimation and effort. It contains of a linear finite impulse response (FIR) filter whose transfer operate is adjusted by dynamic the filter weights in keeping with associate degree optimisation algorithmic rule. Usually,

©IJRASET: All Rights are Reserved

least mean sq. (LMS) algorithmic rule is most popular to update the filter weights thanks to its simplicity and simple implementation.

In order to hold out the required tasks for filtering and weight change operations. we've got to know to know operation of projected style. Initially, all the input samples square measure keep in register bank with least significant bits (LSBs) of every register forms the address lines of W LUT. The ordered reading of contents from W LUT and followed by shift accumulation (SA) can manufacture the output.

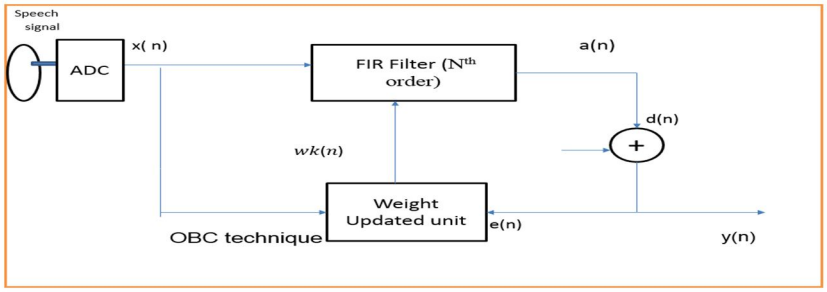


Fig.1 System Level diagram of proposed DA based LMS adaptive filter

OBC can be used to reduce the LUT size by a factor of 2 to 2N−1. By rewriting the input , The OBC scheme is described . The LUT contents for a four tap FIR filter are given. It can be observed that the first half and the second half of this LUT are mirrored vertically. Therefore, its size can be halved by using xj to control the sign of each entry at the cost of a slightly increased hardware complexity. The hardware circuit for implementing a K tap filter, where j starts from j = B −1 and decreases by 1 each cycle until j =0 . S1 is 0 when j =0 and 1 if otherwise, and S2 is 1 when j = B −1 and 0 if otherwise. OBC is derived as follows.

Kogge Stone Adder could be a parallel prefix type carry look ahead adder.It generates carry in O (logn) time and is wide thought-about because the quickest adder and is wide employed in the business for prime performance arithmetic circuits.In KSA, carries square measure computed quick by computing them in parallel at the value of enhanced space.Pre process This step involves computation of generate and propagate signals corresponding too every combine of bits in a very and B.These signals square measure given by the logic equations below: pi = Ai xor Bi gi = Ai and Bi Carry look ahead network This block differentiates KSA fromdifferent adders and is that the main force behind its high performance.This step involves computation of carries cherish every bit.It uses cluster propagate and generate as intermediate signals that square measure given by the logic equations below Pi:j = Pi:k 1 and Pk:j Gi:j = Gi:k 1 or (Pi:k 1 and Gk:j) Post process this is often the ultimate step and is common to any or all adders of this family (carry look ahead) total bits square measure computed by the logic given below: Si = pi xor Ci-1.

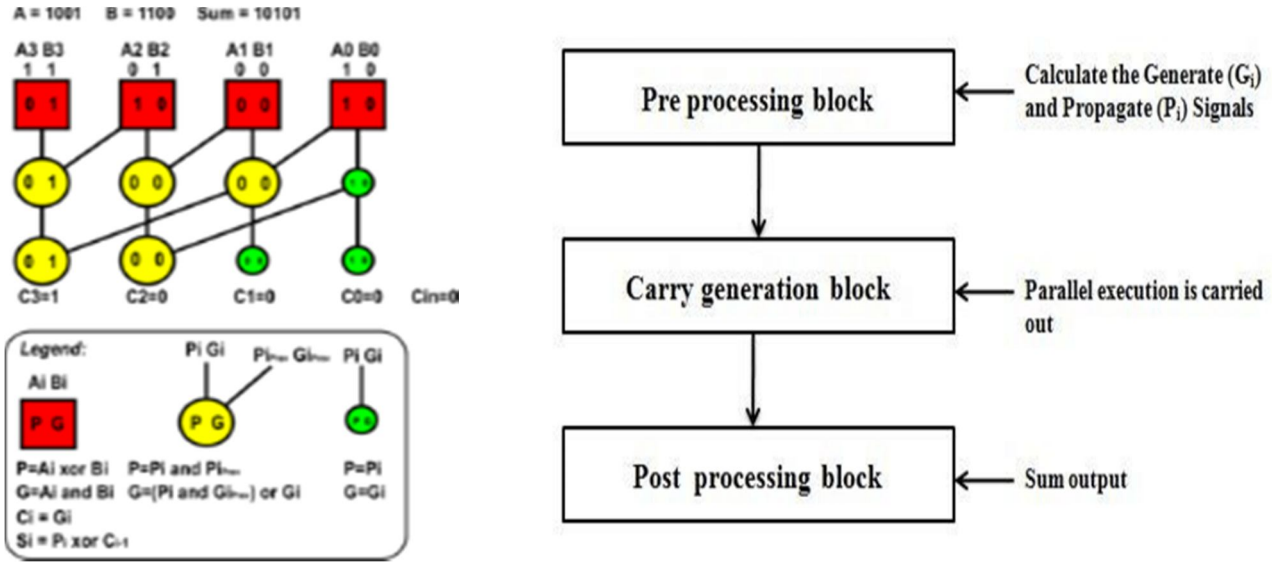


Fig.2 Kogge Stone Adder

©IJRASET: All Rights are Reserved

III. RESULT AND DISCUSSION

In this work, the performance of Carry Select Adder and Kogge Stone Adder (Parallel Prefix Adder) using OBC technique are compared and tabulated .From this tabulation we know that,by using the Kogge Stone Adder with OBC technique the speed of the system get increased.

A. Performance Evaluation of Kogge Stone Adder using OBC Technique

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	270	768	35%
Number of Slice Flip Flops	311	1536	20%
Number of 4 input LUTs	445	1536	28%
Number of bonded IOBs	19	124	15%
Number of GCLKs	1	8	12%

Fig.3 Performance evaluation OBC Technique

B. Timing Summary

1) Timing Summary of the filter using Carry Select Adder is given below .

```
   Minimum period: 9.021ns (Maximum Frequency: 110.854MHz)
   Minimum input arrival time before clock: 6.346ns
   Maximum output required time after clock: 6.441ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
```

Fig.5 Timing Summary of Carry Select Adder

2) Timing Summary of the filter using Kogge Stone Adder is given Below.

```
   Minimum period: 3.733ns (Maximum Frequency: 267.860MHz)
   Minimum input arrival time before clock: 2.093ns
   Maximum output required time after clock: 2.806ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

Fig.6 Timing Summary of Kogge Stone Adder

3) Output Simulation Of Kogge Stone Adder using OBC Technique

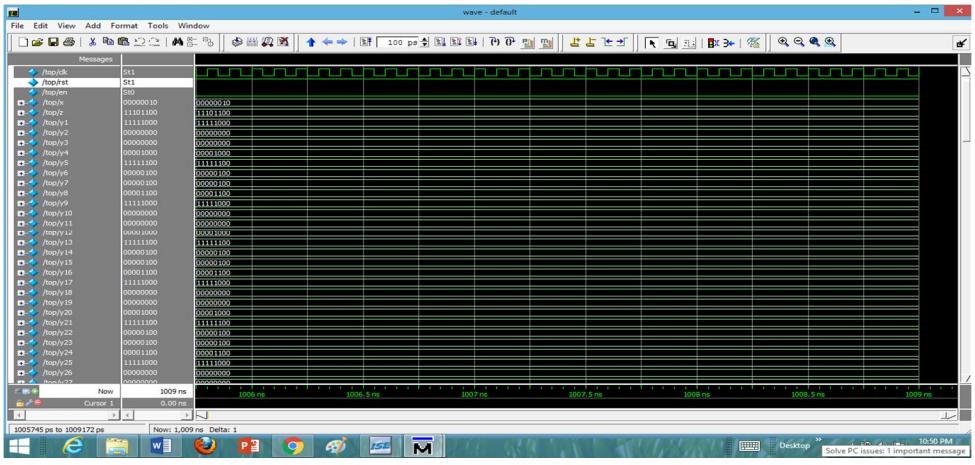


Fig. 6 Simulation Output

©IJRASET: All Rights are Reserved

4) The bar chart comparison of Speed Range of Carry Select Adder and Kogge Stone Adder is given below:

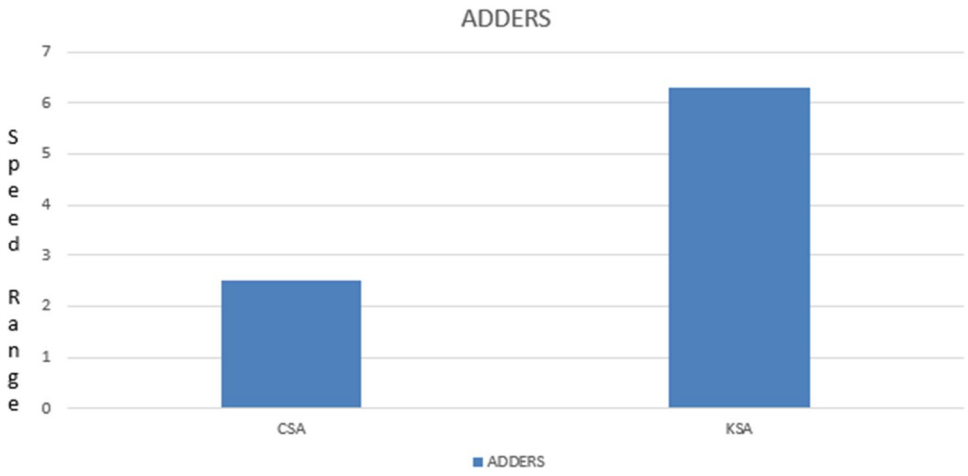


Fig.7 Bar Chart Camparision Of Adders

IV. CONCLUSION

In this work, the speed of the system is increased by using Kogge Stone Adder which is a high speed adder than the carry select adder using Offset Binary coding which consumes less area when compared with Non-OBC tecnique. The proposed technique is executed by utilizing Xilinx (ISE 12.4).

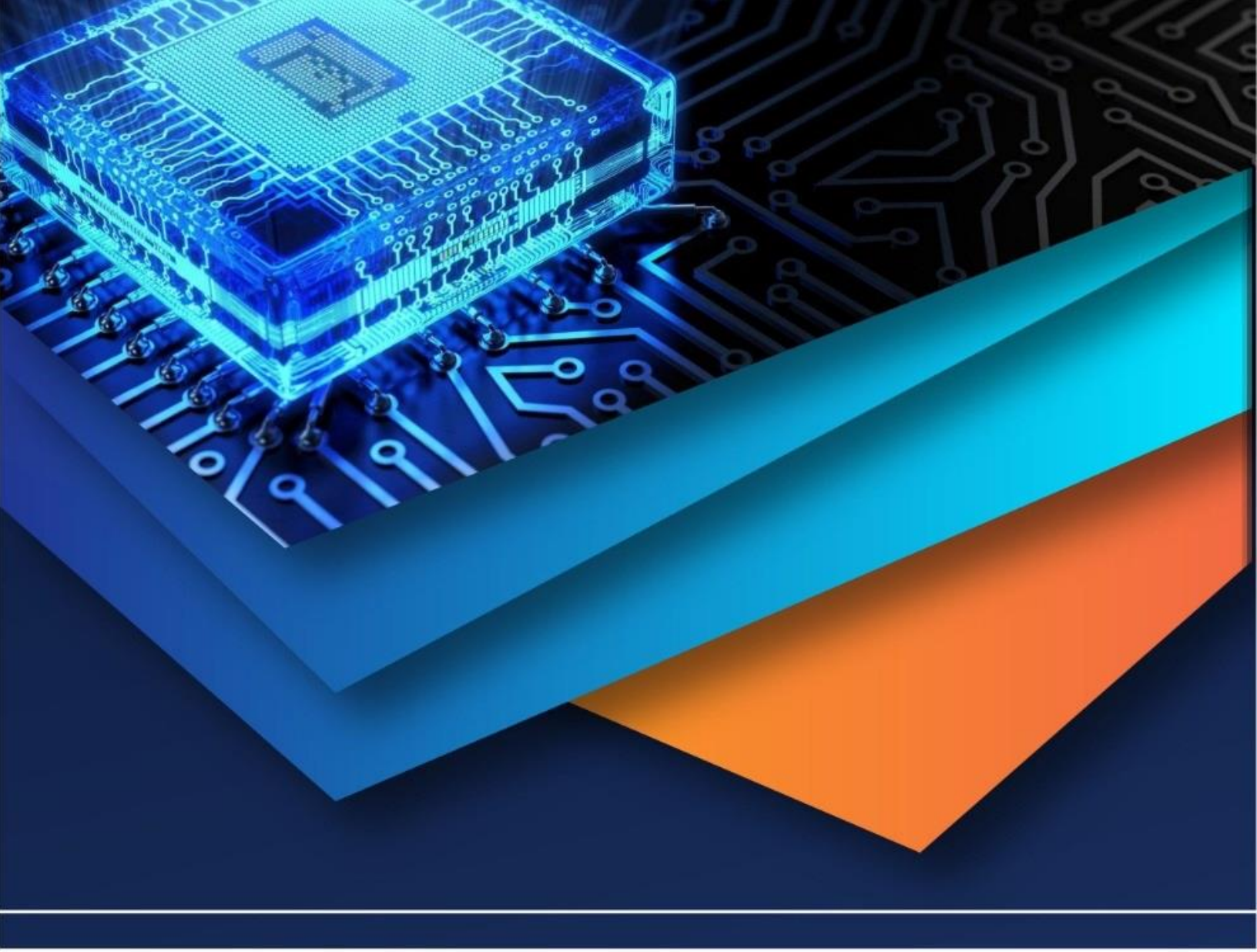
V. ACKNOWLEDGMENT

The authors want to acknowledge Department of ECE , Jeppiaar Engineering College,Chennai,India for providing necessary facility.

REFERENCES

[1] .Swaroop Ghosh, Patrick Ndai, Kaushik Roy. "A Novel Low Overhead Fault Tolerant Kogge-Stone Adder Using Adaptive Clocking", vol. 07, no. 11, pp. 781–787. DATE 2008.
[2] Guo, Rui and DeBrunner, Linda S, “A novel adaptive filter implementation scheme using distributed arithmetic,” in Signals, Systems and Computers (ASILOMAR), 2011 Conference Record of the Forty Fifth Asilomar Conference on. IEEE, 2011, pp. 160–164.
[3] M. S. Prakash and R. A. Shaik, “Low area and high throughput architecture for an adaptive filter using distributed arithmetic,” Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 60, no. 11, pp. 781–785, 2013.
[4] S. Y. Park and P. K. Meher, “Low power, high throughput, and low area adaptive fir filter based on distributed arithmetic,” Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 60, no. 6, pp. 346–350, 2013.
[5] P. K. Meher and S. Y. Park, “High throughput pipelined realization of adaptive fir filter based on distributed arithmetic,” in VLSI and System on Chip (VLSI SoC), 2011 IEEE/IFIP 19th International Conference on. IEEE, 2011, pp. 428–433.
[6] B. K. Mohanty, P. K. Meher, and S. K. Patel, “LUT optimization for distributed arithmetic based block least mean square adaptive filter,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 5, pp. 1926–1935, 2016.
[7] B. K. Mohanty and P. K. Meher, “A high performance energy efficient architecture for fir adaptive filter based on new distributed arithmetic formulation of block lms algorithm,” IEEE transactions on signal processing, vol. 61, no. 4, pp. 921–932, 2013
[8] C. F. N. Cowan and J. Mavor. New digital-adaptive filter implementation using distributed-arithmetic techniques. IEE Proceedings, 128, Pt. F(4):225–230, August 1981.
[9] C. H. Wei and J. J. Lou. Multimemory block structure for implementing a digital adaptive filter using distributed arith- metic. IEE Proceedings, 133, Pt. G(1):19–26, February 1986.
[10] S. A. White. Applications of distributed arithmetic to digital signal processing: A tutorial review. IEEE ASSP Magazine, 6:4–19, July 1989.
[11] S. A. White, “Applications of distributed arithmetic to digital signal processing: A tutorial review,” IEEE ASSP Mag., vol. 6, no. 3, pp. 4–19, Jul. 1989.
[12] R. Guo and L. S. DeBrunner, “Two high performance adaptive filter implementation schemes using distributed arithmetic,” Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 58, no. 9, pp. 600–604, 2011
[13] D. J. Allred, H. Yoo, V. Krishnan, W. Huang, and D. V. Anderson, “LMS adaptive filters using distributed arithmetic for high throughput,” Circuits and Systems I: IEEE Transactions on, vol. 52, 1327–1337, 2010.
[14] .J. Rabaey, "Digital Integrated Circuits: A Design Perspective", Prentice Hall, , vol. 11, no. 11, pp. 881–7851556

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)