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Design of High gain LNA using 180nm CMOS for Wearable Devices Network

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Abstract: ***Low Noise Amplifier is the very importance block in any receiver front end. This paper presents the design of a Low Noise Amplifier (LNA) operating at 2.4 GHz for wearable devices for Wireless Body Area Network (WBAN) using 0.18 um CMOS technology. The proposed circuit is a single stage low noise amplifier based on the inductive source degeneration topology for achieving best impedance matching and stability. The cascade design of CMOS is used to achieve high gain of 22.904 dB and very low noise figure of 0.814 dB. The proposed LNAs is made to operate with supply voltage of 1.8 V. The designed circuit and results are simulated using Advanced Design System (ADS) software by tuning some library files and LNA parameters.***

Keywords: ADS, CMOS, Inductive source degeneration, Low noise amplifier, WBAN

I. INTRODUCTION

The wearable devices are vital wireless application of a micro-lightweight device to be easily wore. Wearing a device for example smart watches, tracking devices, VR glasses not only entertain, but check and analyze physical conditions, providing users such as footprints, burning calories, blood pressure info to improve their life quality. A body area network (BAN), also referred to as a wireless body area network (WBAN) or a body sensor network (BSN) or a medical body area network (MBAN), is a wireless network of wearable computing devices. Wearable devices may be embedded inside the body, implants, may be surface-mounted on the body in a fixed position. The IEEE 802.15.6 standard supports 2.4 GHz band for RF transceiver of wearable sensors.

The existing design of LNA for wearable sensor network is designed using 40nm CMOS technology using current reuse technique but it has resulted in high noise figure with moderate gain [1] Hence the proposed LNA is designed with the aim of achieving improved gain and low noise figure with low voltage supply. The description of this paper is depicted as follows. In Section II, the proposed LNA is explained and analyzed. The simulation results of the LNA are presented in Section III. The conclusion details and performance comparison between the proposed Low Noise Amplifier and some previously designed Low Noise Amplifiers is tabulated and analysed in Section IV.

II. DESIGNED LNA

A. Topology Analysis

There are different LNA topologies such as Resistive Termination, Series Shunt Feedback, Common gate termination, Inductor degeneration, common gate, common source, cascade and current reuse topology etc. The analysis of the advantages and disadvantages of all the topologies leads to the conclusion that the most preferable topology for LNA design is the common source topology as it can produce high gain which is the main performance parameter for the LNA. By implementing the inductive source degeneration, the best performance LNA for narrowband applications can be designed. The main advantages of inductive source degeneration LNA are low Noise Figure (NF), high stability, linearity and low power consumption. The main disadvantage of this topology is that the poor isolation than other topologies. It is seen that cascode design can provide good isolation. Hence cascode inductor source degeneration is chosen for designing the proposed LNA.

B. Conventional LNA

In the inductively source degenerated cascode LNA, L_s adds a real part to the input impedance, while (L_g+L_s) resonates with C_{gs} (gate-source capacitance) of M] to provide impedance matching at the operating frequency. Ideally, L_s adds no noise to the system, making this input matching method highly attractive. In order to increase the gain the L_s value should be lesser than 0.1 nH which is difficult to be implemented on chip Hence capacitance C_{gs} is used to increase the Source Degenerated inductor value. The input impedance of the LNA is well known to be

$$Z_{in}= (1/(j\omega C_{gs})) \parallel (j\omega (L_g+L_s)) \parallel (g_m*L_s/C_{gs}) \quad (1)$$

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By using the below formula we can achieve the input impedance matching to 50 Ohms.

$g_m * L_s / C_{gs} = 50$ (2)

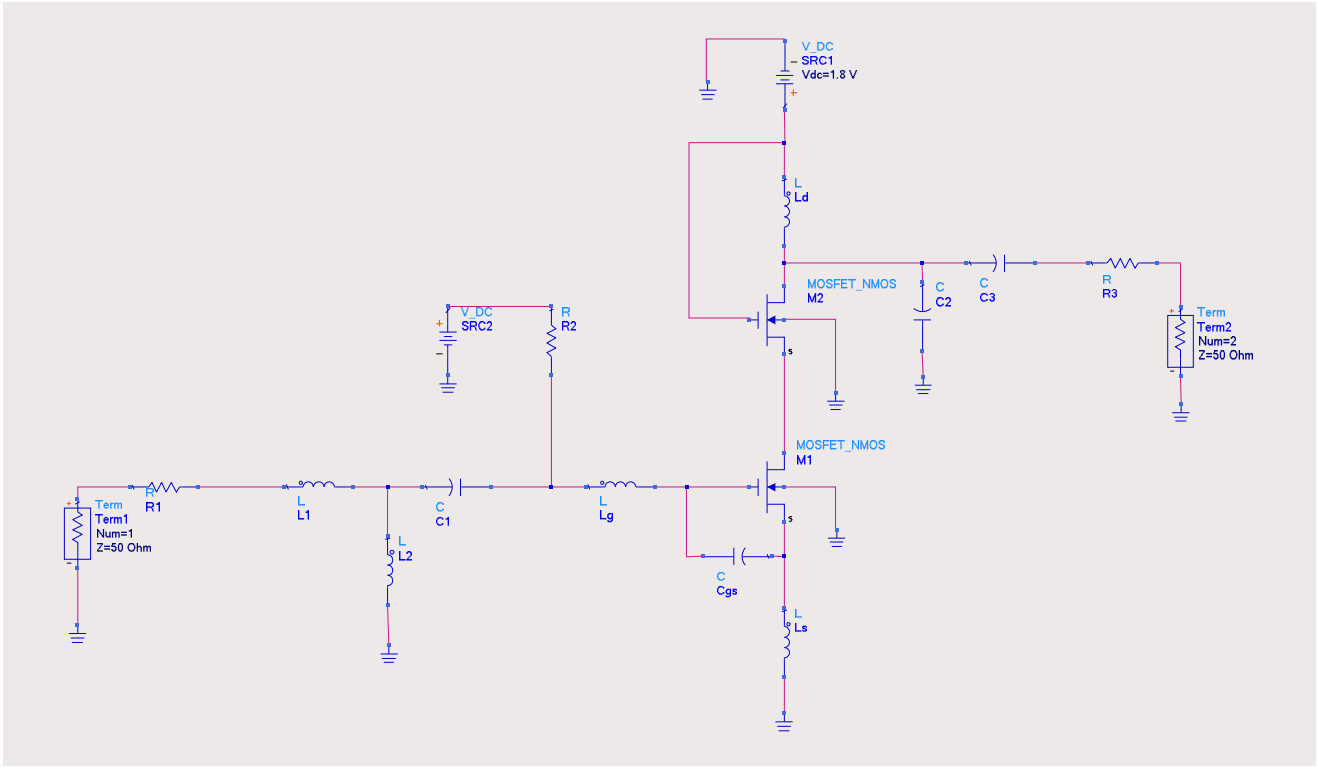


Fig 1: Schematic diagram of proposed Low Noise Amplifier

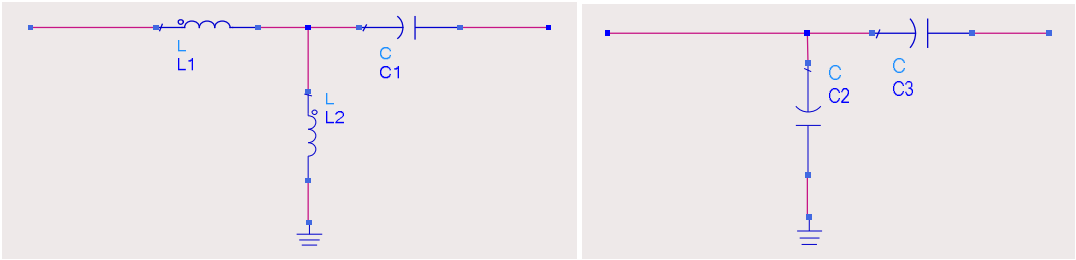


Fig 2: Input and Output Matching Circuits

C. Proposed LNA Architecture

Based on the above topology analysis and considering our application to be Wearable devices Network. The proposed LNA design uses the inductively degenerated LNA architecture .The cascode structure also helps to obtain higher input-output isolation and high gain .The circuit is made to operate with supply 1.8V . Mosfet M1 of the common-source stage and M2 of the cascode stage are given the proper biasing voltages.

Table 1: Important circuit components of proposed LNA

Circuit Components	Values
MOSFET-1	360µm/0.18µm
MOSFET-2	85µm/0.18µm
L_g	2.56nH
L_d	1nH
C7	1pF

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D. Impedance Matching circuits

Though minimum noise figure is obtained by the proposed LNA's common-source cascade topology, the input matching of this configuration is not suitable. Hence the circuit made up of L1, L2 and C1 has been used at the input stage of the amplifier for input matching which in turn has reduced the input reflection coefficient (S11-input return loss). Similarly, in order to ensure the maximum power is transferred to the load, the input and output impedance matching is required. Hence an output matching circuit composed of C2 and C3 is used at the output.

$Z_{in}=(j\omega L1) \parallel (j\omega L2) \parallel (1/j\omega C1)$ (3)

$Z_{out}=(1/j\omega C2)\parallel(1/j\omega C3)$ (4)

III. SIMULATION RESULTS

A. LNA Gain, Return Loss and other S parameters

The designed LNA with cascode design of common source MOSFET helps in achieving high gain of 22.904dB at 2.4GHz frequency. The amplifier gain of the designed LNA is shown in fig.3. By using the input matching circuit, the input impedance approximated to 50 Ω is achieved. The cascode topology helps to enhance the power gain and the reverse isolation of the amplifier. The input reflection coefficient (S11) is -15.393 dB at 2.4 GHz. The output port voltage reflection coefficient (S22) and the reverse isolation (S12) obtained is -12.168 dB and-36.576 dB

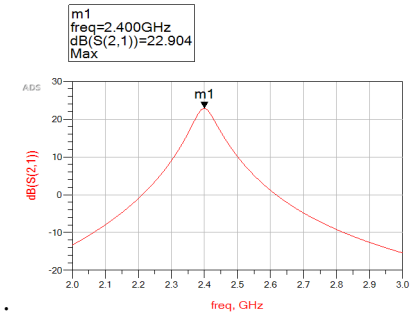


Fig 3: Gain of the LNA

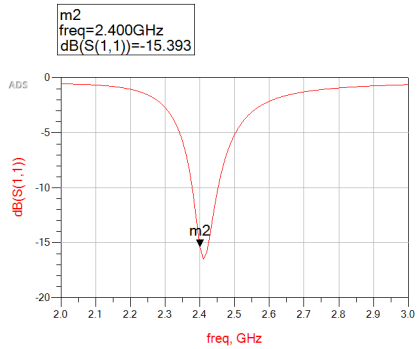


Fig 4: Return Loss of the LNA

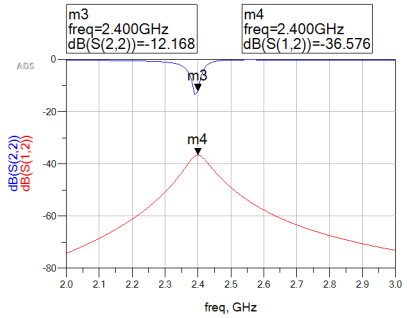


Fig 5: LNA S-Parameters S22 and S12

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B. Noise Figure

Noise figure (NF) gives the measure of reduction of the signal to noise ratio (SNR) during the amplification of the input signal. It is proposed that a good LNA must have very low noise figure value in the range of 0 to 3dB and the minimum noise figure should be lesser than 1.The NF curve shows that the noise figure and minimum noise figure achieved is 0.814 dB and 0.611 dB respectively. The NF plot of the designed LNA is shown in fig 6.

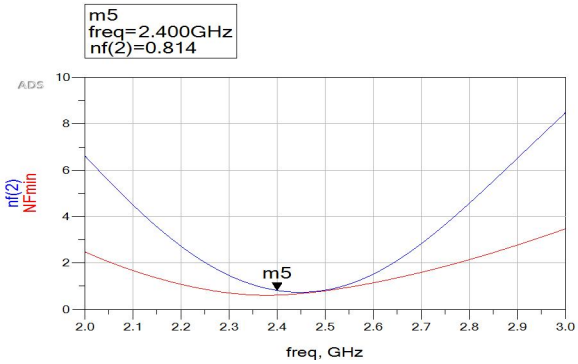


Fig 6: Noise Figure of the LNA

C. Stability factor

For any amplifier the very important property is that it should be stable in its operating range which is defined by the Stability factor K for the LNA. A stable LNA should have K value greater than 1. The K value of designed LNA is 2.274 which is depicted in fig 7. The stability factor can be found using the below formula

$K = (1+|\Delta|2-|S11|2-|S22|2)/(2|S21||S12|)$ (6)

$\Delta = S11S22 - S21S12$ (7)

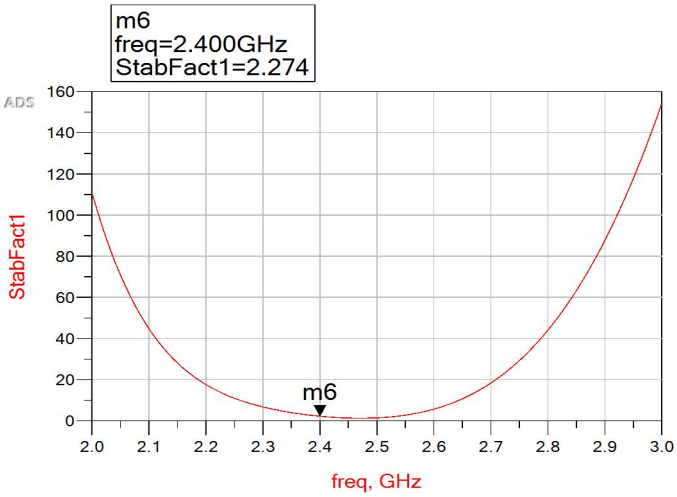


Fig 7: Stability Factor of LNA

IV. CONCLUSION

In this paper, a high gain low noise amplifier is designed for the application of wearable devices network operating at 2.4 GHz using 180nm CMOS technology. The proposed high gain LNA is designed using inductive degeneration topology and cascade of MOSFET. Tuning is also performed in the proposed circuit in order to achieve the high gain. At 2.4 GHz the designed LNA can provide gain of 22.904 dB along with very low noise figure of 0.814 dB. Thus the designed LNA meets the trade off between gain and noise figure in such a way that both requirement is met. The input and output matching circuits are added to the circuit to achieve proper impedance matching. The designed LNA is supplied with supply voltage of 1.8V. The return losses and reverse isolation meets the LNA specifications for wearable devices network. In summary, the designed LNA provides the high gain with low noise figure and proves to be an unconditionally stable low noise amplifier. The performance comparison between the proposed Low Noise Amplifiers and some previously designed Low Noise Amplifiers is tabulated in table 2.

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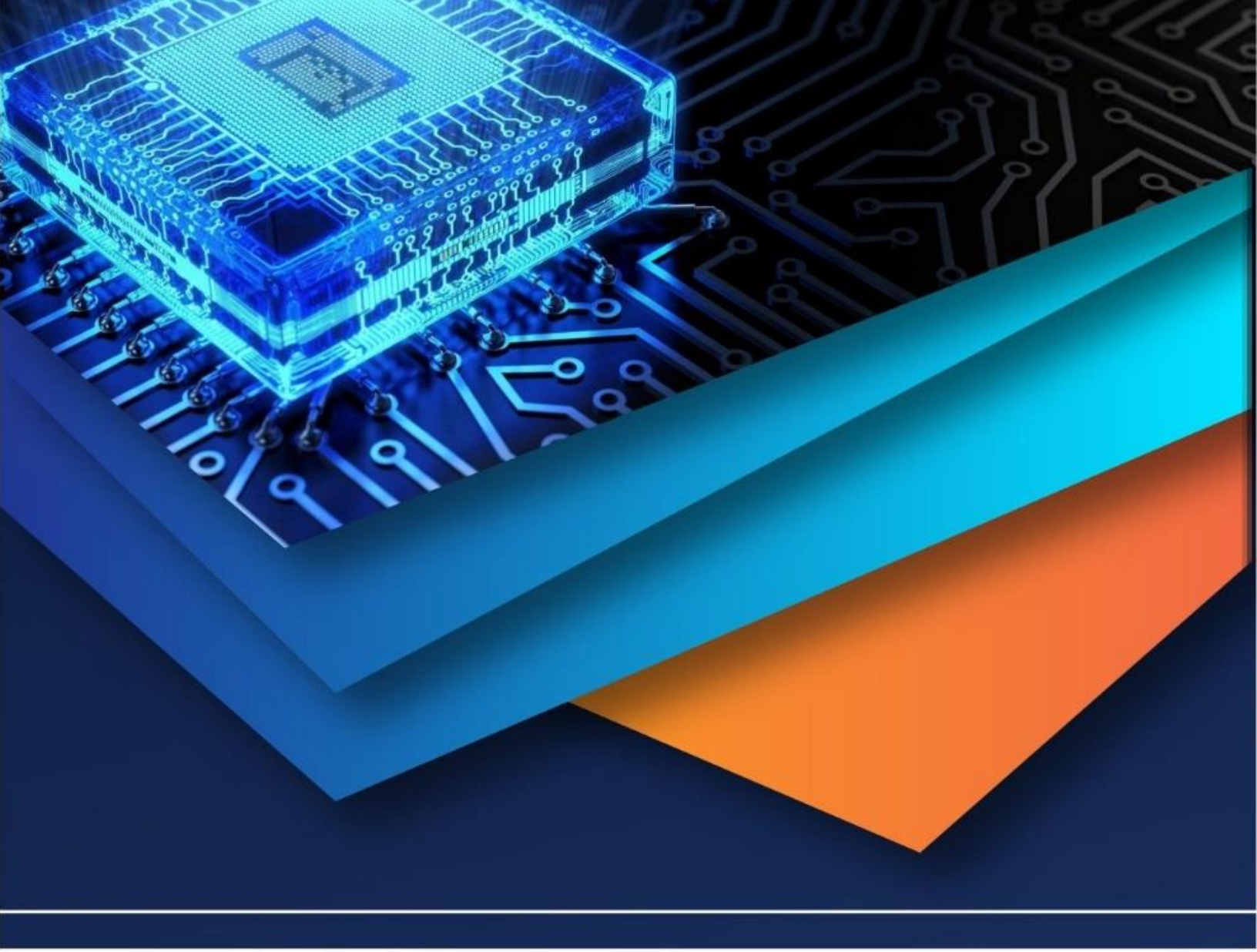
Table 2 : Performance Comparison with Existing Low Noise Amplifie

Reference	Frequency (GHz)	CMOS Technology (nm)	Supply Voltage Vdd (V)	Amplifier Gain S21 (dB)	Noise Figure (dB)	Return Loss S11 (dB)
[2]	2.4	180nm CMOS	1.8	12.68	3.14	-13.5
[3]	2.4	180nm CMOS	1.8	14.55	1.209	-14.15
[5]	2.4	180nm CMOS	1.8	14.7	4.8	-18
[8]	2.4	180nm CMOS	1.8	4.5	2.77	-15.6
[9]	2.4	180nm CMOS	1.8	16.6	2.14	-15.3
[Proposed Work]	2.4	180nm CMOS	1.8	22.904	0.814	-15.393

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