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NOC based Power Efficient Router using Low Power Methodology Clock Gating Techniques

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Abstract: ***The power used by digital integrated circuits has become a key restriction for design and development of VLSI as the device complexity and transistor density increase. Clock-gate synthesis methods are applied to circuits to prune changes in registers by modifying the next-state register functions in order to reduce complex power dissipations. Therefore, sequential inspection of the clock-guided circuits (SEC) is needed for testing this form of synthesis. A new design to rising the efficiency of network-on-chip buffers is being proposed. The non-uniform use of buffers in the network is leveraged and control is used in unusual buffers. A part of the buffer is turned on instead of shutting down the buffer completely. There is a significant performance gain when preferring setup, since the buffer will accept network packages. According to the growing need for better reliability with low energy consumption, scaling up of CMOS technology continued. The Smartphone and battery-operated devices market has further expanded this competition. A variety of processor and System Control methods, such as clock gating, operand separation, memory splits, power gating, dynamic voltage and frequency scaling, etc, are recommended for the research community to meet the challenge of increased energy efficiency and performance. This chapter also analyses other architectures and optimization techniques built in order to reduce power further without noticeable loss of performance or area costs.***
Key word: Clock gating, Density, Efficiency, System control methods, Network on chip, Optimization.

I. INTRODUCTION

Traditional chip system (SoCs) is based on bus. They add problems related to cable delay, noise, power dissipation, signal synchronization. The inter connection architecture of on-chip communication is called Network on Chip (NoC), it provides a high performance communication infrastructure. Networks-on-Chip (or NoCs) have all the specifications to be potential SoCs. It is composed of a series of interconnecting routers and point-to-point channels in a structured way.

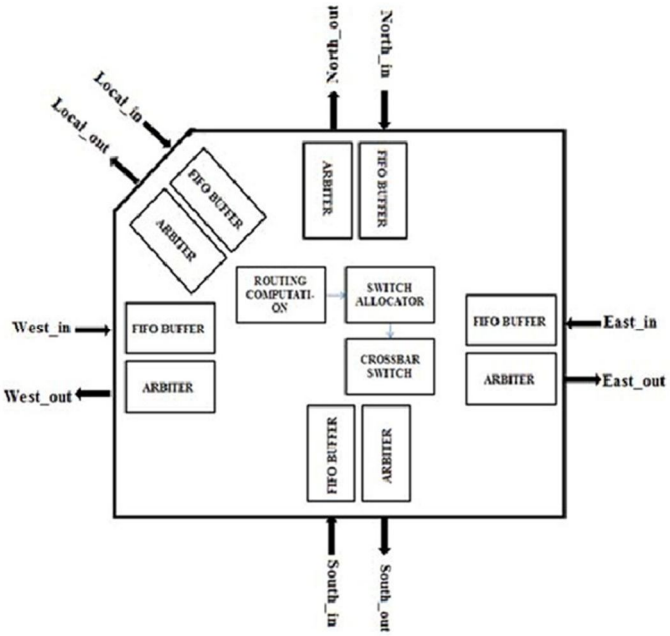


Fig: Basic NOC Router Architecture

Traditional computer network considers collision between packets to be an unavoidable problem, and the ultimate aim of computer networks is to reduce the likelihood of collision, but the possibility of dropped packets is very small in on-chip networks. This is related to the fact that the router's communication links within a NoC are shorter than those in computer networks, thereby allowing tight router synchronization. Some of an on-chip network's characteristics are: low power consumption, small area (in routing nodes), cheap cables, and low interconnect latency. Though traditional computer network characteristics are: long wires, high communication latency, and a lot of complex routing nodes.

Several recent works have proposed the chip network, in the SPIN micro-network is described as an a generic, scalable device on chip interconnect architecture. The SPIN architecture relies on packet switching and point to point bi-directional links between the routers to implement in the micro-network, in the design and implementation of a configurable router intended as a dedicated embedded NoC support module in an FPGA is presented. The router is built using dual crossbar switching and is used to interconnect routers in the handshaking communication protocol. Chip Network (NoC) interconnects IP to boost system performance and power consumption for consumer electronics, automotive and other applications on chip (SoC) devices.

II. PROPOSED DESIGN

Mainly, it is focused on techniques that are deem to minimize the dissipation of power by the links of the network on chip and also by routers and network interfacings of their subscription are expected to increase as per the recent technologies. In particular, this project is a set of data encoding schemes operating at high levels and on an end-to-end base system, which can allows us to minimizing together the switching activity and the coupling switching activity. The proposed encoding methods are presented and discussed at both the algorithmic level and are assessed by means of simulation on synthetic and real traffic situations. The investigation considered into a account of several aspects and metrics of the system design in the communication subsystem, as well as gate area, power dissipation and utilization of energy. The results are shown that by using the proposed encoding methods in the communication system power and the energy can be saved without any momentous reduction in performance and with the area overhead in the NI.

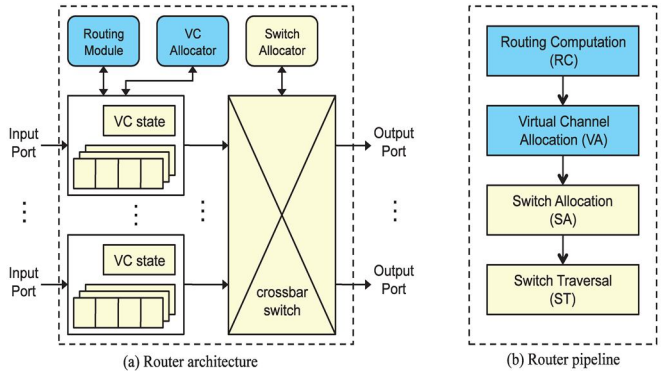


Fig: Router Architecture

1) *FIFO Flexibility Controller (FFC):* This is added to the module for authentic of finding any suitable FIFO in the router in order to store the incoming packets. And it is also responsible to communicate with the output ports to transfer the received packets to their downstream routers according to the routing algorithms used.

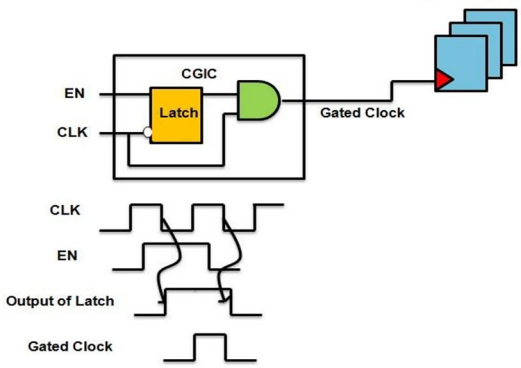


Fig: Clock Gating Technique

2) *FIFO Buffer:* The FIFO can receive packets not only from the direct connected upstream router of the FIFOs of the Base router, but also from other input ports connected in it.
3) *Routing Logic:* Applies the routing algorithm to resolve the packet direction in order to choose the appropriate output ports in the crossbar switch**.**

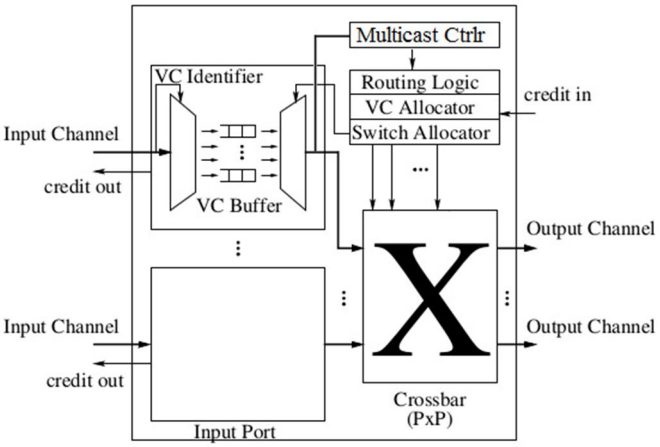


Fig: Internal Functions in the Module

The operation of the Flexible router is the same as the operation of the Base router but in case of working it will be different. When working, the Flexible router will not wait until the requested full FIFO to have one or more free slots as the Base router does, but now the FFC will search for a free slot in any suitable but not full FIFO in the router (including the FIFO of its input port because it may find one or more free slots while searching) by requesting the FIFOs that are not full in other input ports then once it finds a free slot it grants back the request to the upstream router. Then the packet gets transferred to the selected FIFO. After that, the operation of the Flexible router will be exactly similar to the Base router.

III. ROUND ROBIN ALGORITHM

Round Robin algorithm (RRA) is employed because it's a network scheduling process in routers. Round robin scheduling is typically used for time slices (This process is called as time quanta) are assigned to every process in a very circular order, handling all processes without priority (also called as cyclic executive process). Round-robin scheduling is easy and simple to implement and also starvation free. Round-robin scheduling can even be applied to the other scheduling process like data packet scheduling in computer networks. It's an operating system based concept. The name Round robin algorithm came from the round robin principle.

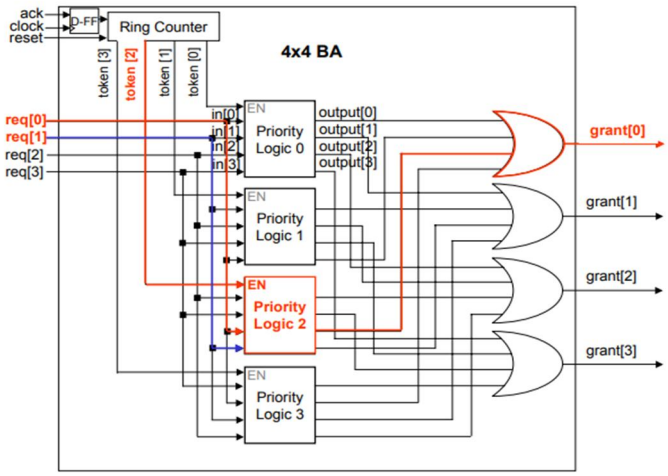
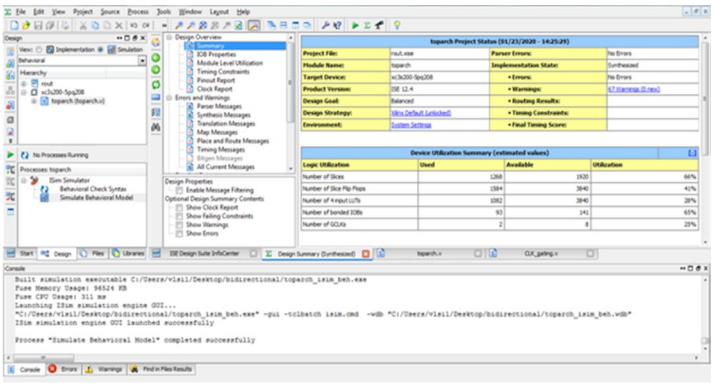


Fig: Round Robin Internal Architecture

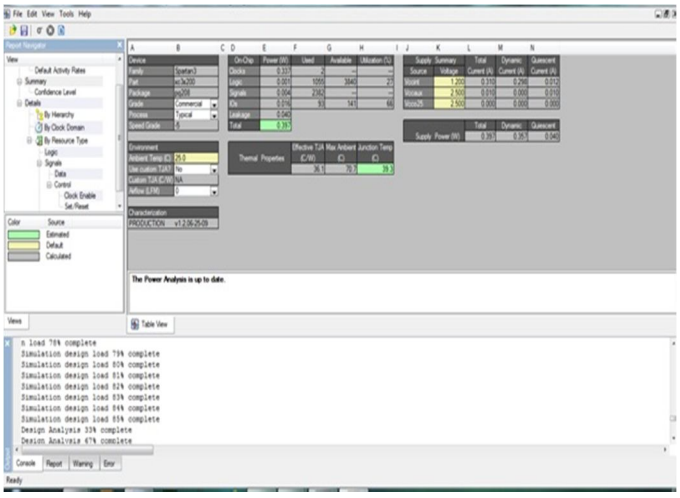
IV. RESULTS AND DISCUSSION

In this work, The performance of Arbiter (Round Robin Algorithm), Crossbar Switch and Router with Crossbar switch and Arbiter are explained and showed by using pictures. Here it is showed the LUT size and power gets reduced. The delay is also gets reduced which is tablulated here.

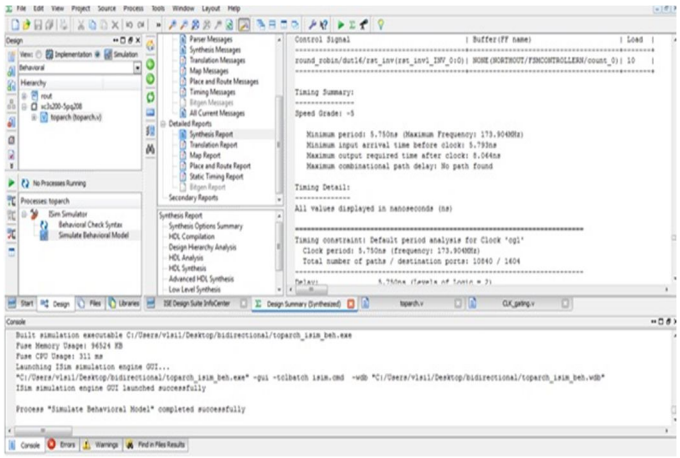
A. Device Utilization Summary of the Module



B. Power Usage in this Module



C. Timing Summary of this Module



D. Table Comparison Of Previous Model And Proposed Model

	Previous model	Proposed model
Min. period	7.928 ns	5.750 ns
Max. frequency	126.132 MHz	173.904 MHz

Note: Compared previous model is 'NoC based router architecture to reduce power using round robin algorithm'

E. Router Output

The output is predicated on the selection pin which is connected between crossbar switch and arbiter. Here, arbiter works under the principle of Round Robin Algorithm.

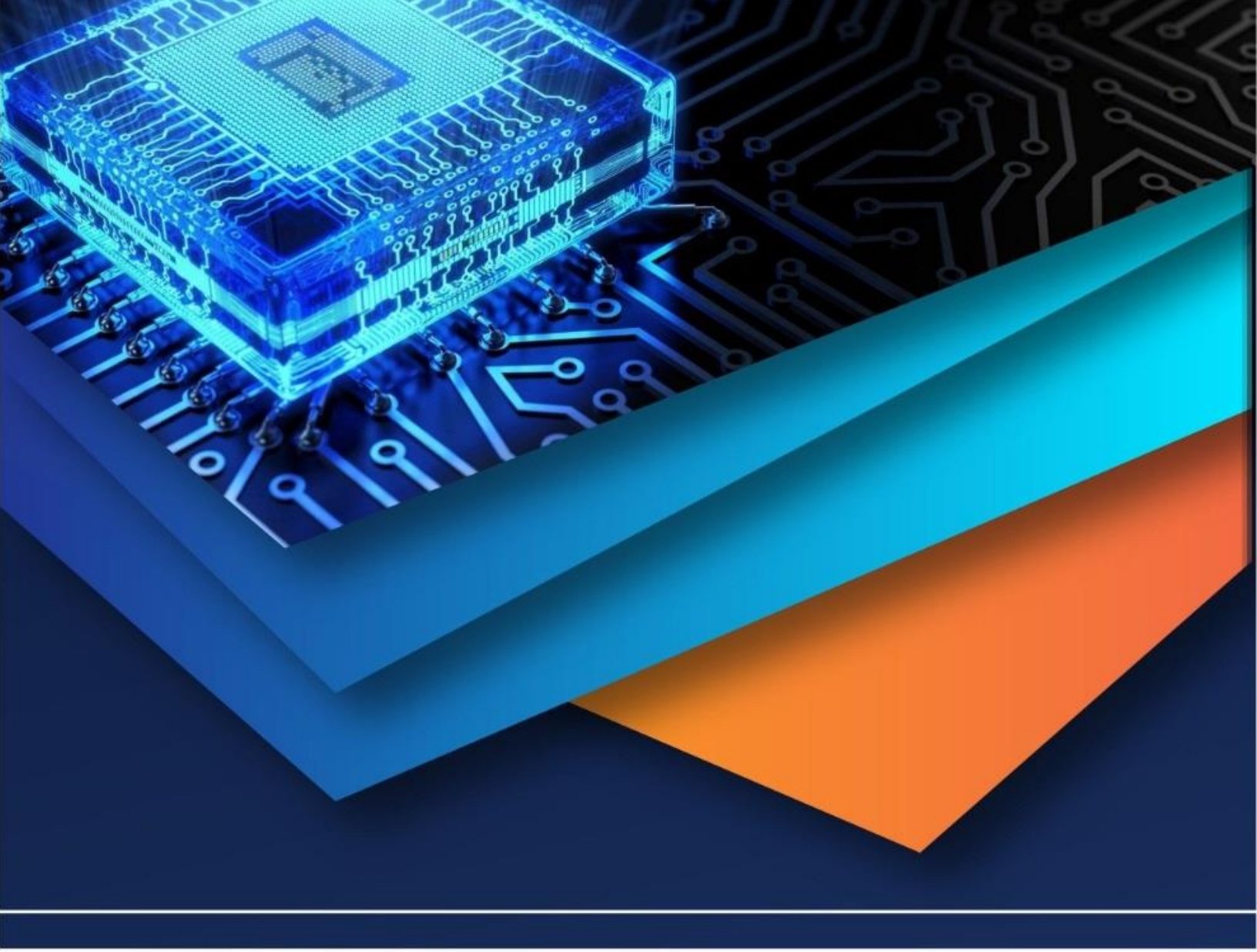
V. CONCLUSION

In some more challenging corner cases, manually identified as the most important and relevant, the network-on-chip was developed, introduced and then tested along with other simple random tests. Such changes can be seen in the future as a logical progression of this mission. In terms of design, better efficiency could be accomplished by speculating on the simulated channel allocation to the router, i.e. by defining the outcome to accomplish it in the same clock period as the head-flit allocation of a single packet.

In recent and future many core systems require NoC to be well designed to ensure both performance and power efficiency. However, as technology continually reducing, leakage power takes up a bigger proportion of total power, and it's increasingly important to cut the leakage power for the power-efficient NoC design. Power gating as a representative low power technique that may applied to NoC to cut back this increasing leakage power. However the disconnection problem severely limits power-gating to be effectively utilized thanks to its negative impact on performance. It proposes a complete unique partial power-gating approach to obviate the disconnection problem with in the power-gated NoC. The approach mainly includes a direction slicing scheme and an improved routing algorithm and a deadlock and live lock recovering mechanism. First, It utilize direction-slicing scheme to separate router into two slices and adopt different power supply modes for them: keeping one slice always-on to construct an energetic and fully connected subnet, while utilizing both power-gating and clock-gating to gate the opposite one is to store possible leakage power and clock power. Second, we redesign the corresponding routing algorithm to support packet transmitting on sliced networks. And third, it offers a novel Deadlock recovery mechanism to resolve the deadlock situation which can happen because of the improved architecture and routing algorithm. In synthetic traffic simulation, results shows that the sliced network with partial power gating is more power efficient at low load range and having better performance behavior than the conventional power gated design.

REFERENCE

[1] Guerrero, G. Maas, and W. Hogland, "Solid wa[1] T. Kogel, M. Doerper, A. Wiefrink, R. Leupers, G. Ascheid, "A Modular Simulation Framework for Architectural Exploration of On-Chip Interconnection Networks," in Proc. IEEE/ACM/IFIP International Conference on Hardware/ Software Codesign and Systems Synthesis (CODES/ISSS), pp. 712, 2003.
[2] B. Dally and B. Towles, "Route Packets, Not Wires: On-Chip Interconnection Networks," in Proc. of IEEE Design Automation Conference (DAC), pp. 684-689, 2001.
[3] N. Binkert, B. Beckmann, G. Black, S. K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. R. Hower, T. Krishna, S. Sardashti, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M. D. Hill and D. A. Wood, "The GEM5 Simulator," SIGARCH Computer Architecture News, vol. 39, no. 2, pp. 1-7, 2011.
[4] E. S. Chung, E. Nurvitadhi, J. C. Hoe, B. Falsafi and K. Mai, "PROToFLEX: FPGA-Accelerated Hybrid Functional Simulator," in IEEE Int'l Symp. on Parallel and Distributed Processing Symposium, vol. 1, no. 6, pp. 26-30, 2007.
[5] Z. Tan, A. Waterman, R. Avizienis, Y. Lee, H. Cook, D. Patterson and K. Asanovic, "RAMP Gold: An FPGA-based Architecture Simulator multiprocessors, "in Proc. Of IEEE Design Automation Conference (DAC), pp. 463468, 2010.
[6] S. S. Mukherjee, P. Bannon, S. Lang, A. Spink and D. Webb, "The Alpha 21364 Network Architecture, " in IEEE Micro, vol. 22, no. 1, pp. 26-35, 2002.
[7] S. Borkar, "Thousand Core Chips: A Technology Perspective," in Proc. of ACM/IEEE Design Automation Conference (DAC), pp. 746749, 2007
[8] J. Nan, J. Balfour, D. U. Becker, B. Towles, W. J. Dally, G. Michelogiannakis and J. Kim, "A Detailed and Flexible Cycle-Accurate Network-on-Chip Simulator," in Performance Analysis of Systems and Software (ISPASS), Proc. of Int'l Symp. on., pp. 86-96, 2013.
[9] K. Goossens, J. Dielissen, O. P. Gangwal, S. G. Pestana, A. Radulescu and E. Rijpkema, "A Design Flow for Application-Specific Networks on Chip with Guaranteed Performance to Accelerate SOC Design and Verification," in Proc. Design, Automation and Test in Europe(DATE), pp. 1182-1187, 2005
[10] L.-S. Peh and W. J. Dally, "A Delay Model for Router Microarchitectures," in IEEE Micro, vol. 21, no. 1, pp. 26-34, 2001.
[11] Xilinx Inc., "ZC706 PCIe Targeted Ref. Design (UG963)" Available: https://www.xilinx.com/support/documentation/boards_and_kits/zc706/2_014_4/ug963-zc706-pcie-trd-ug.pdf,2015.
[12] D. Seo, A. Ali, W. T. Lim, N. Rafique and M. Thottethodi, "Near-Optimal Worst-Case Throughput Routing for Two-Dimensional Mesh Networks," in Proc. of Int'l Symp. on Computer Architecture (ISCA), pp. 432-443, 2005.



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