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Timing and Control Signals Generator in Radar Application by Using Spartan 3e

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Abstract: ***This paper is to grant the architecture design and implementation of a software and hardware module appeal to Timing and Control Signal Generator (TCSG) for pulsed RADAR (Radio Detection and Ranging) application. Radar consists of scalar of sub-systems like Exciter, Receiver, Radar Controller, TCSG, Duplexer Antenna etc., and they are distributed. All these sub-systems are being guide, with phase coherence, with the support of Timing Control Signal Generator (TCSG). This phase coherency is executed by applying a sinusoidal clock signal to TCSG, which is being trace from the exciter unit. The Timing Control Signal Generator is to control the of the RADAR sub system by using Spartan-3E FPGA operation.***
Key words: Timing and control signal generator (TCSG), Ethernet phy, Spartan 3E FPGA

I. INTRODUCTION

A Radar system is a separate sensing implement usefulness to place the presence of an object and its direction of movement in atmosphere. The Radar system main target of this kind of Radar is the refractive index finger of the atmosphere. Radar consist in of number of sub-systems a like Exciter, Receiver, Radar Controller, TCSG, Duplexer Antenna etc..,. All these sub-systems are being controlled, with phase coherence, with the help of Timing Control Signal Generator (TCSG). This phase coherency is realized by devote a sinusoidal clock signal to TCSG, which is being trace from the exciter unit. The main performance of this Timing Control Signal Generator is to control the agency of the RADAR by synchronizing all the sub-system. The synchronization of all the sub-systems is completed by generating a pulse called 'Inter Pulse Period'. And all the control pulses need the Radar system i.e.., Exciter pulse, Transmit pulse, Gating pulse, Blanking pulse, T/R pulse etc., are generated with by the Inter pulse period. The fast-advancing region of software determines hardware enabled combinations of embedded system used by the exponential growth per-device resources in field-programmable gate array (FPGA) technology has made inroads into most electronic design system. The Spartan-3E of Field-Programmable Gate Arrays (FPGAs) is specifically sketch to meet the necessarily of high volume, cost-sensitive consumer electronic applications. New features improve system exploit and reduce the price of configuration.

II. SPARTAN-3E CONFIGURATION

Spartan-3E FPGAs are ideally suited to a broad range of consumer electronics applications, intercept broadband access, home networking, display, and digital television equipment. The Spartan-3E is a suzerain alternate to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibleness of conventional ASICs. FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs. The Timing and Control Signal Generator (TCSG) is developed on a single board Xilinx Spartan-3E based card with trans-receivers for electrical compatibility with external logic levels. There are four elements in total test setup

FPGA (Spartan-3E) Board.

Multi output calibrated Programmable Power Supply from Agilent to generate +5V DC, +3.3V DC and +2.5V DC.

A PC running GUI based control program to send/receive command string through Serial communication port (COM Port). This software is developed using Visual Basic 6

on MS-Windows XP platform.

Oscilloscope to measure and record the waveforms

Functional testing of the timing Control Signal Generator has been carried out by creating a VHDL programmable project with four instantiations of the TCSG modules. Instances are named as TCSG1-4. CD is clock divider block inserted for simulation purpose which generated timing reference clock. The design implementation of a module for generating

Certain specific control signals using the FPGA in the radar controller of the radar unit

III. TIMING AND CONTROL SIGNAL GENARATOR

Timing Signals can be generated using standard timer IPP triggering pulse. It will be used as reference to generate different timing and control signal. Considering beneficial of implementation and flexibleness for particular application, Timing and control Signal Generator (TCSG) is a module supported on Unified Timing and control Signal Generator are used to switch different RF switches. In both transmitting and receiving. The TCSG is application particular timing signal generator that meets timing requirements of pulsed RADAR (Radio Detection and Ranging). Each of the 133 TR modules in the out-door field consists of a Xilinx Spartan-3E based TCSG card for control, communication and monitoring purposes. Communicate radar controller and TR module through Ethernet. Electrical Ethernet is to communicate with in-door sub systems and optical Ethernet is to communicate with out -door TR modules.

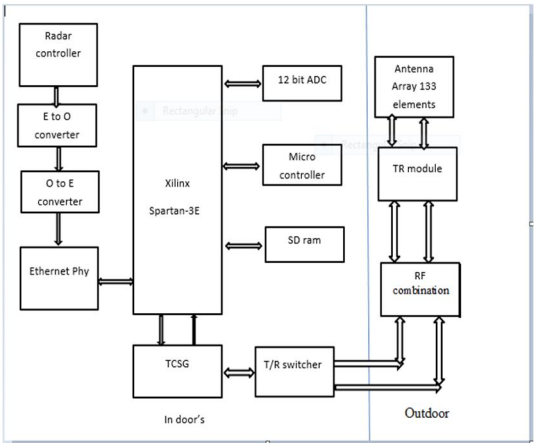

Fig1: Block diagram of TCSG

These Bock diagram shows in fig.1 how to communicate radar controller and TR module through Ethernet (KSZ8041TL) provides MII/RMII/SMII interfaces to transmit and receive data. HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables. Functional block diagram of Ethernet phy (KSZ 8041TL) is shown below. This basically contains the main control unit (MCU) and fiber transceiver unit (FTU). FTU translates the incoming optical domain (Ethernet TX, Ethernet Rx, IPP, and CLK) signals into electrical domain using optical receivers. MCU RC pre-loads the user specified experimental parameters in to the TR modules. Depending on the data received from the RC. The KSZ8041TL is a single 3.3V supply Fast Ethernet transceiver. On the media side, the KSZ8041TL protect 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable discovery of and correction for straighten-through and crossover cables. The KSZ8041TL offers a choice of MII, RMII, or SMII data interface connection to a MAC processor. The MII management bus option gives the MAC processor complete access to the KSZ8041TL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change. Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size. The KSZ8041FTL has all the identical rich features of the KSZ8041TL plus 100Base-FX fiber support.

IV. RADAR CONTROLLER

Radar comptroller (RC) and timing and control signal generator (TCSG) will toil together in coordination. The PC-supported RC Radar Controller executes the vocation fundamental performance. (i) RC concede the use to prepare the experimental parameters and beams need for function of the radar, through the GUI, (ii) Stores the calibration phase data and propagate phase correction file. Generates the phase data request for each TR module for the beams selected, (iii) Pre-loads the experimental parameters and phase data into the TR modules through the Optical Ethernet Switching Network, (iv) Reads the status data from the TR modules during action and exhibit the status data through the GUI, and (v) Sends the experimental parameters to Digital Receiver through Ethernet

switch before starting the radar action and communicates during the function

Fig2: Photograph of the TCSG card

V. OPTICAL DISTRIBUTIONNETWORK

Since the out-door TR modules and the RC are separated by 140 m, intercommunication and control of TR modules is carried out through Optical dispensation network is employed to interface the 133 TR modules with RC and TCSG. ODN subsist of (i) optical Ethernet intercommunication switching network, (ii) signal distribution network.

Fig3:Optical distribution for timing and control signals

TR module necessarily to communicate with the RC through Ethernet. Each TR module necessarily 16-MHz CLK and IPP trigger pulse from the TCSG. The show in above in this figer3 optical distribution for timing and control signals Optical fibers are used to carry the Ethernet-Tx, Ethernet-Rx, IPP and CLK signals from the in-door RC/TCSG to out-door TR modules. Optical fibers are also used to carry two additional RF signals, Cal-Tx and Cal-Rx, between the radar receiver and TR modules. Signal disposition network dispense the centrally (performance scope) generated IPP and clock signals to all the TR-modules in the antenna field. Distribution is carried out in two-levels; (i) one centralized 7-way distribution and (ii) seven numbers of sub-array level (19-way) distribution. The IPP and 16-MHz CLK signal generated by the TCSG are first distributed in the electric domain and then converted into optical signals using optical transmitters. These optical signals are routed to the respective TR modules through Fiber Optic cable.

VI. DISTRIBUTED TIMING AND CONTROL SIGNAL GENERATOR

Each of the 133 TR modules in the out-door field consists of a Xilinx Spartan-3E supported DTCSG (Distributed timing and control signal generator) card for control, intercommunication and supervise purposes. Which basically contains the main control unit (MCU) and fiber transceiver unit (FTU) transfer the income optical dominion (Ethernet TX, Ethernet Rx, IPP, and Clock) signals

into electrical domain using optical receivers. Show in bellow in this fig5 fiber transmitter unit MCU is the CPU for the system with FPGA Spartan-3E, micro controller, DDR, ADCs and other circuitry for supervise and controlling. RC pre-loads the use specified experimental parameters in to the TR modules. Depending on the data take from the RC, MCU generates all the timing and control signals to different switches, 6-bit phase shifter, and 5-bit attenuator of the TR module in synchronization with IPP accept from MTCSG. Phase and amplitude SDRAM with 64 Mbytes that is used for program execution; it is accessed by Micro Blaze using Multi-Port Memory Controller.

Fig4: Fiber trasmitter unit

VII. TR MODULES

Accuratephase monitoring of the TR modules is very cruciform for ordinary transformation of any phased order radar. Differential phase errors (proceed over the period) of the TR modules (both in TX and Rx) must be moderated and accurate from period to period for particular beam shaping. Figure-10 reveals the diagram within the TR model to monitor the phase in both TX and Rx paths. During the TX method, The TX-RF indication at forward conjugate port of the directional coupler is reborn in to an optical signal by using optical transmitter. This signal is sent to the restraint room through the optical fiber network and reborn back to the RF signal by using optical receptor. The TR model will be selected using the RF switching network in the performance room. The phase of this signal is moderated with the relation to the TX vibration at the exciter. In the allow method a frequent-change simulated vibration from Exciter unit is routed to an RF switching network, reborn into optical field by optical transmitter, routed to the selected TR model. This signal is converted back to the RF signal by using optical receptor placed in FTU and fed to the accept division of the TR model through bi-directional coupler. The signal then come through the whole radar allow path. The phase of this indication is measured with respect to the pretended vibration. Once the phases of all the TR modules are moderated, RC calculate the discriminating phase-errors and provide the lively phase rectification list.

A. Implementation

In this paper utilizing proposed strategy FPGA utilized as a part of Xilinx Spartan3E. These method is utilized to develop the delicate center processor framework .It is made out of the equipment part and programming part. The equipment part is portrayed in Microprocessor Hardware Specification (MHS) record and exchanged to a bit document utilizing ISE outline flow(design passage ,union, execution ,confirmation, gadget programming) .The product part is depicted in microcontroller programming detail (MSS) record and moved into ELF document through programming era steps. The bit document can be arranged on FPGA through JTAG.

B. Timing Pulses Generating Using Spartan 3E

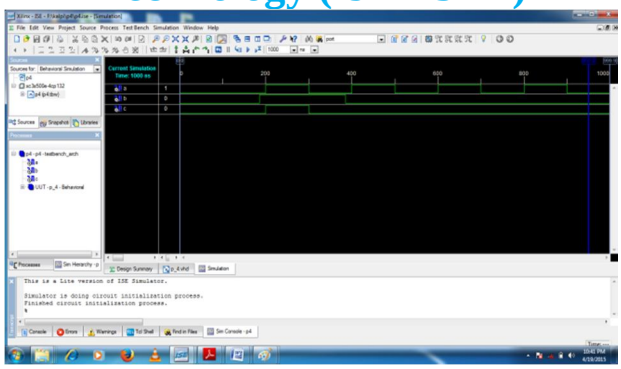

Fig 5: Spartan 3E

All these control pulses required for the Radar system. Transmit pulses are generated with respect to this Inter pulse period. The output pulse is generated for 100 ns.

VIII. CONCLUTION

The timing pulses are generated with different time periods are simulated and configured on FPGA of Spartan3E.Which presents flexible, easy and trustable methodology. The configured system can be programmed to act according to the target of the system.

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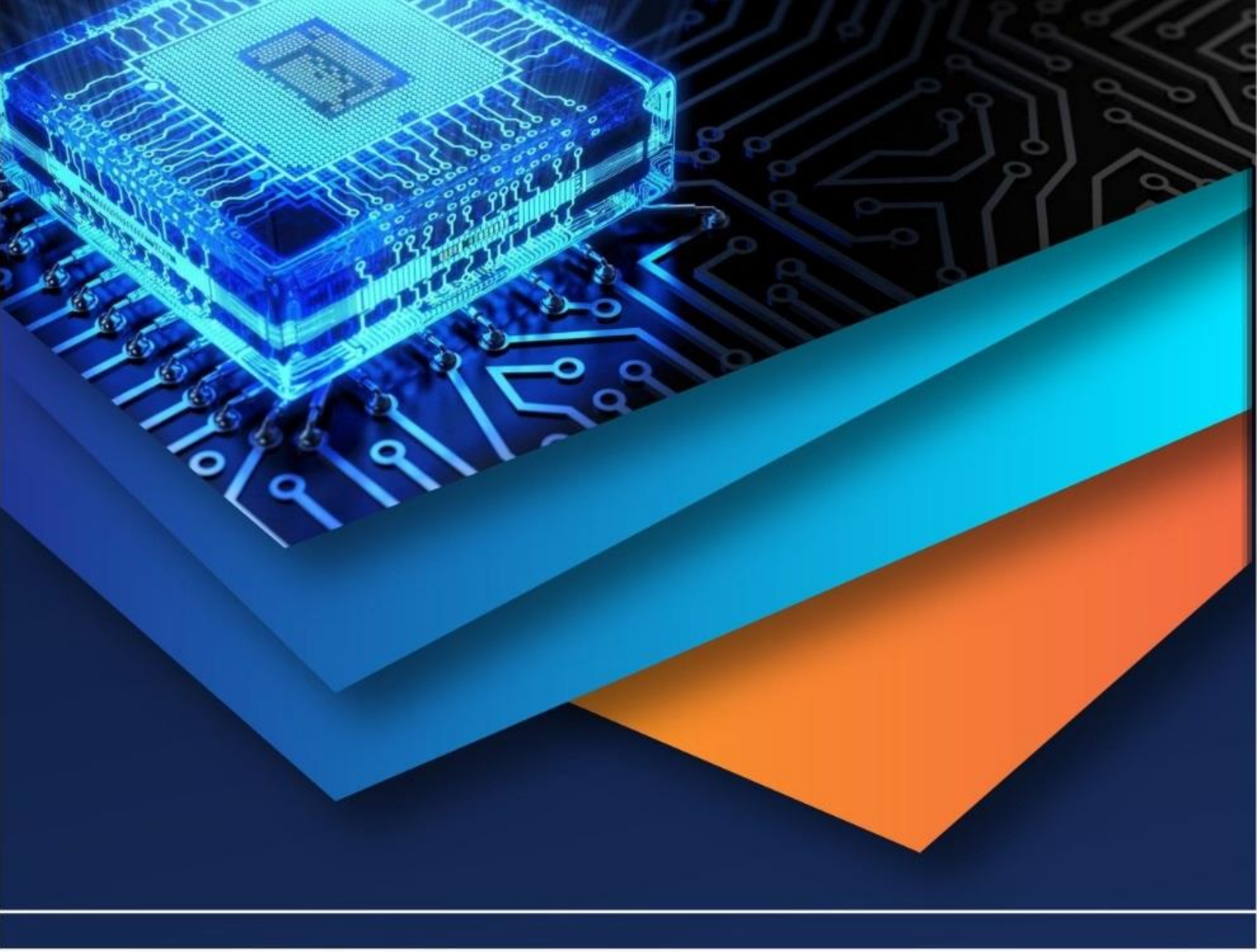

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