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Design of High Speed & Power Optimized Sense Amplifier using Deep Nano CMOS VLSI Technology

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***Abstract:** In this paper we have designed Faster & Power Efficient Sense Amplifier for CMOS SRAM using VLSI Technology i.e. primarily schematic of sense amplifier is designed & simulated using ADS (Advanced Design System). The sense amplifier then implemented & analyse at chip level Microwind 3.1- a layout editor. The 45 nm & 32 nm technologies are used to analyze performance of Sense Amplifier. Our focus will be to reduce the size, to improve the power consumption and also improve the response time of sense amplifier.*
***Keywords:** CMOS SRAM, Sense Amplifier, Microwind, ADS, layout. Etc.*

I. INTRODUCTION

CMOS technology scaling will be a main drive force of the electronics industry in this era and also provided a path toward both faster and denser integration. The CMOS transistors manufactured today are 20 times faster and occupy very less area than those built 20 years ago. The number of components per chip and the system performance is improving exponentially over the last two decades. As the length of channel is reduced, the performance of the transistor improves, the power per switching event decreases, and the density improves Oxide thickness, transistor length (Lg) and transistor width (W) were scaled by a constant factor (1/k) in order to provide a delay improvement of 1/k at constant power density. As a consequence of continued density scaling, features are moving ever closer to fundamental dimensions This paper presents the same scaling effects of technologies i.e. 45nm & 32nm using.

The layout of sense amplifier being analyzed & it proves the scaling impact on CMOS devices i.e. the size of the sense amplifier decreases, as the density of transistor increases the power consumption increases at chip level, The Access time also decreases i.e. speed of the sense amplifier increases &as the time decreases, the frequency increases.

A. Sense Amplifier

A sense amplifier is part of the read circuitry which is used when data is required to be read from the memory; The main role of sense amplifier is to sense the low power signals from a bitline i.e. 1 or 0 stored in a memory cell, and also amplify the small voltage to required logic levels so the data can be interpreted properly by logic outside the memory There are two main categories of sense amplifiers Differential sense amplifiers, also known as voltage mode sense amplifiers, and non differential amplifiers, also known as current modesense amplifiers.

The differential sense amplifier is commonly used because there is no static current flow after the amplifier latches, which will cause reduction in power. Also, it is simple and reliable The circuit shown in Fig. 1 is the sense amplifier used to read data from the cell.

The amplifier is composed of a differential pair (Transistors M1 and M2) with an active current mirror load (M3 and M4) and a biasing current source (M5). As soon as the SE signal goes HIGH, the sense amplifier senses the appropriate difference between the BIT and BIT voltages and produces an output voltage. The access time of the memory, which is defined as the time the initiation of read operation and the output, initiation of the read operation and the output, mainly dependent on the performance of the sense amplifier? So the design of the sense amplifier is the main criteria for the design of memories Advanced Design System is the leading electronic design automation software in the world for RF, microwave, and high speed digital applications.

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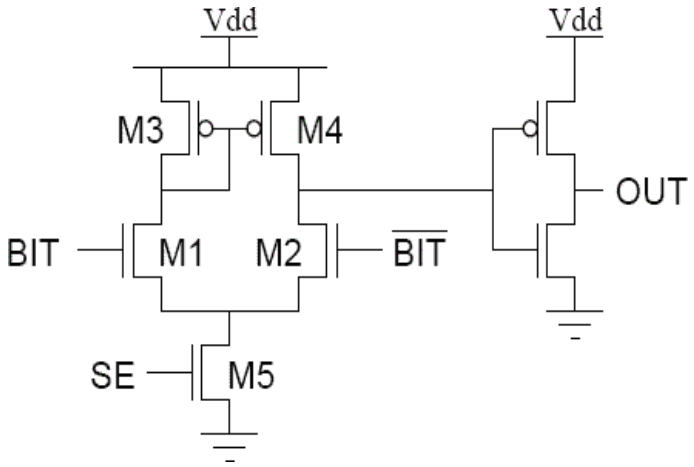

Fig. 1-The sense amplifier

B. Microwind Software

Microwind is integrated EDA tool encompassing IC for designs from concept to completion, enables chip designerto design beyond their imagine. MICROWIND in integrates traditionally separated back-end and front-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. The 45 nm technology invented in 2007 & it has effective Gate length of 30 nm whereas The 32 nm technology invented in 2009 & it has effective Gate length of 27 nm Compared to 45- nm technology, the technology offers 30% increase in switching performance, 30% less power consumption, double higher density, two times reduction of the leakage between source and drain and through the gate oxide. At each lithography scaling, the linear dimensions are approximately reduced by a factor of

0.7, and the areas are reduced by factor of 2. Smaller cell sizes lead to higher integration density which has risen to per mm2 in 45 nm & 32 nm technology respectively.

Key Benefits of ADS

1) Application-specific-Design promotes years of expertise in an easy-to-use interface.

2) ADS is supported exclusively or months earlier than others by leading industry and foundry partner.

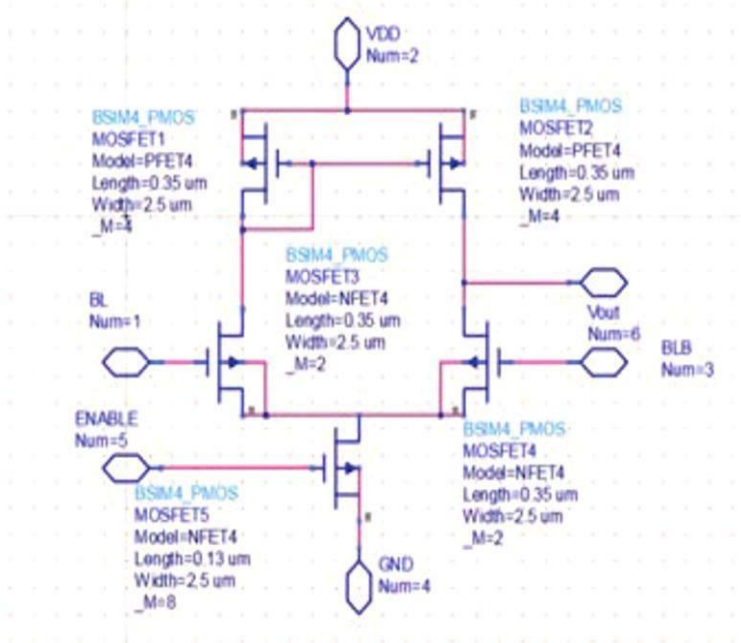

Fig. 2-The circuit diagram of sense amplifier designed in ADS

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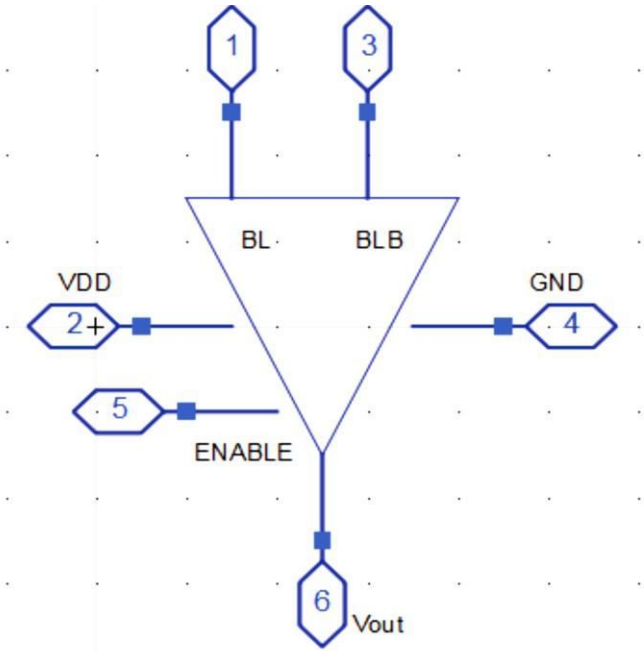

Fig.3- Symbol

C. Implementation Using ADS

The Fig. 2 shows the circuit diagram of sense amplifier designed in ADS. To ensure that the current is divided equally, the PMOS devices M3 and M4 must be sized identically. The NMOS devices M1 and M2 must also be sized identically.Hence width of PMOS devices M3 & M4 have been selected of about 2.5 um and multiplication factor (M) is 4 to have width of 10.0 um 0.35 um. Likewise, both the NMOS M1 & M2 also have identical sizing i.e. width of about 2.5 um and multiplication factor (M) is 2 to have width of 5.0 um & length 0.35 um. A biasing current source (M5) has width 20.0 um & length 0.13 um. The Fig. 3 shows the symbol of Sense Amplifier.This symbol has all internal components shown in Fig. 2. We can easily use this symbol for the simulation of Sense Amplifier directly or this symbol can be used in SRAM design for reading the data as well. The Fig. 4 shows the simulation results in ADS. It shows the waveform of BL, BLB, Vout& ~Vout (i.e. output of an Inverter). The BL & BLB input voltages are exactly opposite to each other i.e 1800 phase shift. The sense amplifier senses the difference between these voltages & produces an output voltage (Vout). From the graph it is observed that the output voltage waveform of sense amplifier shown in green color has less amplitude i.e. 1 v than required level i.e. 1.2 v.

D. Impementation using Microwind 3.1

The Fig.5 shows.The Layout of Differential Voltage Sense Amplifier designed using Microwind software. The circuit diagram for this layout shown in Fig. 1. Now, The Layout has two PMOS (M3, M4) connected back to back, the drain & source are shown in blue & the N- well of PMOS shown in dotted green which is connected to Vdd. The source of both PMOS is connected to Vdd. Gate of both PMOS's is made up of Polysilicon (Red) & those are connected to each other & then to drain-drain connection of PMOS (M3) & NMOS (M1) as well by Poly –Metal connector. The layout of two NMOS (M1 & M2) is also connected back to back. channel length between drain & source of every transistor is being reduced i.e. speed of the sense amplifier increases & Now, As the time decreases,the frequency increases by 400%. both NMOS is connected to drain of both PMOS which is shown in blue color i.e. Metal . Input BL & BLB is given to gate i.e polysilicon (red) of M1 & M2 respectively. Now the source of NMOS is connected to each other & then connected to drain of NMOS (M5) i.e biasing current source. The source of M5 then connected to ground. The ENABLE i.e Vdd signal is given to gate of M5.The Layout of sense amplifier is ready for simulation. But to increase the voltage level of sense amplifier, an Inverter is connected at the output. Hence layout also has one more PMOS & NMOS structure. The gate & drain of both the transistor are connected to each other shown in red & blue color respectively. The source & N- well of PMOS is connected to Vdd. &The source of NMOS is connected to ground. The output of sense amplifier Vout is connected to input of an Inverter.

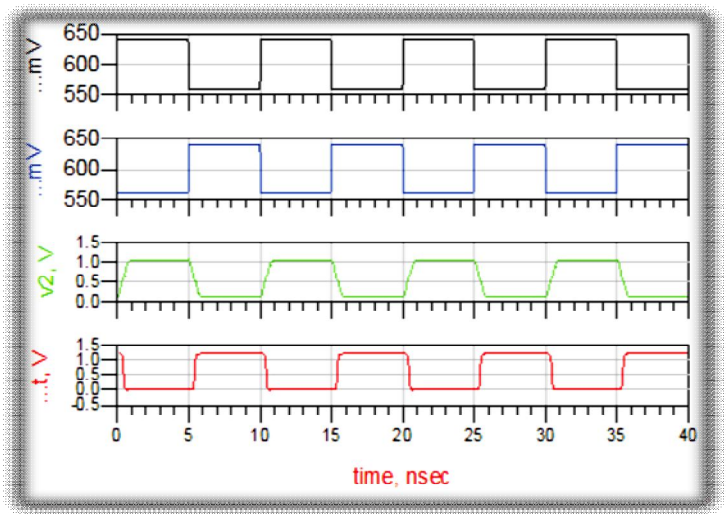

Fig.4- simulation result

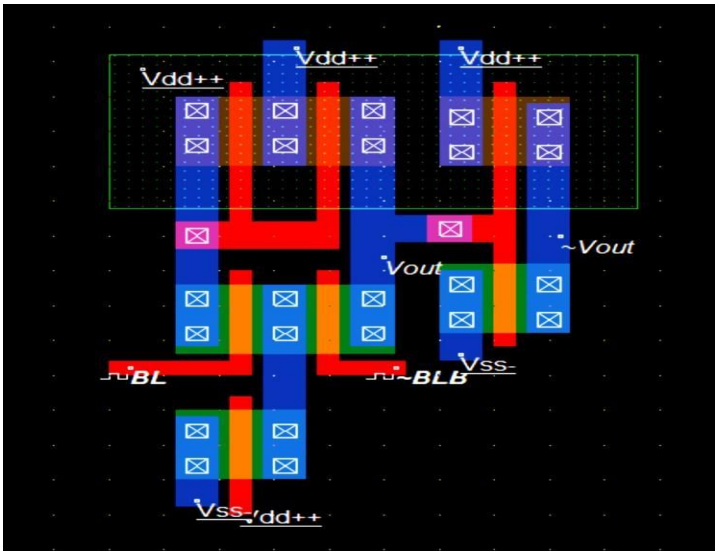

Fig.5-Layout Design

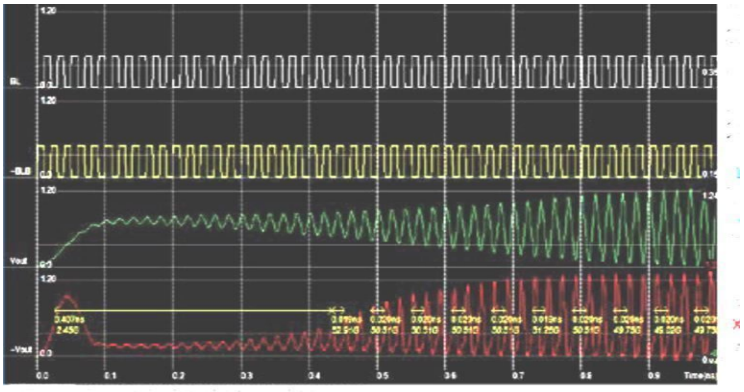

Fig. 7 Simulation results in 32 nm technology

The output voltage of an Inverter is ~Vout This Layout is implemented in both technology i.e. 45nm & 32 nm to analyze the scaling effect. In 45nm the dimension of layout achieved are 1.20 µm * 1.70 µm & In case of 32 nm technology.

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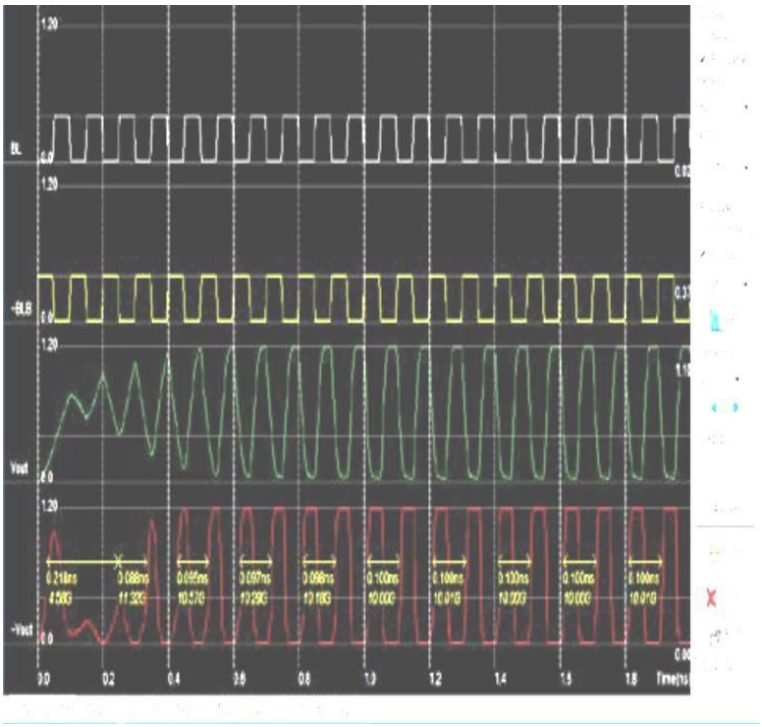


Fig. 6 Simulation results in 45 nm technology

The Fig.6 shows the simulation results of sense amplifier in45 nm technology. It shows the input of sense amplifier i.e.BL(white) & BLB(Yellow), the output voltage of sense amplifier in green & the output of an Inverter in Red. The gain of an Inverter is very high hence it is connected across the output of sense amplifier to increase the level of output voltage.The Fig. 7 shows the simulation results of sense amplifier in 32 nm technology. It also shows BL, BLB, Vout& ~Vout . The Fig. 8 shows the three dimensional view of layout of sense amplifier with an Inverter. It shows all the processes i.e. from initial substrate to passivation etching to be carried out on silicon wafer to design I.C. of sense amplifier.The Table 1 shows the comparative analysis of sense amplifier layout implementation in 45 nm & 32 nm technology. It presents as technology scales down i.e.
45 nm to32 nm. The size of the layout of sense amplifier decreases by40% i.e. transistor density increases on same space. The power consumption increases by 18 % because number of transistors are more on less space to consume more power. The Access360time also decreases by 75 % .

Table I
Comparative Analysis Of Two Technologies

Sr.no	Parameter	45nm	32nm	Percent.
1	Size	2.04µm2	1.228	40%
2	Power Consumption	0.083 mW	0.104 mW	18%
3	Access Time	0.095 ns	0.020 Ns	75%
4	Frequency	10 GHz	50	400%

II. CONCLUSION

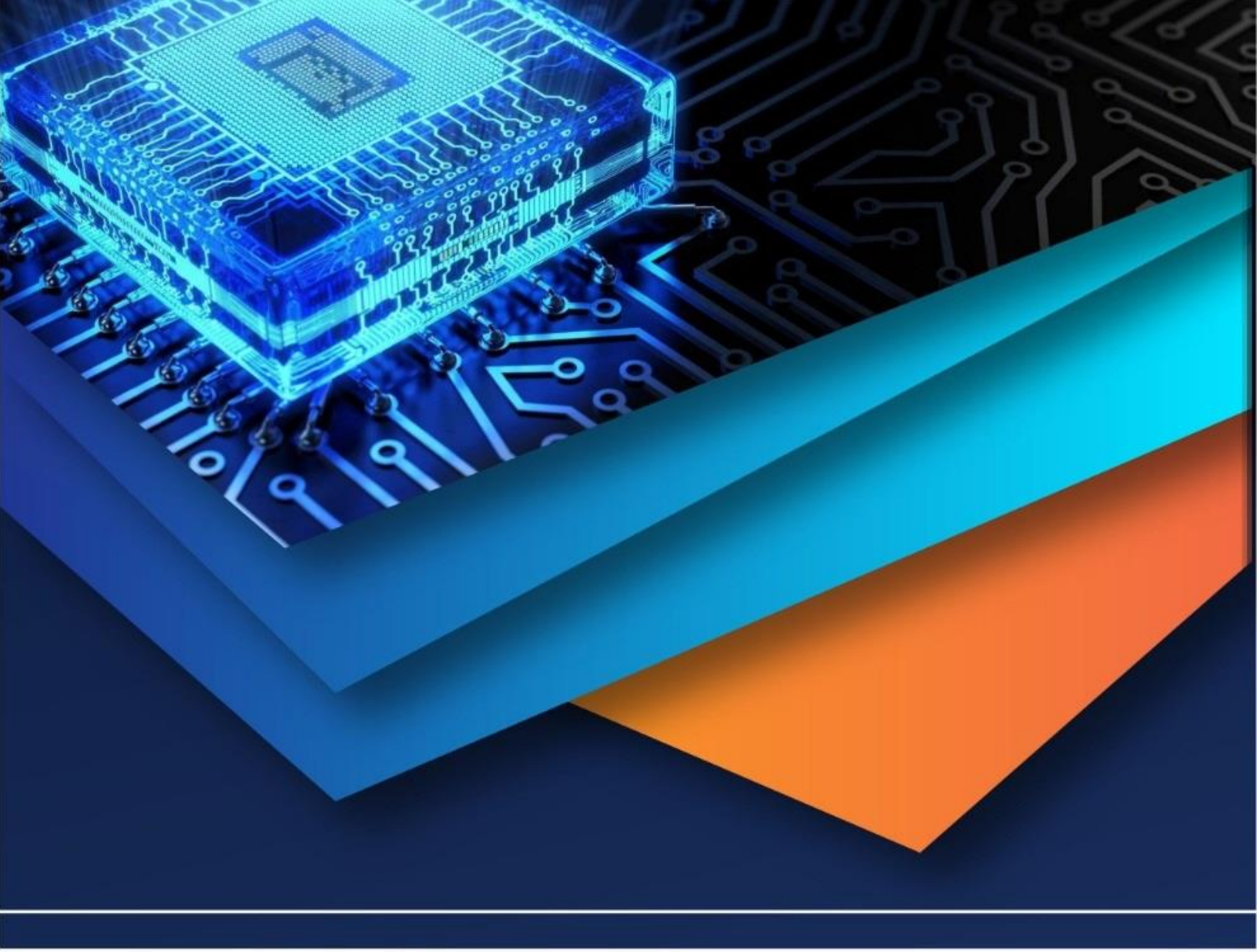
The proposed Sense Amplifier has been designed in standard 180 nm technology. The design of proposed sense amplifier has been done on the basis of the characteristics of various sense amplifiers. The latch type sense amplifier has been found to be most efficient sense amplifier among these. The performance of latch sense amplifier has been further enhanced by isolating its input by inserting the pass transistors. This type of sense amplifier can be used in the SRAM for achieving high speed with low power.

This sense amplifier circuit achieves a nominal value of sensing delay of 0.15 ns and average power of 0.2 mW, for the bitline capacitance of 1 pF and supply voltage of 1.8 V. These simulated results indicate that the designed sense amplifier has been 40% faster than latch type sense amplifier without any if increment in power consumption. The designed sense amplifier has been compared with the existing sense amplifiers. Here a lot of improvements have been observed in sensing delay with respect to variation in bitline capacitance or powersupply.This Paper has illustrated improvement in the performance ofthe Sense Amplifier for CMOS SRAM. The circuit is designed & simulated in the ADS (Advanced Design System). The simulation result shows that the required output voltage i.e. 1.2V is available after addition of an Inverter at the output & having identical transistors i.e. PMOS & NMOS in the circuit. This circuit is implemented at Layout level using MICROWIND 3.1 software. In this software 45 nm & 32 nm technologies are used to design Layout & simulation results are analyzed with the impact on size i.e reduced by 40%, Power Consumption is reduced at cell level Access Time is reduced by 75 % i.e. speed increases and Frequency is also increases by 400%. Hence, It is observed that the performance of the sense amplifier has been improved drastically. It also proves that the technology scaling will have huge impact on transist or performance. To have better results now our future work will concern the 22-nm technology.

Future Scope- In case of sense amplifier the small difference between the bit lines is amplified to the full digital level. So there may be a chance of false switching of output due to small offset voltage at the input. By employing offset compensation techniques this problem can be overcome. Also by using low power and high speed logic techniques such as Multi Threshold CMOS (MTCMOS) and Variable threshold CMOS (VTCMOS) the power dissipation can be further reduced and the speed of circuit can be further enhanced.

REFERENCES

[1] E.Sccvinck, P. J. van Beers, and H. Ontrop, “Current- Mode Techniques for High- Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAMs,”IEEE Journal of Solid-State Circuits vol.26 No.4 pp.525-536 April1991.
[2] Chrisanthopoulos,Y.Moisiadis,Y.Tsiatouhas,A.Arapo yanni “Comparative study of different current mode sense amplifiers in submicron CMOS technology”, IEE Proc.-Circuits Devices Syst., vol. 149, No.3, June2002.
[3] Chun-Lung Hsu and Mean-HomHo “High Speed Sense Amplifier for SRAM applications” IEEE Asia- Pacific conference on circuits and systems pp 577- 580 december-6-9,2004.
[4] Anh Tuan Do, Jeremy Low Yung Shern, ZhiHui Kong, Kiat Seng Yeo and Josuha Low Lih ,“A full current mode sense amplifier for low power Sram applications” IEEE division of Circuit and System- 2008.
[5] Dotuan,Kong-ZhiHui,YeoKiatSeng,”Hybrid,mode SRAM sense amplifiers new approach on transistor sizing” IEEE transactions on circuits and systems vol. 55, no.10 october2008.
[6] Anh-Tuan Do, Zhi-Hui Kong, Kiat-Seng Yeo, and Jeremy Yung Shern Low “Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM” IEEE VLSI Systems, vol. 19, no. 2, Feb2011.
[7] Pathrikar, A. K., and R. S. Deshpande . "Design of faster & power efficient sense amplifier using VLSI technology." 2016 IEEE International Conference on Advances in Electronics, Communication and Computer Technology (ICAECCT). IEEE, 2016.
[8] Jota Hooda, Sarita Ola, Manisha Saini, “Design and Analysis of a lowPower CMOS Sense Amplifier for Memory Application”, International Journal of Innovative Technology and Exploring Engineering ISSN:2278-3075, Volume-2, Issue-5, April 2013,pp 271-279
[9] B. Mohammad, P. Dadabhoy , K.Lin, and P. Bassett, “Comparative Study of Current Mode and Voltage Mode Sense Amplifier Used for 28nm SRAM”,in Microelectronics (ICM), 2012,24th International Conference on, Dec 2012, pp. 1-6.
[10] Key sight Technologies,” Key sight EEs of EDA Advanced Design System” The Industry’s Leading RF,Microwave and High-Speed Design Platform, Published in USA, December 30, 2014 5988-3326EN.
[11] Etienne-SICARD,Syed-Mahfuzul aziz,“introduction micriwind3.1”,MICROWIND APPLICATION and 27/06/07, pp1-16.[9] Etienne SICARD, Syed Mahfuzul Aziz,” Introducing 32 nm technolog in Microwind3”, The MICROWIND APPLICATION NOTE, 10/07/10, pp1-24.[10]
[12] Etienne Sicard ,“MICROWIND & DSCH V3.5 lite user’s Manual” ,September 2009. Chandrakasan, B.Nikolic,“Digital Integrated Circuits, A Design Perspective”, 2nd ed., ser. Prentice Hall Electronics and VLSI Series, C. G. Sodini, Ed.Pearson, 2003
[13] EtienneSICARD,Syed Mahfuzul Aziz,” Introducing 45nm technology in Microwind3”, MICROWIND APPLICATION NOTE, 27/06/07, pp1- 16.
[14] SICARD, Syed Mahfuzul Aziz,” Introducing 32 nm Microwind3.1”,technology,MICROWINDAPPLIC ATION NOTE, 10/07/10, pp1-24



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