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Effect of Doping Concentration on Electrical Parameter of Tri-Gate Junctionless N-channel FinFET

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Abstract: ***Now days, Nano scale devices are in demand due to their higher packing density and high performance in microelectronics circuits. Tri-gate Junctionless N-channel FinFET provides better performance at nano scale regime. This paper analyzes the effects of channel doping concentration on electrical parameter of Tri-gate Junctionless N-channel FinFET. Different important device electrical parameter such as ON current, OFF current, I_{ON}/I_{OFF}, Threshold voltage, Subthreshold slope, DIBL.***
Results show that as the channel doping concentration of the Tri-gate Junctionless N-channel FinFET the threshold voltage (V_{TH}) decreases.
Besides, the drain-induced barrier lowering and the subthreshold swing of the Tri-gate Junctionless N-channel FinFET become larger as the channel doping increases.
We also found that as the channel doping increases, the off-current (I_{OFF}) increases and the on-current (I_{ON}) actually decreases due to the doping-dependent mobility degradation. The conduction mechanisms under different channel doping concentrations were also investigated by TCAD simulation.
Results show that for short channel devices the better performance is obtained with smaller channel doping concentration with higher I_{ON}/I_{OFF} and smaller values of Subthreshold slope, DIBL.
Keywords: Junction less FinFET, Visual TCAD, 22 nm Technology, DIBL, Subthreshold slope.

I. INTRODUCTION

Conventional planar CMOS transistors on bulk silicon substrate have been a key component in ultra- large-scale integration technology for the past four decades, but are approaching the fundamental physical limits imposed by short-channel-effects (SCEs) and gate oxide tunnelling. FinFET have been proposed as an alternative to planar devices mainly because of their robust electrostatic control.

However, FinFETs too face technological challenges in super-steep doping profile requirement and high thermal budget for sub- 20 nm channel length era along with excessive short channel effects. Junctionless FinFET, which do not have any pn junction in the source-channel-drain path can be scaled to lower channel lengths because of lower SCEs and easy fabrication steps. It has homogeneous and uniform doping throughout the source-channel-drain region unlike a junction based (JB) inversion mode (IM) transistor.

A Junctionless FinFET demands high channel doping concentration (~10^{19} cm^{-3}) in the channel region to achieve an acceptable threshold voltage. Despite its high doping concentration, Junctionless FinFET has comparable drain current as Junction based FinFET.

Therefore, Junctionless FinFET can be a prospective candidate for replacement to conventional FinFETs in ultra short channel length regime. Junctionless FinFET has same doping concentration at source, channel and drain regions. Thus, the structure of a Junctionless FinFET is $N^+ – N^+ – N^+$ for n-channel and $P^+ –P^+ –P^+$ for p-channel in the source-channel-drain region. Because of uniform and homogeneous doping in the channel region, a Junctionless FinFET eliminates the subsequent annealing process and the device can be fabricated with shorter channel lengths. In addition, Junctionless FinFETs offer low standby power operation and low gate induced drain leakage. Also, lesser fabrication steps reduce process cost significantly compared to junction based devices of similar dimension. Junctionless FinFETs exhibit lesser random telegraph-noise and 1/f noise. Junctionless FinFET has fully CMOS compatibility.

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II. METHODOLOGY

1) *Device structure and simulation:* Fig.1 shows 2D cross-sectional view of Tri-gate Junctionless N-channel FinFET, Fig.2 shows Schematic view of Tri-gate Junctionless N-channel FinFET. And To study the effect of the channel doping concentration on Tri-gate Junction less 22nm N- channel FinFET all the simulation are done on Visual TCAD software using Genius simulator.

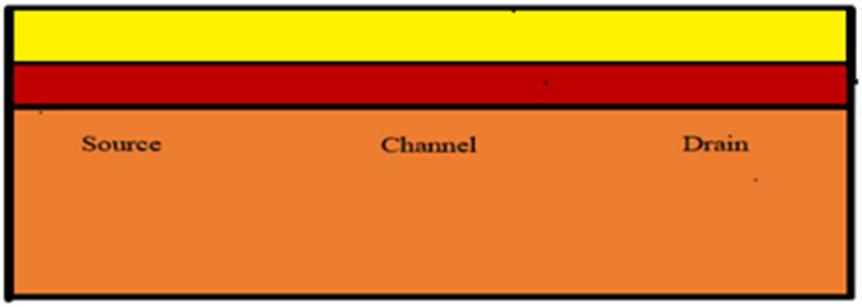

Fig.1: 2D cross-sectional view of Proposed Device

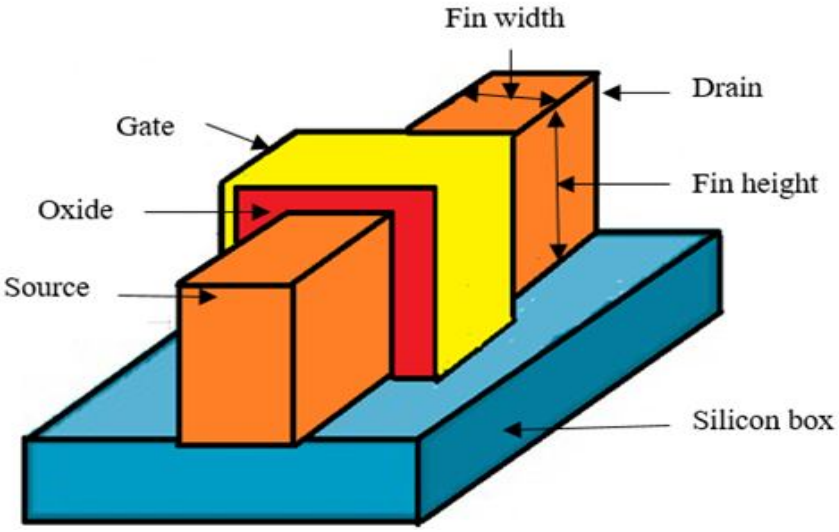

Fig.2: Schematic view of Proposed Device

Junctionless FinFET, which does not have pn junction in the source-channel- drain path. It consists of a thin semiconductor film deposited in a thin insulator layer, itself deposited in a metal electrode (gate). Thus, it does not have a junction; rather it is a simple "resistor". It is also called "gated trans-resistor". Commonly, a Junctionless FinFET has same doping concentration at source, channel and drain regions. Thus, the structure of a is $N^+ - N^+ - N^+$ for n-channel and $P^+ - P^+ - P^+$ for p-channel in the source-channel-drain region. P^+ and N^+ polysilicon gates are used for n and p channel Junctionless FinFET respectively (N^+/ P^+ denote highly doped with N/P-type dopants respectively).

Table: (a) Structure parameters of Tri-gate Junctionless N-channel 22nm FinFET

S. No	Parameter	Dimension
1.	Gate length	22nm
2.	Fin Height	15nm
3.	Fin Width	5nm
4.	Oxide Thickness	1nm
5.	Source & Drain Doping	1E19/cm^3
6.	Channel Doping	1E17 to 1E20/cm^3
7.	Workfunction	5.2eV
8.	Gate oxide material	SiO_2

2) Electrical parameters of FinFET:

a) Threshold Voltage: It is the minimum gate to source voltage at which channel create between drain and source. It is define as the constant current threshold voltage. Threshold voltage is the gate to source voltage required to produce a drain current of 10E-7* Effective Width of Channel / Length of the gate.

$$\text{Effective Width of Channel} = 2H_{FIN} + W_{FIN} \quad \text{.....(1)}$$

Where, H_{FIN} = Height of FIN

W_{FIN} = Width of FIN

b) Subthreshold Slope: It is define as the variation in gate voltage that has caused one decade increase in drain current.

$$SS = \frac{\partial V_{GS}}{\partial \log_{10} I_{DS}} \quad \text{.....(2)}$$

Where, V_{GS} = Gate to Source Voltage

I_{DS} = Drain to Source Current

c) DIBL: In Ideal MOSFET drain current is controlled by gate but when the length of channel scale down, drain current is decreased by increasing drain voltage and this effect is commonly called DIBL.

$$DIBL = \frac{\partial V_{TH}}{\partial V_{DS}} \quad \text{.....(3)}$$

Where, V_{DS} = Drain to Source Voltage

V_{TH} = Threshold Voltage

III. RESULTS AND DISCUSSION

The results obtained are as discussed below :

A. I_{DS} — V_{GS} Transfer Characteristics for different channel doping concentration

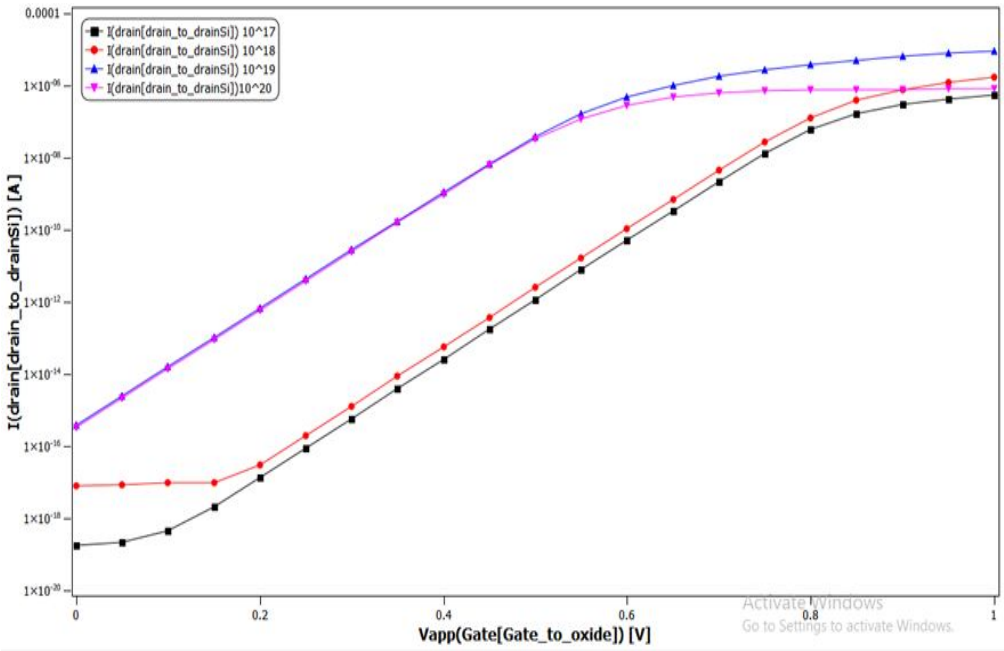

Fig.: 3 I_{DS} — V_{GS} Transfer Characteristics for varying channel doping concentration (1E17 to 1E20/cm^3)

I_{DS} — V_{GS} Transfer Characteristics for varying channel doping concentration (1E17 to 1E20/cm^3) and source & drain doping (10^19 /cm3) at V_D = 1V and V_{GS} ranging from 0 to 1V. From the I_{DS} — V_{GS} Transfer Characteristics as shown in Fig.3. We observed that as the channel doping concentration increases, the device turns ON at a lower gate voltage.

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B. Effect of Doping concentration on Leakage current

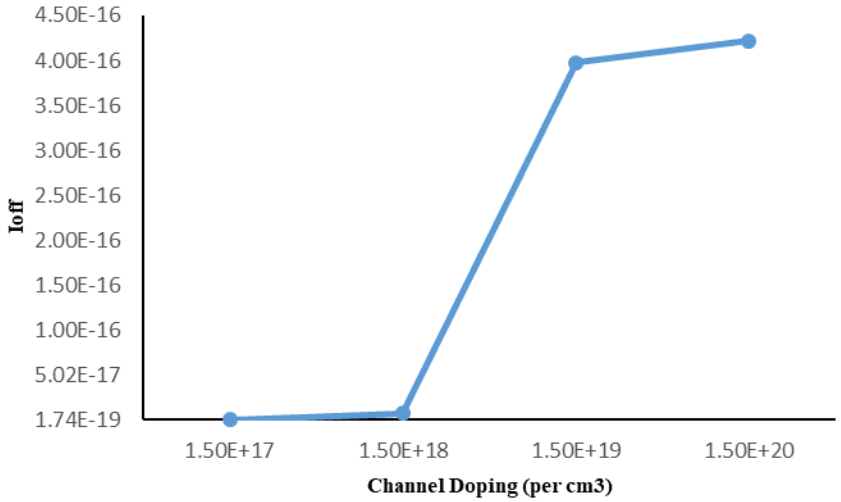

Fig.4: I_{OFF} of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E20/cm^3)

I_{OFF} of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E20/cm^3) and source & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.4. I_{OFF} increases with increasing channel doping concentration. On increasing the channel doping concentration, inversion charge carrier density increases, this leads to increment in I_{OFF} current.

C. Effect of Doping concentration on Drive Current

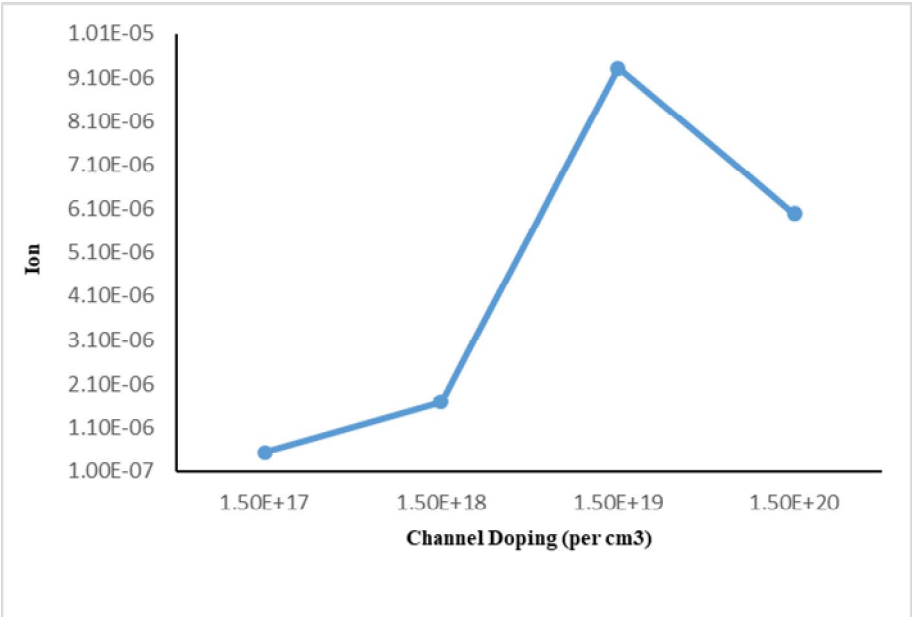

Fig.5: I_{ON} of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E20/cm^3)

I_{ON} of Junctionless N-channel FinFET Proposed device for varying channel doping concentration (1E17 to 1E20/cm^3) and source & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.5. As the channel doping concentration increases, the ON current of the Junction less N-channel FinFET tends to decreases. For the Junction less N-channel FinFET with higher channel doping concentration, although the electron density is higher, the electron mobility is lower. Since the mobility degrades as the channel doping concentration increases, the Junctionless N-channel FinFET with higher channel doping concentration has lower mobility and thus lower ON current by integrating the current density.

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D. Effect of Doping concentration on I_{ON}/I_{OFF} ratio

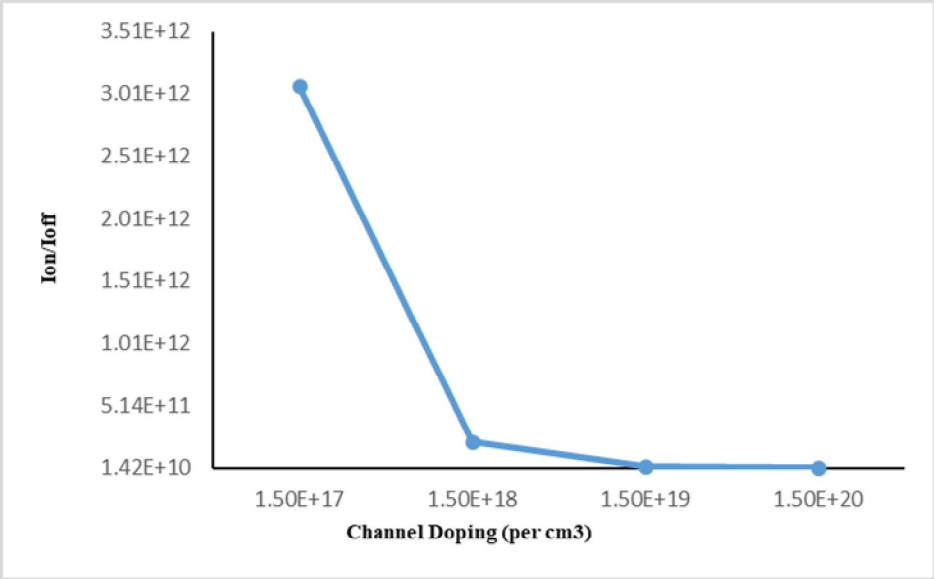

Fig.6: I_{ON}/I_{OFF} of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E20/cm^3)

I_{ON}/I_{OFF} of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E20/cm^3) and source & drain doping (10^19 /cm3) at VDS = 1V and VGS ranging from 0 to 1V shown in Fig.6. I_{ON}/I_{OFF} decreases with increasing channel doping concentration.

E. Effect of Doping Concentration on Threshold Voltage

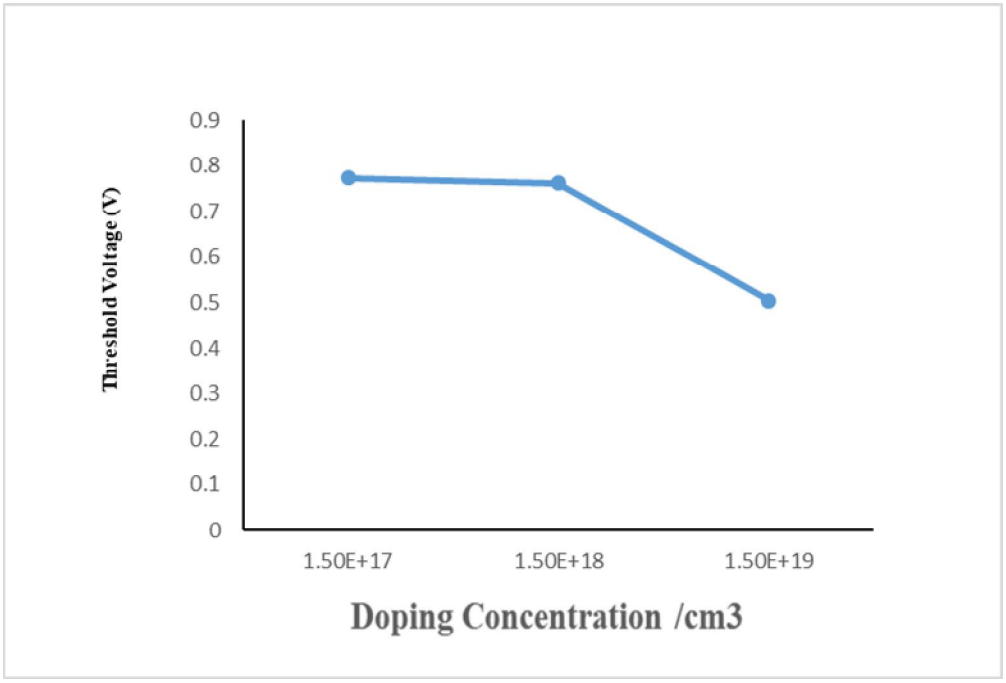

Fig.7: Threshold voltage of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E19/cm^3)

Threshold voltage of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E19/cm^3) and source & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.7. The threshold voltage of N-channel Junctionless FinFET decreases as the channel doping concentration increases.

F. Effect of Doping concentration on Subthreshold Slope

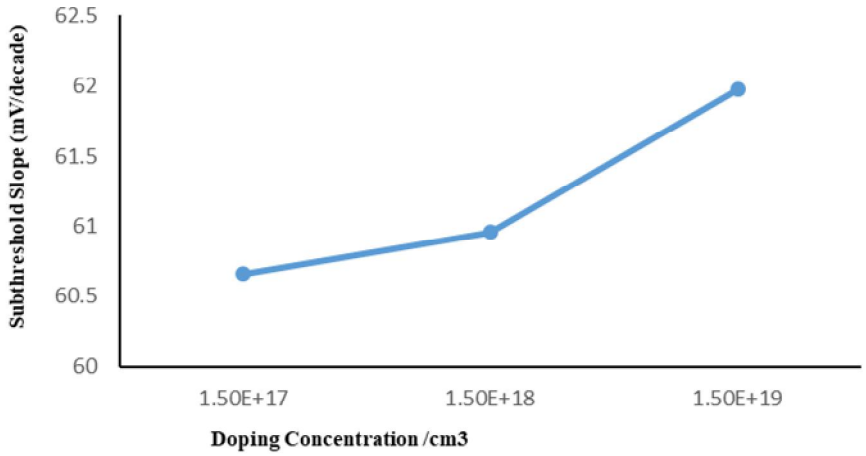

Fig.8: Subthreshold slope of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E19/cm^3)

Subthreshold slope of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E19/cm^3) and source & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.8. The subthreshold slope of N-channel junctionless FinFET becomes larger as the channel doping concentration increases. The electron density distribution is more uniform under lower channel doping. That means the average distance between conducting carriers and gate is longer for higher channel doping device. Consequently, the N-channel Junctionless FinFET with lower channel doping concentration passes better gate controllability on conducting carriers and hence better Subthreshold Slope.

G. Effect of Doping concentration on DIBL

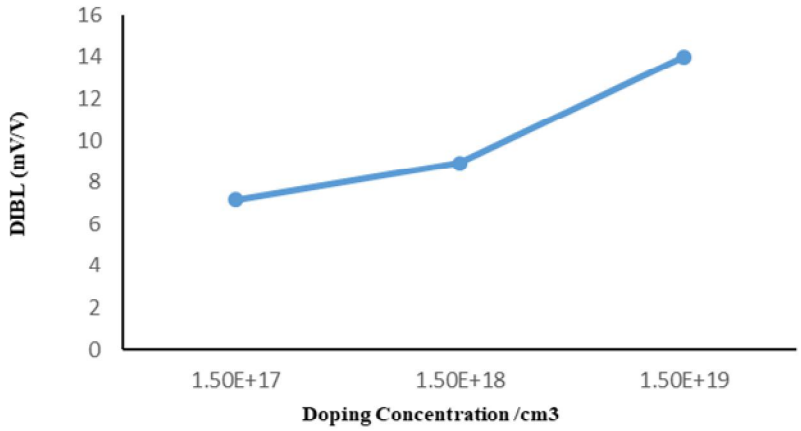

Fig.9: DIBL of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E19/cm^3)

DIBL of Junctionless N-channel FinFET for varying channel doping concentration (1E17 to 1E19/cm^3) and source & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.9. With the Drain Induced Barrier Lowering (DIBL) the improvement on these devices comes from a smaller channel doping concentration.

Table: (b) Comparison of Ioff current, Ion/Ioff, subthreshold swing and Drain Induced Barrier Lowering (DIBL) of proposed device Junctionless N-channel FinFET with conventional FinFET.

S. No	Parameter	Proposed Device	Conventional FinFET
1.	I_{OFF}	3.69E-18	2.821e-10
2.	I_{ON} / I_{OFF}	1.58E+12	.621*(10^5)
3.	SS	60.71 mV/dec	70.0mV/dec
4.	DIBL	7.44 mV/V	50.0 mV/V

On comparing the Proposed device i.e. Tri-gate Junctionless 22nm N-channel FinFET with other devices i.e. conventional FinFET electrical characteristics ($I_{ON}/I_{OFF,}$ Subthreshold slope, DIBL) of proposed device has been significantly improved. Tri-gate Junctionless FinFET due to the presence of three gate, it provide better screening of short channel effects in term of DIBL, Subthreshold slope and improved ON state current, resulting in high I_{ON}/I_{OFF} ratio.

IV. CONCLUSION

The dc characteristics Tri-gate JL N-channel FinFETs scaled down to 22nm channel length is investigated and the effects of varying the channel doping concentration is analyzed. It is observed that the threshold voltage decreases and ON-current decreases with increasing channel doping concentration. While DIBL and subthreshold swing of Tri-gate Junctionless N-channel FinFET increases with increasing channel doping concentration. DIBL and subthreshold swing of Tri-gate Junctionless devices are also measured and compared with that of conventional FinFET. A Tri-gate Junctionless FinFET has better control over channel charges, nearly ideal subthreshold slope, high ON/OFF current ratio, lower subthreshold leakage current. Thus JLFinFET is observed to suppress the short channel effects in a better way.

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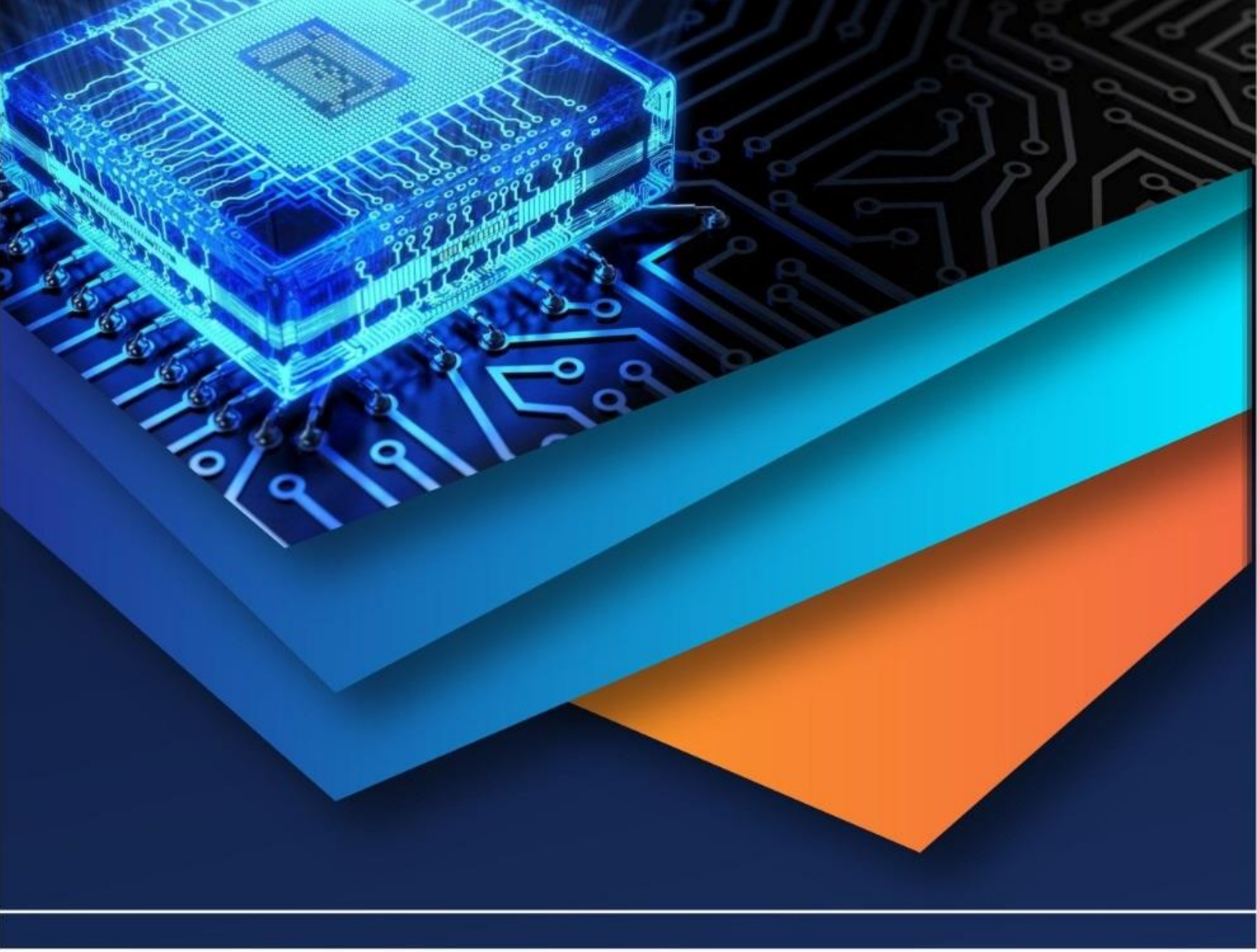

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