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Evaluating the Effectiveness of Detecting Small Delay Defects Using Signature Analysis Technique and Scan Design

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Abstract---This paper presents a delay measurement technique using signature analysis, and a scan design for the proposed delay measurement technique to detect small-delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator(VCG). The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors. The evaluation with Rohm 0.18-μm process shows that the measurement time is 67.8% reduced compared with that of standard delay scan design on average. The area overhead is 23.4% larger than that of the delay measurement architecture using standard scan design, and the difference of the area overhead between enhanced scan design and the proposed method is 7.4% on average. The data volume is 2.2 times of that of test set for normal testing on average.
Key words: Delay measurement, standard scan design, signature analysis, Variable clock generator (VCG).

I. INTRODUCTION

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems[1]. If small-delay defects cannot be detected in LSI screening, the chips will behave abnormally under particular operations in certain applications, and their lifetime may become very short due to the vulnerability to the transistor aging. Therefore to keep the reliability after shipping, enhancing the quality of the testing for the small-delay defect detection is an urgent need. The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects[2]. However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. Therefore development of the embedded delay measurement technique is required. Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques[3]. In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high ac-curacy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation. However, it has a drawback. The measurement time of the technique depends on the time for the scan operation. These days, the gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical. Noguchi *et al.* proposed the self testing scan-FF. The flip flop reduces the required number of scan operations, which makes the measurement time practical[2]. They also proposed the area reduction technique of the self testing scan-FF[4]. However, the area overhead of these methods is still expensive compared with the conventional scan designs. This paper presents a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and

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silicon debugging. The rest of this paper is organized as follows. In Section II, preliminaries are discussed. Section III explains the proposed method. Section IV shows the experimental results. Finally, Section V concludes this paper.

II. PRELIMINARIES

A. *Related Works*

These days, various methods for small-delay defect detection have been proposed. The path delay fault testing with a normal clock width is the most popular and is widely used[5]. In this method, we choose the longer paths to detect the smaller cumulative delay due to the small delay distributed on the paths. The larger the cumulative delays, the higher the probability of the detection of the distributed small delay. However, the coverage of the small delay defect detection largely depends on the normal clock width, which is a problem of this method. On the other hand, to solve the problem, methods with delay fault testing using a variable clock generator have been proposed. The delay fault testing with a smaller test clock reduces the slack of the paths. Therefore the smaller delay defects which cannot be captured with the normal clock width can be captured with the appropriate smaller test clock width.

Yan *et al.* proposed a delay testing scheme that identifies small-delay defects in the slack interval by comparing switching delays of a neighboring die on a wafer[7]. In this method, a fault site is sensitized multiple times continuously with reducing the test clock width by the slack interval. The abnormal switching delays are detected by comparison with the test results in the neighboring die. Another work detects small-delay defects by analyzing the failing frequency, which is the minimum frequency that the delay fault testing fails when the path is sensitized multiple times continuously with increasing the test clock frequency[8].

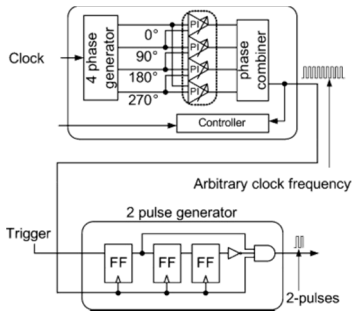


Fig 1: On-Chip Variable Clock Generator

These days, small-delay defect detection methods using on-chip delay measurement techniques have been proposed. The direct measurement of the real delay of each path of each chip screens outlier chips robustly even in the presence of process variation or the gap between real and simulation environment. It realizes higher fault coverage of small-delay defects than the simulation based ones. In addition, it can be used not only for the detection of small-delay defects, but also for the debugging[16]- [17]. Because modern chips are too huge and complex, LSI CAD tools cannot optimize the design enough. Hence, the manufactured first silicon chip usually does not meet the specification in spite of the tighter release to production(RTP) schedule. Therefore silicon debugging and design for debugging (DFD) become much more important in modern chips[18]. Various silicon debugging technologies and DFD methods have been proposed[19]–[22]. On-chip delay measurement provides accurate information of the delay of inside paths for the debugging of small-delay defects[23]. Most of the conventional works of on-chip delay measurement are classified to either a proposal of an embedded delay measurement circuit or that of a scan architecture for scan-based on-chip delay measurement with a variable clock generator. Some works proposed embedded delay measurement circuits of modified vernier delay line(VDL). Datta *et al.* the embedded delay measurement circuit with high resolution[24]. It is the first work of an embedded measurement circuit of modified VDL to the best of our knowledge. Tsai *et al.* proposed the area efficient and noise insensitive modified VDL with coarse and fine parts namely BIDM[25]. Pei *et al.* also proposed the area efficient modified VDL. The feature of this method is delay range of each stage of VDL. The delay ranges increase by a factor of two gradually, which reduces the required stages. Therefore the area is smaller than Datta's work. The modified VDLs achieve high resolution. However they require redundant lines to feed the input and output signals of the measured paths, which needs the compensation of the delay effect of the redundant lines. Tanabe *et al.* solved the problem by removing the delay of the redundant lines from the measured delay using some additional embedded circuits. The proposed technique is categorized to the scan-based one.

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B. On-chip Variable Clock Generator

In the proposed method, the clock width should be reduced continuously by a constant interval as explained later. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator is indispensable for the proposed method. Various variable on-chip clock generators have been proposed[9]–[12]. In this paper, we use the on-chip variable clock generator proposed by Noguchi *et al*[2]. Generally, the variable clock testing requires a variable on-chip clock generator. In variable clock testing, the test clock frequency should be optimized to each test vector. To improve the test quality, various optimization methods of the test clock and test set have been proposed[13]–[15]. Fig. 1 illustrates the circuit. The circuit consists of the phase-interpolator-based clock generator and the 2-pulse generator. The phase-interpolator-based clock generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal. Some of the specification and the evaluation results are shown in Table I[11].

C. Evaluation of Small-Delay defects with Measurement of delay on Chip

The proposed method uses the Noguchi's small-delay defect detection technique[2]. In this technique, the test clock width for delay fault testing of each path is determined with the normal path-delay distribution of each path. This strategy has already been applied to various small-delay detection techniques[13].

SPECIFICATIONS[11]: TABLE I

Process	90nm CMOS
Occupied area	300 [μm] × 128 [μm]
Input clock	1.5GHz 4phase
Output clock	1GHz to 2GHz 4phase
Functions	· Frequency control · Jitter generation · Duty ratio control · Phase control
Timing (Phase) Step resolution	5.2ps (2.8°)
Step error (5 chip measured)	±1.3ps ∼ ±2.4ps (±0.7° ∼ ±1.3°)
Cumulative timing error (5 chip measured)	Best chip Worst chip ±5.4ps ∼ ±11.2ps (±2.9° ∼ ±6.3°)

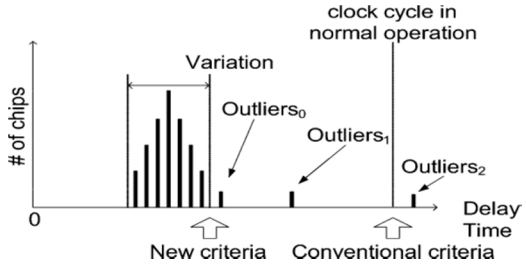


Fig 2: Decision of test clock width based on path delay distribution obtained by chip measurement [2]

But its originality is to obtain the path-delay distribution with the delay measurement of the paths of the fabricated chips. Fig.2 shows the path delay distribution of a path obtained by the delay measurement of the fabricated sample chips. The horizontal axis is measured delay. The vertical axis is the number of chips. The chips which have delay inside the range Variation are normal chips. The chips which have delay outside the range Variation, namely outliers$_0$, outliers$_1$, outliers$_1$, are abnormal chips. The delay outliers$_2$ is the outside of the clock cycle in normal operation. Therefore it will be detected by conventional delay fault testing with the clock cycle in normal clock operation which is Conventional criteria. The delay outliers$_0$ and outliers$_1$ are within the clock cycle in normal operation. The conventional delay fault testing regards them as good chips. However because the delay is outside Variation, it will cause improper operations under particular operation in certain applications and may cause improper operations after shipping due to the effect of aging[2]. In Noguchi's technique, the test clock cycle is set to the upper limit of the distribution of normal chips, which are new criteria. Then all the outlier chips are detected by the delay fault testing. In small technology, the path-delay distribution calculated by simulation is different from that of the fabricated chips. Therefore the quality of its strategy is higher

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than that of simulation based ones. Because the Noguchi's technique requires the measurement of the explicit paths, the paths should be single-path sensitizable[5]. The aim of the technique is to screen the chips which have abnormal delay in gates or wires. Therefore the test set for the measurement should detect all the transition faults which are sensitized through single-path sensitizable paths. The proposed method is a new delay measurement technique for the small-delay defect detection technique.

III. PROPOSED DELAY MEASUREMENT TECHNIQUE USING SIGNATURE ANALYSIS

This section explains the proposed measurement method. Section III-A presents the concepts of the proposed method. Section III-B explains the implementation of the proposed method. Section III-C ex-plains the reduction method of the tester channel and describes the scheme for the decision of the number of the required extra latches to keep the cost realistic. To apply the proposed method and realize short measurement time, some constraints should be put on ATPG.

A. Basic concepts of proposed method

This section explains the concept of the proposed delay measurement. The target paths of the proposed method are single-path sensitizable[5]. Basically, the proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement. Fig.3 shows the basics of the proposed method. This example has three flip flops FF_0, FF_1, and FF_2 . Each flip flop has the input line (bottom), the output line (upper), and the

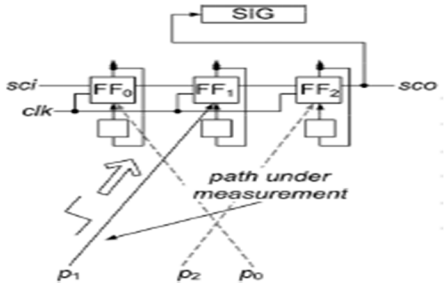


Fig 3: Concept of proposed delay measurement

clock line clk each flip flop FF_i is connected to an extra latch. At first, we assume that each flip flop has its own extra latch. The value of each flip flop is stored in the correspondent latch, and the value of each latch can be loaded to the correspondent flip flops in arbitrary timing. In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation. It reduces the time for multiple sensitization of a path drastically. The horizontal line through these flip flops represents the scan path. The symbols sci and sco represent the scan input and output, respectively. The rectangle SIG represents the signature register using the linear feedback shift register as its basic component. The input of SIG is connected to the output of the last flip flopFF_2. More detail structures of the flip fops and the signature register are shown in Fig.4 and 5, respectively.

Here, we measure the delay of p_1. In this example, we assume that the clock width of normal operation is 10 ns, and the resolution of the delay measurement is 2 ns. First, SIG is initialized with reset operation. Second, the target path p1 is tested continuously 5 times with the test clock reduced gradually by the resolution. The multiple clock width testing is realized by the variable clock generator explained in Section II-B.

When the number of flip flops is n, clock width is T, the measurement resolution is ΔT, and the continuous testing time is N_{means}.Delay measurement sequence of a target path is as follows. Here, we assume that the test vector is already stored in the latches.

Step 1:Initializing SIG.

Step 2:The vector is loaded from the latches.

Step 3:Test clock width T is set to normal clock width.

Step 4:Test clock is applied.

Step5:The test response is sent to SIG which is connected to the output of FF_{n-1} with n-k clocks.

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Step 6:If testing time is equal to N_{meas}, go to Step7 after the signature value of SIG is retrieved, otherwise go back to Step2 after the clock width T is updated to T-ΔT.
Step 7: The delay value is estimated by comparing the retrieved signature value.

B. Implementation of Measurement technique
In this subsection, we explain the implementation of the proposed measurement system. First we explain the important components to understand the whole proposed system. After that, the whole system is presented.

1) Scan Flip Flop for Measurement: Fig. 4 is the gate level description of the scan flip flop for the proposed measurement. The lines *D*, *Q*, and clk are the input, output, and clock lines, respectively. The line *latch* is connected to an extra latch which provides the test bit to the flip flop. The lines *si* and *so* are the input and output for constructing the scan path. The input *si* is connected to *so* of an adjacent scan flip flop or the scan input. The output *so* is connected to *si* of an adjacent scan flip flop or the scan output. The flip flop has two multiplexers. The lines *si* and latch are the inputs of the upper multiplexer controlled by se_1. The output of the upper multiplexer and *D* are the inputs of the bottom multiplexer controlled by se_0. When se_0=0, the flip flop is in normal operation mode. When se_0=1 and se1=*1*, the flip flop is in scan operation mode. When se0=*1*, se1=*0*, the flip flop loads the value stored in the latch connected to the latch line.

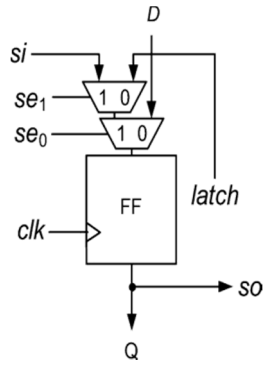


Fig 4: Scan flip flops for proposed measurement

2) Reconfigurable Signature Register: The signature register for the proposed measurement requires the following functions to meet the demand of the proposed measurement.

Capturing the test response in arbitrary timing.
Shifting out the signature data in arbitrary timing.

Fig. 5 shows the architecture of the signature register for the proposed measurement. The length of the signature register in this example is four bit. Therefore it has four flip flops FF_0,FF_1,FF_2,FF_3. The signature register can be configured to a shift register. The line sge controls the configuration. When sge=1, it works as a signature register. When sge=0, it works as a shift register. The line in is the input of the signature register. During measurement, test responses are sent to in. The line clk is clock line. The clock line is controlled be sck. When sck=0,the signature register does not capture the input value. When sck=1, the signature register capture the input value synchronizing with the positive edge of clk. By controlling sck signature registers capture the target test response. When sge=0,this circuit configure to the shift register. The input is is sgi. The output is sgo.

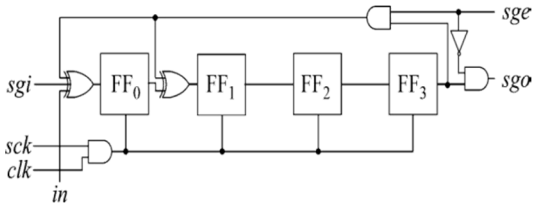


Fig 5: Four bit Reconfigurable signature register

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3) Proposed system: Fig.6 shows the proposed measurement system. The proposed system consists of the low cost tester and the chip with the variable clock generator (VCG) explained in section II-B and BCD decoder. The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flip-flops and the signature registers independently. The reset operations are controlled by the tester.

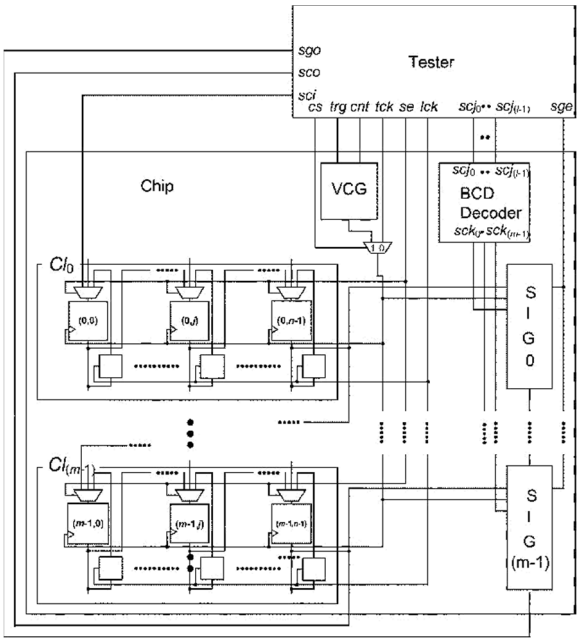


Fig 6: Proposed measurement system

The low cost tester controls the whole measurement sequence. The clock frequency tck is slower than the functional clock. The line Sgo Retrieves the signature data from the signature registers to estimate the measured delay. The line sci sends the test vectors to the scan input of the chip. The line sco gets the data of the flip-flops from the scan output of the chip. In the proposed measurement sequence, sco is not used. However it is used to check the flip-flops are the additional latches before the measurement. The line cs is the controller line. The proposed measurement used both the slow tester clock tck and the fast double pulse generated by on chip VCG. The line cs selects the slow and fast clock. If cs is 1,the fast clock is sent to the clock line clk of the components. Otherwise the slow tester clock tck is sent. The lines trg and cnt are the input lines for VCG. The double pulse is launched synchronizing with the positive edge of trg. The line cnt controls the width of the double pulse. The lie se controls the scan flip-flops. The line lck controls the latches for storing test vectors. The lines $scj_0 \ldots scj_{i-1}$ are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of signature registers $sck_0 \ldots sck_{m-1}$ .As explained later ,the decoder is used to reduce the input lines for the control data of the signature registers. The sge is the enable signal for the signature registers. The flip-flops in the chip are classified to the clusters $Cl_0 \ldots Cl_{(m-1)}$. Here, we assume that each cluster has n flip-flops, and thus the number of flip flops is mn .In general, the number of flip flops of the last cluster is N_{FF}modn, where N_{FF} is the number of flip flops, or n. The coordinate(i,j) written in the flip flops indicates the location. The number i is the cluster id. The number j is the order in the cluster. The output of the flip flop of (i,n-1) which is the tail flip flop of each cluster cl_i is connected to the flip flop of (i+1,0) which is the head flip flop of Cl_{i+1}.These lines construct the scan chain. The output of tail flip flop of each cluster is connected to the input of the signature register. The paths whose test response is captured by the flip flop s included in Cl_i is measured by SIG_i. The control lines of the signature registers are connected to the BCD decoder.

C. Measurement sequence

Here, we explain the measurement sequence. First, the measurement sequence of the paths simultaneously sensitized in a test vector is explained in Section III-C1. After that, the whole measurement sequence is explained.

1) Measurement Sequence Per a Test Vector: When the measurement system has *m* signature registers, $SIG_0 \ldots SIG_{(m-1)}$, *m* paths can be measured in parallel maximally. To reduce the measurement time, we measure multiple paths simultaneously.

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2) Tester Channel Reduction: If sck of each signature register is directly fed to the inputs of the chip, it requires the same number of the extra inputs as the number of the signature registers. It increases tester channel width. To keep the tester channel width short, we use the BCD decoder as depicted in Fig.6. Each bit value of these bit sequences is grouped. Generally, the width of the slice of sck is n, the width of encoded slice of scj is $[\log_2 n]$. However, for the encoding, each slice is permitted only 1 bit with the value 1. More than two bits with value 1 is not permitted. This restriction puts the constrain on ATPG for the generation of the test set for the measurement.

3) Scheme for Decision of Number of Extra Latches: The proposed method uses extra latches to accelerate the measurement time. To simplify the explanation, we have assumed that each flip flop has an extra latch. But adding an extra latch to each flip flop makes the area overhead unrealistic. To solve the problem, we make multiple flip flops share an extra latch. This subsection explains the scheme for the decision of the number of the required extra latches.

The proposed scheme decides the number of the required extra latches, the connection from the outputs of flip flops to the inputs of the latches, and the connections from the outputs of the latches to the latch lines of the flip flops. The proposed scheme makes the number of the required extra latches as small as possible considering the test vectors and the routing restriction. Routing window is introduced to avoid extraordinary long redundant lines. In the process of searching the sets of flip flops sharing a latch, the search space is restricted within the window.

IV. RESULTS & DISCUSSION

In this section, we present the experimental results. In Section IV-A, the proposed method is compared with the conventional methods. The clock frequencies are the same as that of Noguchi's methods[2]-[4], that is, the normal clock frequency is 100 MHz, and the scan clock frequency is 10MHz. The length of the signature register is 8 bit. The test set consists of test vectors which detects all single-path sensitizable transition faults. The paths sensitized by these test vectors are measured. In this evaluation, the average delay of signal propagation of the measured paths is assumed to be the half of the clock width. The results are obtained by synthesis with Synopsys design compiler using Rohm0.18 μm process. The result should be realistic compared with the conventional scan designs for DFT.

A. Comparison with conventional scan-based measurement

In this section, the proposed method is compared with the delay measurement with conventional scan designs, namely standard scan design and enhanced scan design.

1) Measurement time: The comparison of measurement time is shown in Table II. Here, we show the result when N_{meas}=100 and N_{meas}=200,respectively.The sub columns T_{STD}(ms) and T_{SIG}(ms) are the measurement time of standard scan design and the proposed method.

Table III shows the time delay in total logical blocks from sge to sgo in the proposed system compared with existing methods[21]-[22].

TABLE II: Measurement Time

circuit	N_{meas} = 100			N_{meas} = 200		
	T_{STD}	T_{SIG}	R_T	T_{STD}	T_{SIG}	R_T
s5378	635.4	181.2	71.5	1270.8	347.0	72.7
s9234	703.1	135.5	80.7	1406.1	255.4	81.8
s13207	1,068.7	291.8	72.7	2,137.4	544.1	74.5
s35932	700.4	516.2	26.3	1,400.7	817.2	41.7
s38417	7,432.1	1,263.1	83.0	14,864.1	2,199.1	85.2
s38584	4,025	1,101.6	72.6	8,049.8	1,952.9	75.7
Ave.	-	-	67.8	-	-	71.9

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TABLE III

Pro.sys.		[21]	[22]
Delay	0.71nsec	1.7ns	1.5ns
Data Path	Sge to sgo	Sge to sgo	Sge to sgo

B. Synthesis & Simulation Report

In this section, the proposed method synthesis and simulation results are reported.

1) Synthesis Report: Synthesis report shows the design summary including number of LUT's, I/O buffers, Slice registers, flip flop pairs as shown in Table IV.

TABLE IV: Design summary

Logic utilization	Used	Available	Utilization
Number of slice registers	31	10000	0%
Number of slice LUTs	22	5000	0%
Number of fully used LUT-FF pairs	21	32	65%
Number of borned IObs	12	200	6%
Number of BUFG/BUFG CTRLs	2	32	6%

2)Simulation Result: The proposed system is implemented by Xilinx software and the simulation waveforms of each module are shown below.

a) Variable Counter: In measurement of faults the clock width should be reduced continuously by a constant interval. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator utilized for this continuous reduced clock width. simulation wave of the VCG is shown in the below figure8. It consists of three Dfilpflops, one mux and decoder. clk, rst, trigger are in- and out is output of implemented VCG.

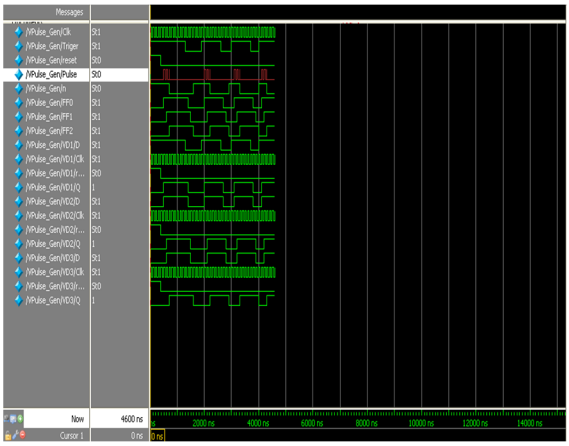


Fig 8: Simulation waveform of the VCG

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b) Signature register: Signature register uses linear feedback shift register as its basic component. Once the test vector stored in the latches by scan-in operation, the test vector can be loaded from these latches in a clock without scan-in operation. Simulation wave of the signature register is shown in the figure9. It reduces the time for multiple sensitization of a path drastically. The length of the signature resister is 4-bit. In the proposed system, signature register is implemented by using four Dfilpflops. clk, in, rst, sck, sge, sgi are in and sgo is output of register. When sge=1, it works as a signature register. When sge=0, it works as a shift register.

c) Cluster: Each cluster has n number of flip flops. The output of tail flip flop of each cluster is connected to head flip flop of next cluster. Simulation wave of the cluster is shown in the below figure10. It forms the scan chain and connected to signature register. Cluster gets the input from scan-in operation of test vector. The cluster of proposed system contains three scan-FF. Each FF have one Dflipflop , Latch and two mux , with clk, d, en, rst, sei, se0, se1 as in and scl is outputs.

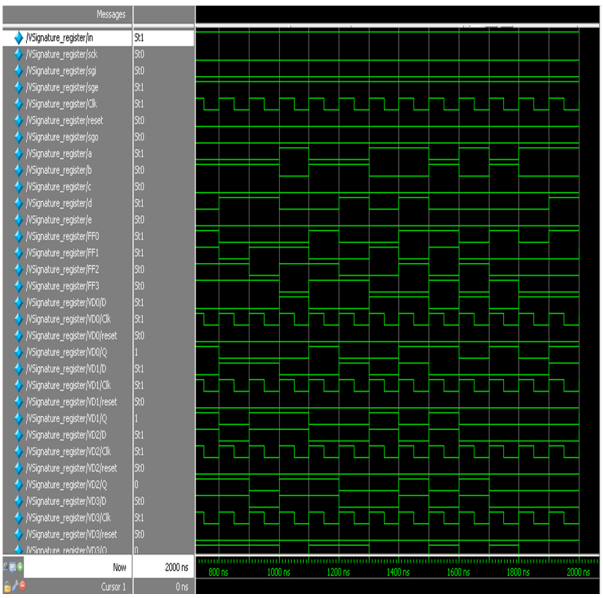


Fig 9: Simulation waveform of signature register

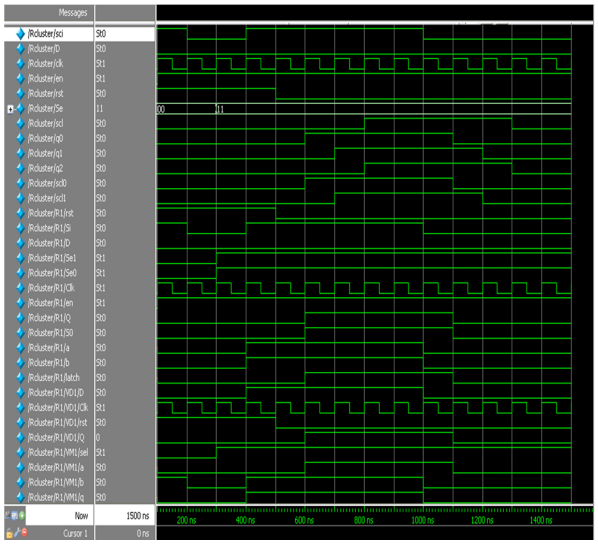


Fig 10: Simulation waveform of the cluster

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When se0=0, the flip flop is in normal operation mode. When se0,se1=1 the flip flop is in scan operation mode. When ,se0=1, se1=0, the flip flop loads the value stored in the latch connected to the latch line.

e) Top Module: The path of top module is from Sge to Sgo which are connected through several blocks and all are connected with a Tester. The output of top module is generated by the output of signature registers. Signature registers evaluate the output from clusters output data. And clusters generate the test vector for signature register by the test vector of scan flip flops. The below simulation result in figure11 shows the output generated from Sge to Sgo.

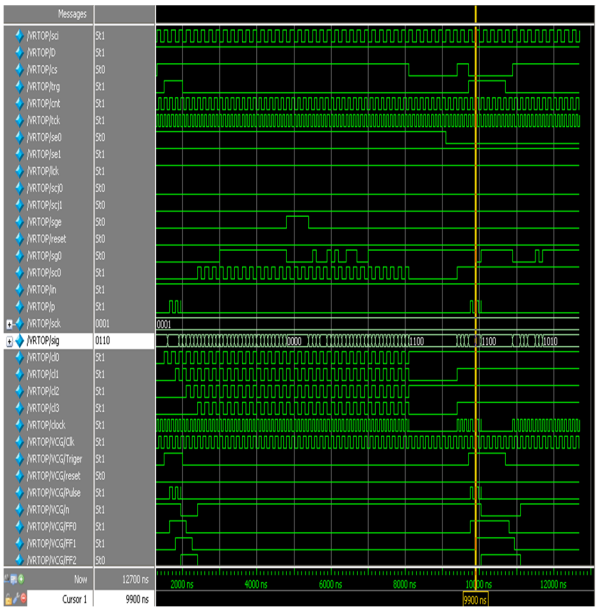


Fig 11: Output generated from Sge to Sgo

V. CONCLUSION

Effectiveness of detecting small delay defects using signature analysis technique and scan design is proposed. The proposals can be applied not only SOC but also field programmable gate array(FPGA).Because the process of FPGA is getting extraordinary smaller these days, the small delay defect becomes serious problem in FPGA, too. The application of proposed method is very useful to FPGA. A future work is the low cost application of the proposed measurement to FPGA. When we measure Short paths, measurement error can be increase for the IR drop induced by higher test clock frequency. It can reduce the test quality. Another future work is the reduction and the avoidance of the measurement error caused by the IR drop.

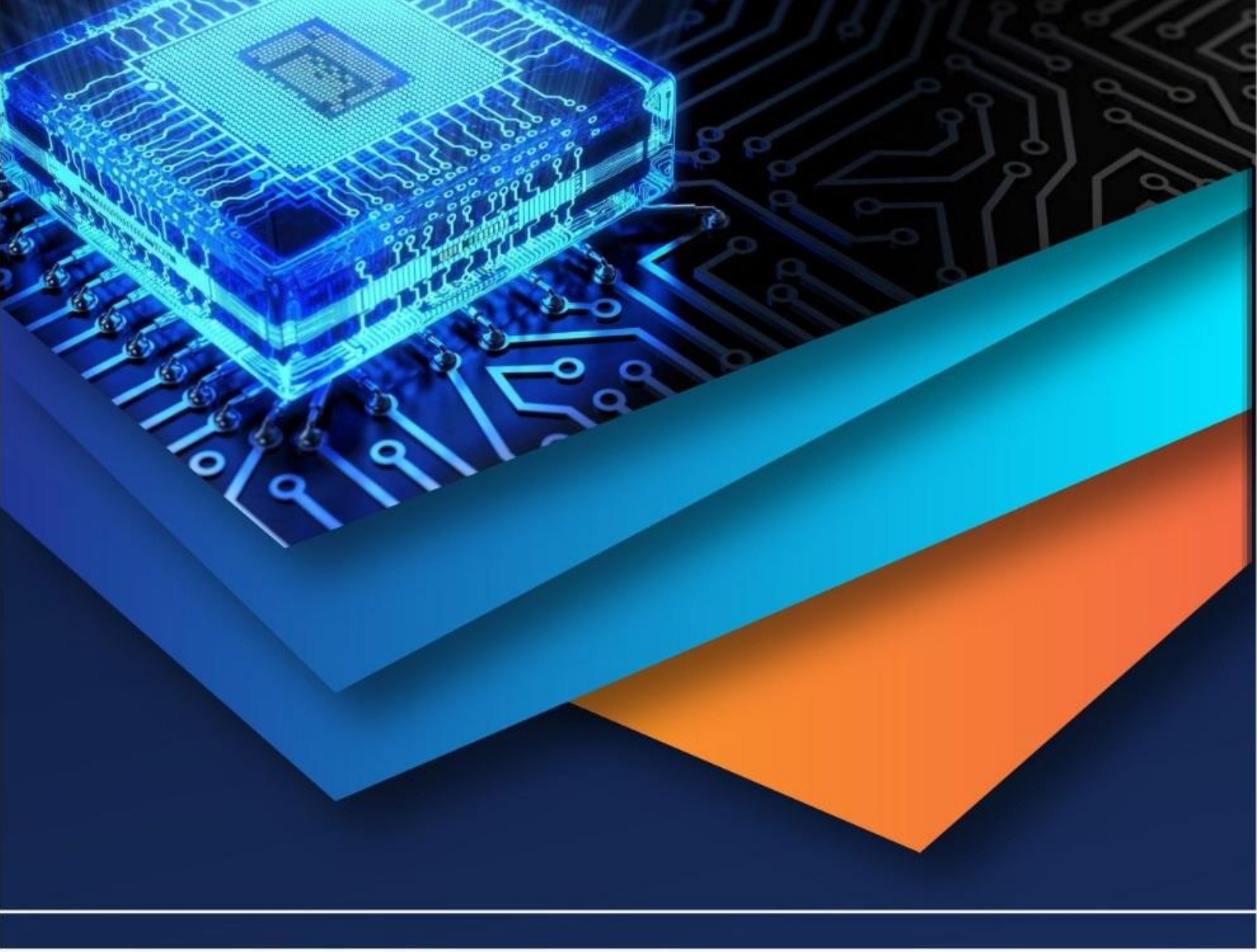
REFERENCES

[1] N.Ahmed and M.Tehranipoor, Nanometer Technology Designs: High-Quality Delay Tests. New York:Springer,2007.
[2] K.Noguchi, K.Nose, T.One and M.Mizuno,"A Small-delay Defect detection technique for dependable LSIs," in Proc. IEEE Symp. VLSI Circuits,2008,pp.64-65.
[3] B.I.Dervisoglu and G.E.Stong, "Design for Testability: Using sca-path technique for path-delay test and measurement," in Proc.IEEE Int.Test conf.(ITC),1991,pp. 365-374.
[4] K.Noguchi, K.Nose, T.Ono, and M.Mizuno, "An area reduction technique of self-testing FFs for Small-delay defects detection," The Inst. Electron., Inf. Commun. Engg. (IEICE), Tech. Rep. DC2009-16,2009.
[5] A.Krstic and K.-T.Chen, Delay Fault Testing for VLSI Circuits. Norwell, MA: Kluwer,1998.
[6] J.-J. Liou, L.-C.Wang and K.-T.Chang,"Enhancing test efficiency for delay fault testing using multiple-clocked schemers," in Proc.Des.Autom. Conf.(DAC),2002,pp.371-374.
[7] H.Yan and A.D.Singh, "Evaluating the effectiveness of detecting delay defects in the slack interval: A simulation study," in Proc. IEEE Int. Test Conf. (ITC), 2004, pp. 242–251.
[8] J.Lee and E.jMcCluskey,"Failing frequency signature analysis"in Proc.Int. Test Conf.(ITC),2008,pp. 1-8
[9] R.Tayade and J.A.Abraham,"On-chip programmable capture for accurate path delay test and characterization," in Proc. IEEE Int. Test Conf.(ITC),2008,pp.148-

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159.
[10] M.Beck, O.Barondeau, X.Lin, and R.Press,"Logic design for on-chip test clock generation-implementation details and impact on delay test quality," in Proc.IEEE Des.,Autom. Test Eur. Conf. Exhib. (DATE),2005,pp. 56-61.
[11] S.Kaeriyama, M.Kajita, and M.Mizuno. "A 1-to-2GHz 4-phase on-chip clock generator with timing-margin test capability," in Dig.Tech. Paper Int. Solid-State Circuits Conf.(ISSCC),2007,pp.174-594.
[12] T-y.Li,S-Y.Huang, H.-J. Hsu, C.-W. Tzeng, C.-T. Huang, J.-J.Liou, H.-P. Ma, P.-C.Huang, J.-C. Bor, and C.-W.Wu, "Af test :Adaptive-frequency scan test methodology for small-delay defects," In Proc. IEEE Int.Symp.Defect Fault Toler. VLSI Syst. (DFT),2010, pp. 340-348.
[13] N.Ahmed and M.Tehr ainipoor,"A novel faster-than-at-speed transition-delay test method considering IR-drop effects," IEEE Trans.Comput.-Aided Des.Integer. Circuits Syst., vol.28, no.10,pp.1573-1582, Oct.2009.
[14] M.Yilmaz, K.Chakrabarty, and m.Tehranipoor, "Test-pattern grading and pattern selection for Small-delay defects," inProc.IEEE VLSI Test Symp.(VTS),2008,pp.233-239.
[15] B.Kruseman, A.K.Majhi, G.Gronthoud, and S.Eichenberger, "On hazard-free patterns for fine-delay fault testing," in Proc. Int. Test Conf. (ITC), 2004, pp. 213–222.
[16] M.Sharma and J.H.Patel, "Bounding circuit delay by testing a very small subset of paths," in Proc. IEEE VLSI Test Symp. (VTS), 2000, pp. 333–341.
[17] E.Flanigan, T.Haniotakis, and S.Tragoudas, "An improved method for identifying linear dependencies in path delay faults," in Proc. IEEE Int. Symp. Quality Electron. Des. (ISQED), 2006, pp. 456–462.
[18] H.Balachandran, K.M.Butler, and N.Simpson, "Facilitating rapid first silicon debug," in Proc. IEEE Int. Test Conf. (ITC), 2002, pp. 628–637.
[19] J.S.Yang and N.A.Touba, "Enhancing silicon debug via periodic monitoring," in Proc. IEEE Int. Symp. Defect Fault Toler. (DFT), 2008, pp. 125–133.
[20] J.S.Yang and N.A.Touba, "Automated selection of signals to observe for efficient silicon debug," in Proc. IEEE VLSI Test Symp. (VTS), 2009, pp. 79–84.
[21] X.Wang and M.Tehranipoor, "Path-RO: A novel on-chip critical path delay measurement under process variations," in Proc. IEEE Int. Conf. Comput.-Aided Des. (ICCAD), 2009, pp. 640–646.
[22] X.Wang and M.Tehranipoor, "Path-RO: A novel architecture for on-chip path delay measurement," in Proc. IEEE International Test Conference (ITC'09), Oct. 2009, pp. 320–329.
[23] Y.Y.Chen and J.J.Liou, "Diagnosis framework for locating failed segments of path delay faults," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 6, pp. 755–765, Jun. 2008.
[24] R.Datta, A.Sebastine, A.Raghunathan, and J.A. Abraham, "On-chip delay measurement for silicon debug," in Proc. Great Lakes Symp. VLSI (GLSVLSI), 2004, pp. 145–148.
[25] M.C.Tsai, C.H.Cheng, and C.M.Yang, "An all-digital high-precision built-in delay time measurement circuit," in Proc. IEEE VLSI Test Symp. (VTS), 2008, pp. 249–254.

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