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Verification of Dual Port RAM using System Verilog and UVM: A Review

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Abstract*: Dual-port RAM place a prominent role in the field of SoC design. Verification of these memories are much more important while designing a complex system. As the rapid developments taken place in verification techniques, System Verilog and UVM (universal verification methodology) takes a higher priority. Because assertion-based coverage can be done using System Verilog and reusability can be achieved by UVM. In this paper, we are analysing the verification of dual port RAM under System Verilog and UVM environment.

***Keywords*: System Verilog, environment, coverage, assertion, UVM.**

I. INTRODUCTION

According to recent advancements in the field of multiprocessor, dual port RAM place a major role, it is widely used due to its interesting characteristics over single port RAM. DPRAM supports simultaneous access of read/write from or to both the ports [1]. In ASIC applications, on chip shared memories are heavily used, because of their high speed and high level of integration. In the same way multi-port SRAM compilers are developed to give acknowledgement to these requirements. Ramgen developed a DPSRAM, which provides design flexibility, high performance and it can be easily implemented in an ASIC design framework [18]. Dual port SRAM consist of two ports it's a clock controlled static RAM; each port has the ability to read/write. One port can dedicate to write operation and the other port for read operation this type of RAM is called as simple dual port RAM. Read/write modes of DPRAM is controlled by write enable signal "WE" [4]. In SoC design flow, design verification is noted as most important task. Verification places a major role; it takes almost 70 to 80 % of the time of overall SoC design process. Verification is a process of verifying the design, which is working correct or not with respect to specification. Verification process is not worried about additional design code, which does not have any affect over correctness of the design. More power can be consumed be these additional design code, and also it is not in the given specification [17].

System on chip is a combination of microprocessor/computer or any other electronic devices which may includes CPU, memory, input output devices, communication buses. Proper verification should be done before tape-out, otherwise it can lead to the unnecessary wastage of time and cost of the whole design [19]. Today, area of developing integrated circuits is growing rapidly. Simultaneously complexity of the IC design is also increasing and it leads to difficulty in verifying them. In the entire design and development, verification takes 70% of the workload. Earlier verification methods are not sufficient to meet the current requirements of verification. Various verification methodologies are developed to improve the efficiency of verification and to reduce the complexity. Universal verification methodology (UVM) is one of the recent verification methodologies which is widely used now a days. UVM is developed from OVM (open verification methodology) and also it inherits some properties of VMM (verification methodology manual) [14].

This paper is categorized as fallows. Section 2 has details of dual port RAM. Verification environment of System Verilog and UVM are discussed in section 3. Section 4, talk about result analysis and fallowed by conclusion in section 5.

II. DUAL PORT RAM

Over a period of advancements in the SoC products, necessary to have a high speed and low power memory to enhance the storage capability. Static Random-Access memory (SRAM) is the one which is largely used for SoC design. To increase the speed of execution, demand towards multi-port SRAM increases. Parallel operations can be done using multi-port SRAM, so that the total performance of the chip will increase [20]. DPRAM supports arbitrary access of the memory, as the name says it has two ports, each port can perform read/write operations simultaneously, it can be done through synchronously or asynchronously. DPRAM supports three operating modes: pipelined mode, flow through mode and moreover impact or burst mode of operation [1].

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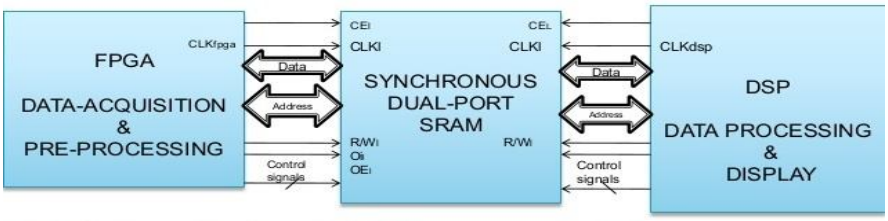


Fig.1. Block diagram of Synchronous DPRAM in coprocessor architecture: -

III. VERIFICATION ENVIRONMENT

A. System Verilog environment

System Verilog is a kind of standard hardware description language, it is well known as hardware description verification language. By making use of System Verilog, it is possible to design, simulate, test, and finally we can implement electronic circuits. System Verilog is an advanced version of IEEE 1364 verilog-2001 standard. It has the properties which are inherited by Verilog HDL, VHDL, C and C++. System Verilog verification environment consists of set of components, DUT (design under test) is verified under this environment [19].

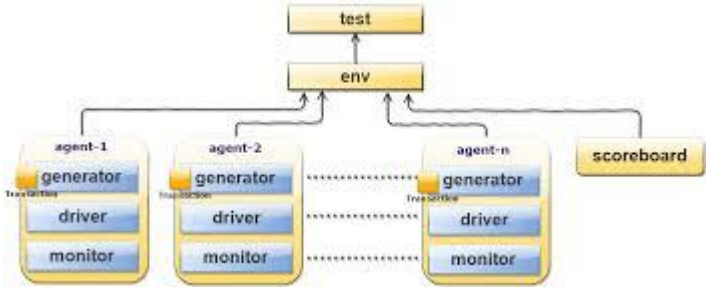


Fig.2. Hierarchy of System Verilog

System Verilog components are as follows: -

1) *Test:* It is responsible for generator behaviour.
2) *Generator:* To create random stimulus or to generate testcases.
3) *Agent:* A set of stimuli is collected and forwarded to specific interface.
4) *Driver:* It drives the stimulus from agent to design under test (DUT).
5) *Monitor*: Monitors DUT interface and forward transaction to higher layer.
6) *Scoreboard:* It compares the actual output with expected output/reference value.
7) *Assertions:* Assertions are used to validate the behaviour of a system properties.
8) *Functional coverage:* Measures how much % of features are covered.

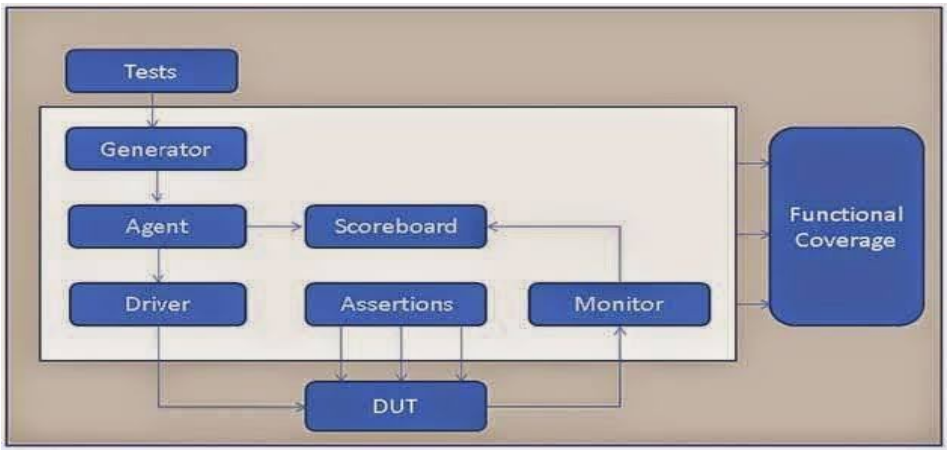


Fig.3. System Verilog verification environment of dual port RAM

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B. Universal Verification Methodology

Now a days UVM is the widely used verification methodology because it provides reusability property. Due to many reasons like unpredictable designs of products, time to market and workload on verification process requires a reusable testbenches. Coverage driven verification (CDV) is carried by UVM with the use of reusable testbench. UVM have well-structured class libraries which are used while designing the well-constructed, reusable testbench [14].

UVM consists of three main classes:

1) UVM-Object
2) UVM-Transaction
3) UVM-Component

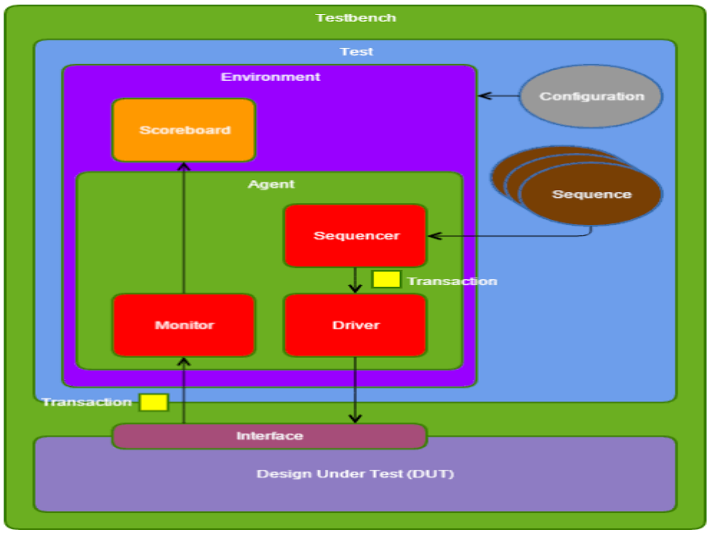


Fig.4. UVM verification environment of dual port RAM

a) Test: It is the topmost class and it handles the testbench.
b) Environment: Higher level components are grouped here.
c) Agent: It will group the UVM components and then forward it to specific interface.
d) Driver: Drives the packet level data which is available inside the sequence-item into pin level (DUT).
e) Monitor: It monitors the DUT activity on interface signals and send to higher layer in terms of packet level signals.
f) Scoreboard: Receives the packet level signals from monitor and compares them with reference values.
g) Sequencer: Responsible for routing the sequence item to the driver or vice versa.

IV. RESULT ANALYSIS

Dual port RAM is considered as a design under test (DUT), it is verified under both System Verilog and UVM. Covergroup coverage achieved as 20.1%, and 100% assertion is achieved from System Verilog environment [1]. Covergroup coverage can be achieved 100%, if the number of bins is executed properly. Because covergroup is depends on bins, if all the bins are hits then it is known as 100% covergroup coverage.

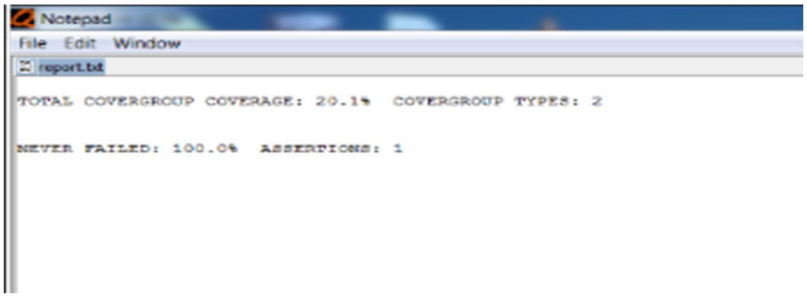


Fig.5. Coverage output

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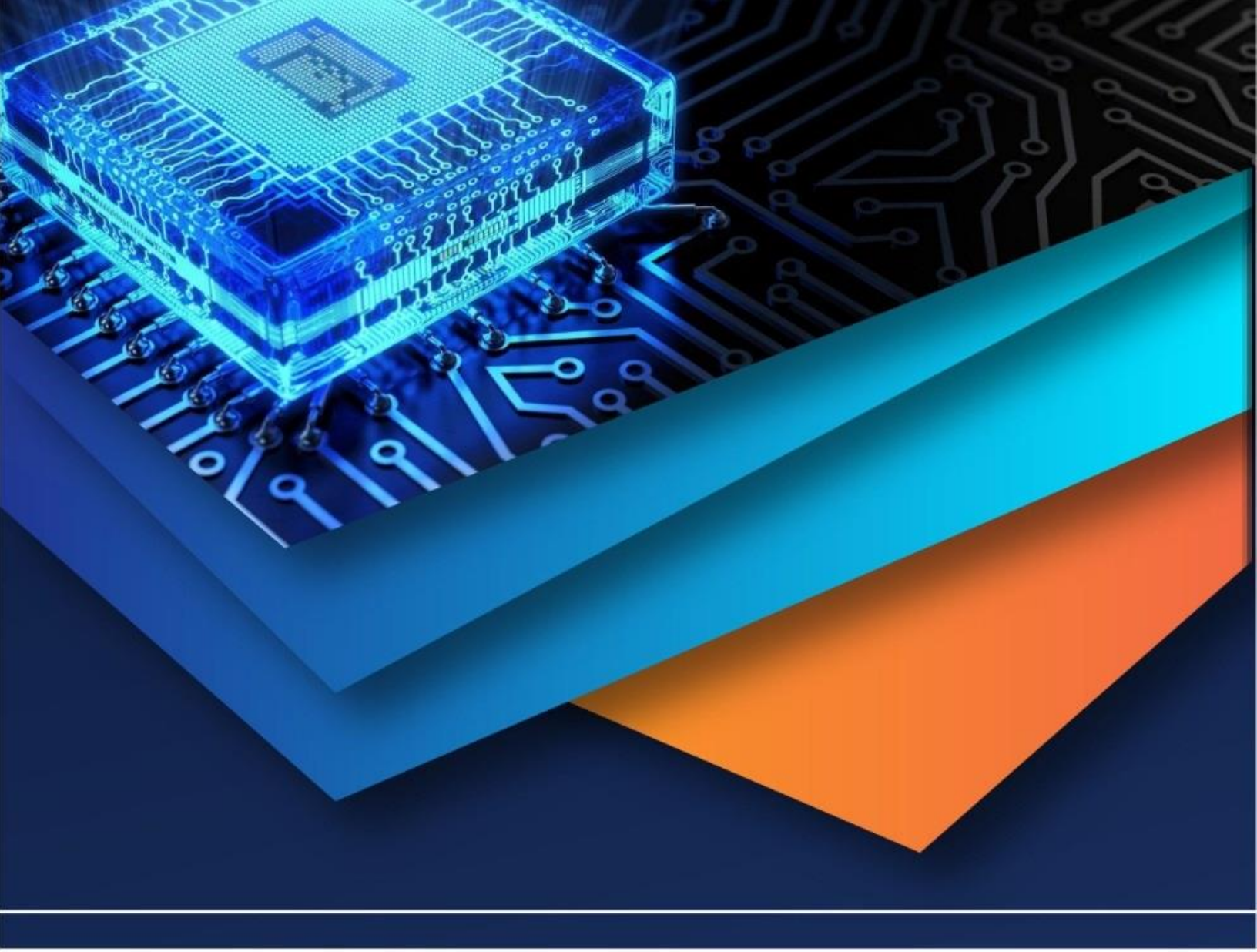
V. CONCLUSION

In this paper, we discussed characteristics of dual port RAM and its verification process under System Verilog and UVM. These verification environments are comprised of different components such as test, top, environment, agent, monitor and scoreboard. Reusability of testcases achieved by using UVM and assertion-based verification done by using System Verilog. How to increase the covergroup coverage is discussed in result analysis section.

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