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Dynamic Threshold MOSFET Based Comparators

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Abstract: ***The metal oxide semiconductor field effect transistor (MOSFET) is one of the semiconductor switching device which is extensively used in amplifiers for amplifying electronic signals. However, the analog circuit designers are continuously looking for developing low voltage and low power switching devices as there is a wide application of MOSFET in miniature circuits. The dynamic threshold metal–oxide–semiconductor (DTMOS) is one of the improved type of MOS which utilizes the body terminal of positive-channel metal oxide semiconductor (PMOS) as forth terminal in bulk conventional complementary metal oxide semiconductor (CMOS) technology to improve the performance of switching device in terms of low voltage and low power. The analog amplifiers used for amplifying electronic signals are based of electronic comparators, which are considered as power hungry device. In this paper, various comparators are implemented using DTMOS technology and compared with conventional CMOS based comparators. The comparators are simulated in CADENCE VIRTUOSO 65nm TECHNOLOGY. The simulation results of all the comparators are compared and the difference is found to be large in terms of the delay and power consumption.***
Keywords: Comparator, Cadence Virtuoso simulations, DTMOS, 65nm Technology

I. INTRODUCTION

With a fast pace of electronic industry, there is a demand of efficient and transferable electronic devices in the market with a low power consumption, high compactness, lesser time consumption with a good performance. As the demand for high rates increases, comparators must cope with this need while achieving as low power consumption and small area as possible. For example, recent communication links try to use digital receivers which mainly depend on ADCs [1]. To achieve these characteristics CMOS went through many downscaling in terms of technology.

The scaling in technology means the reducing the channel length of the MOSFET. In Analog to Digital Converters (ADC), comparator plays a crucial role. Comparator is an electronic circuitry device that is used to compare two voltages i.e. Vin and Vref and results in one output in form of digital signal. A high speed i.e. faster and less power consumption is the primary demand in the electronic world. Because of direct tradeoff between speed and power consumption of a comparator, the focus is on the implementation of a high speed and low power comparator while the other characteristics are in acceptable range [2].

From the last thirty years, there has been a high demand of the comparator with less time delay and less power dissipation. In many power applications, in the analog to digital converter especially, the comparator plays an important role. If the Vin i.e. the input of the comparator is at a greater potential than the Vref i.e. reference input, then the output of the comparator is in the logic HIGH or logic1, where as if the Vin i.e. the input of the comparator is at a lower potential than the Vref i.e. reference input, then the output waveform of the comparator is logic LOW or logic 0.

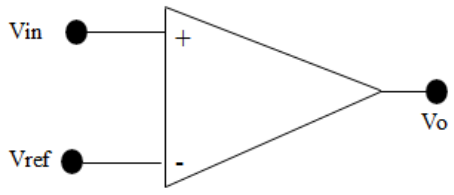

Fig 1. Symbol of a Comparator

In this paper, several comparators circuit designs have been implemented that is one of the most important apparatus of Analog to Digital converters, using conventional CMOS and DTMOS technology. The rest of the research paper is organized as follows. An overview of the DTMOS technology which has been using in the implementation of comparator is in section 2. The various comparator circuit using conventional CMOS and DTMOS is presented in section 3. The simulation results are presented in section 4. Finally, the conclusion of the project is given in section 5.

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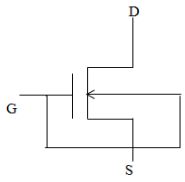
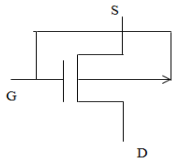
II. OVERVIEW OF DTMOS TECHNOLOGY

The DTMOS was first invented in 1994 by Mr. Fariborz. Basically, DTMOS is a technology in which the gate of the body is tied together with the body of the transistor. This connection between the body and gate causes dependability on both biasing which means any variation in the gate voltage causes the change in the body voltage. As of now, many circuits have been implemented with the help of this technology. This technique can also be used in bulk CMOS technology for applications of analog or digital circuit. However, in some of the circuits body terminal of the MOSFET is used as a forth terminal. There is the principle of dual threshold logic in DTMOS which makes it an efficient technique. When DTMOS transistor is in ON state, the threshold voltage of the transistor decreases with the increase in current and also causes the decrease in the propagation delay which is the sum of rise time and the fall time of the circuit. However, when the DTMOS is in the OFF state, the threshold voltage of the transistor increases with a reduction in leakage current and also with the minimum power dissipation. The analog amplifiers used for amplifying electronic signals are based of electronic comparators, which are considered as power hungry device. In this paper, various comparators are implemented using DTMOS technology and compared with conventional CMOS based comparators. DTMOS provides less delay with increased speed hence it is a great technique than traditional body biasing in the subthreshold region [7]. Among the various biasing techniques, this gate to body bias technique is found to be the best for the lesser delay with an increase speed.



(a)



(b)

Fig 2. Schematic of DTMOS structure (a) Symbol of a N-MOSFET (b)Symbol of P- MOSFET

Figure 2 shows the schematic of DTMOS structure. Due to the body effect, during the different modes of operation, threshold voltage of DTMOS can be altered accordingly.

III.COMPARATORS USING DTMOS TECHNOLOGY

A. Open Loop Comparator

In Analog to Digital Converters (ADC), comparators play a crucial role. A high speed i.e. faster and less power consumption is the primary demand in the electronic world. The open loop comparator is one of the basic versions of the comparator which contains two differential inputs. These types of comparators are completely static in nature. This type of comparators consists of the differential amplifiers, input stage and the output stage. The main advantage of the circuit is it consumes less number of transistors and hence the area to be consumed will be less.

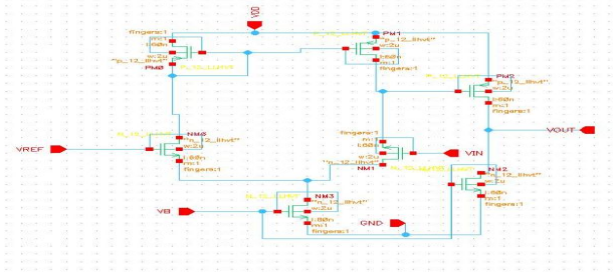


Fig 3. Schematic of Conventional Open Loop based comparator

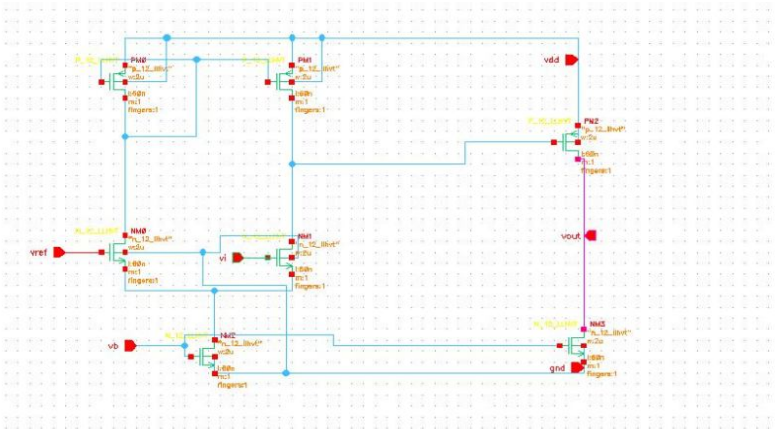


Fig 4. Schematic of Proposed Open Loop based comparator using DTMOS Technology

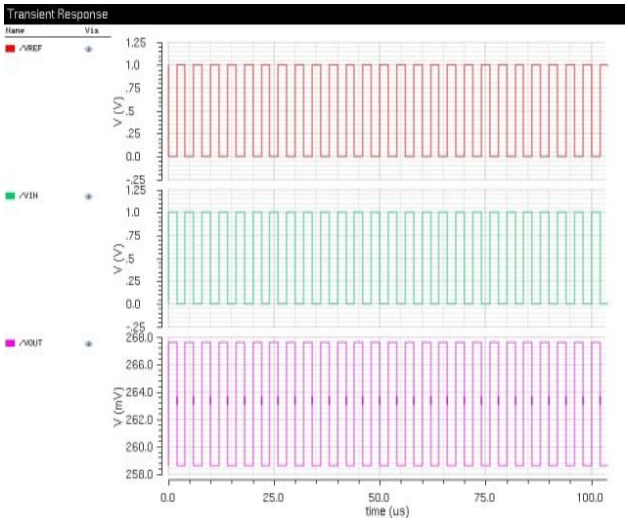


Fig 5. Transient Analysis of Conventional Open loop Comparator

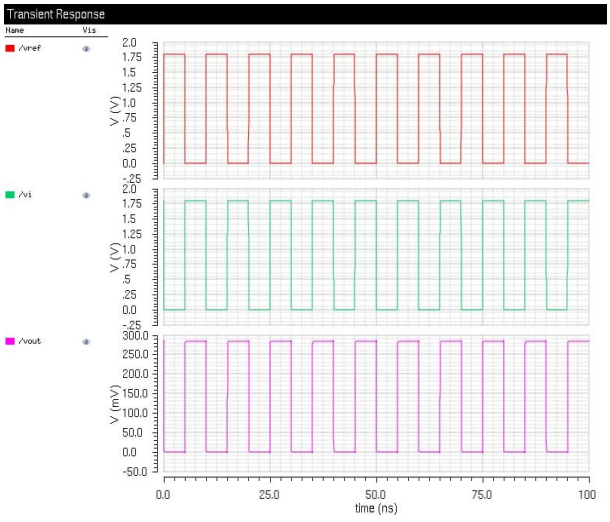


Fig 6. Transient Analysis of Proposed Open loop Comparator using DTMOS Technology

B. Pre-Amplifier based Comparator

The working of this type of comparator is divided into two sequence. The pre-amplification stage consists of the circuit is a differential amplifier with active loads. The decision circuit is the main heart of the comparator and it should be capable of discriminating the level signals. We should also design the circuit with some high rejecting noise on a signal. Now when the V_{in} is at greater potential than the V_{ref}, it will cause the PMOS to start conducting and will deliver V_{DD} which will eventually give us the HIGH potential at the output. In the next phase, the pre-amplifier stage is in disconnecting stage from the comparator and the short-circuit transistor of circuit is also switched off. Now, the comparator (inverter pair) amplifiers the charges imbalances form into digital voltage levels as the output.

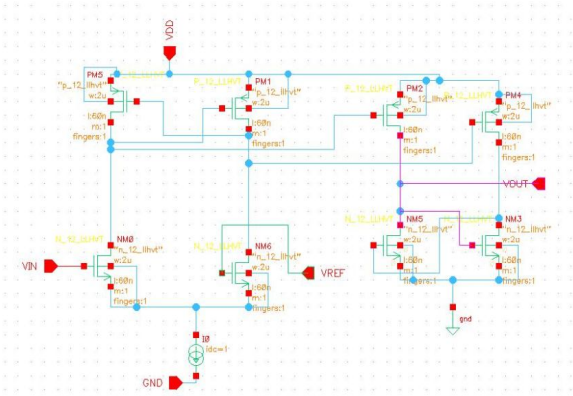


Fig 7. Schematic of Conventional Pre-Amplifier based comparator

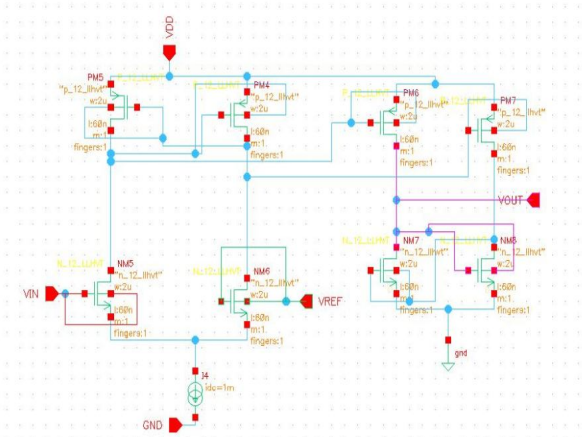


Fig 8. Schematic of Proposed Pre-Amplifier based comparator using DTMOS Technology

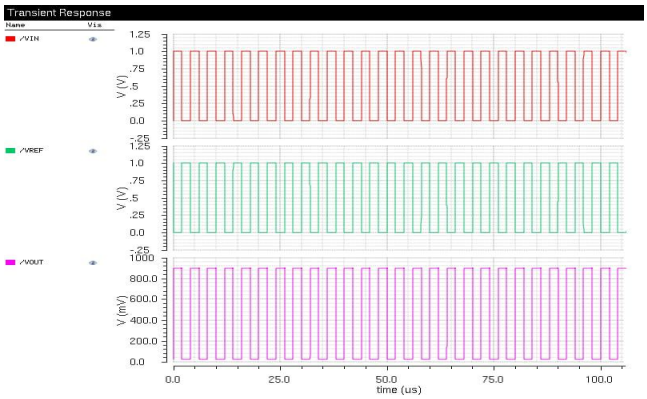


Fig 9. Transient Analysis of Conventional Pre-Amplifier based comparator

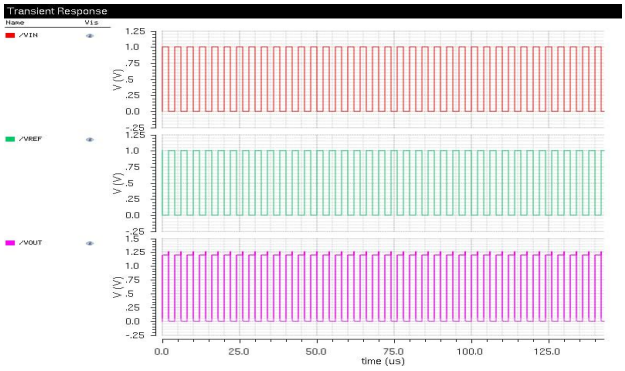


Fig 10. Transient Analysis of Proposed Pre-Amplifier based comparator using DTMOS Technology

C. Strong Arm based Comparator

The strong arm comparator is a dynamic type of comparator which can be used in many high- speed applications. The operation of the circuit is divided into two steps; reset phase when the clock is set to be HIGH and regeneration phase when the same clock is set to be LOW. So, when the clock is at 0, the two PMOS starts conducting and the reset two will remain in OFF condition. As a result, the two NMOS will start conducting and will cause two dependent voltages across the arm and result in cause of parasitic capacitance. Similarly, in next phase it will work.

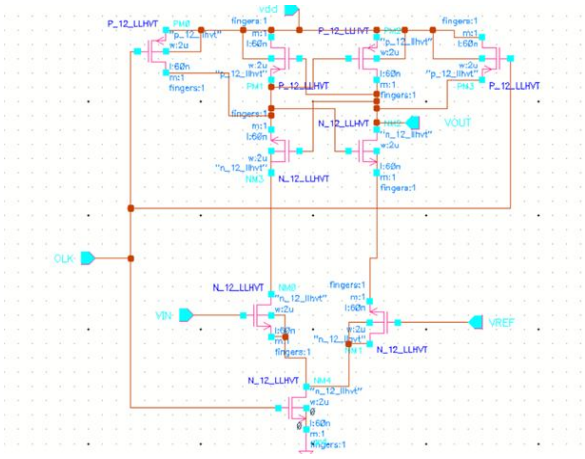


Fig 11. Schematic of Conventional Strong Arm based comparator

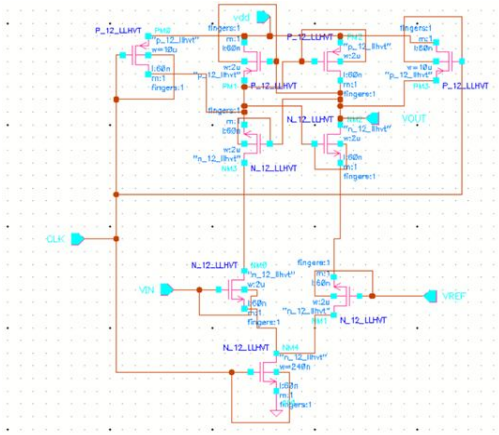


Fig 12. Schematic of Proposed Strong Arm based comparator using DTMOS Technology

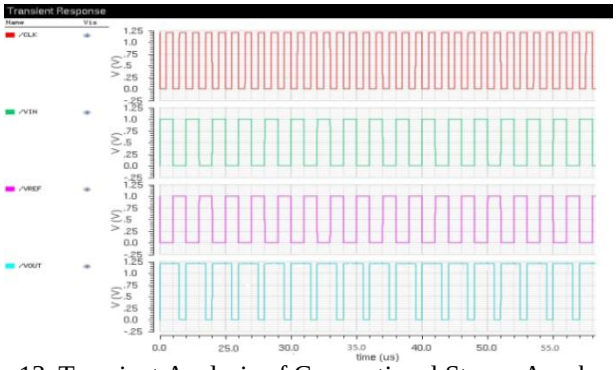


Fig 13. Transient Analysis of Conventional Strong Arm based comparator

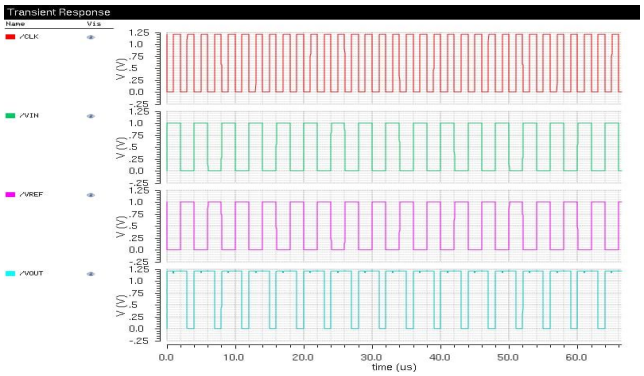


Fig 14. Transient Analysis of Proposed Strong Arm based comparator using DTMOS Technology

IV. SIMULATION & RESULTS

The simulation of the various comparator designs is done in Cadence Virtuoso with GPDK 65nm Technology. The simulation results are presented including power dissipation and delay. In these designs, we have used power supply i.e. 1 V is applied for all the conventional CMOS based comparators and also for all the proposed DTMOS based comparators. The analog amplifiers used for amplifying electronic signals are based of electronic comparators, which are considered as power hungry device. In this paper, various comparators are implemented using DTMOS technology and compared with conventional CMOS based comparators. In this work three comparator designs i.e. open loop based, preamplifier based and strong arm based comparators have been simulated using two technologies i.e. conventional CMOS based and the proposed work of DTMOS technology based to obtain the low power and high speed parameters as it is required for efficient Analog to Digital converters. The simulation results of all the comparators are compared and the difference is found to be large in terms of the delay and power consumption. The final simulation results of the various comparators are shown in Table 1.

TECHNOLOGY	POWER DISSIPATION		PROPAGATION DELAY	
	CMOS	DTMOS	CMOS	DTMOS
OPEN LOOP BASED COMPARATOR	81.38mW	0.26 µW	8.27ns	0.55ns
PRE-AMPLIFIER BASED COMPARATOR	98.07µW	2.66µW	3.82ns	0.29ns
STRONG ARM BASED COMPARATOR	13.22µW	4.26µW	3.01ns	0.08ns

Table-1 Simulation Result: Shows the comparison of Power dissipation and Propagation Delay of all the comparators using CMOS and DTMOS technology

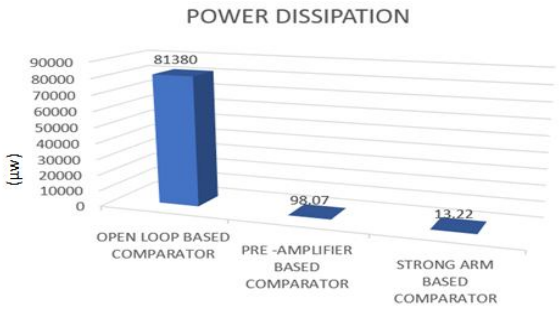


Fig 15. Comparison of power dissipation of conventional CMOS based several comparators

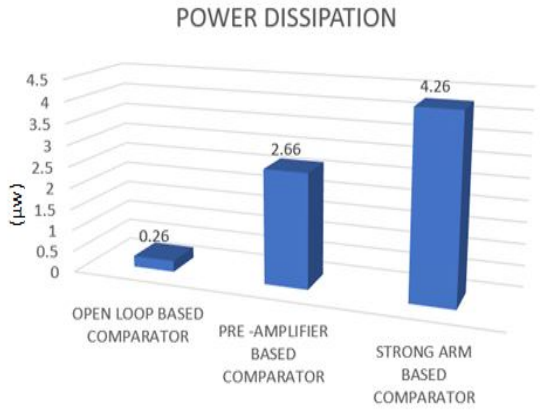


Fig 16. Comparison of power dissipation of Proposed DTMOS based several comparators

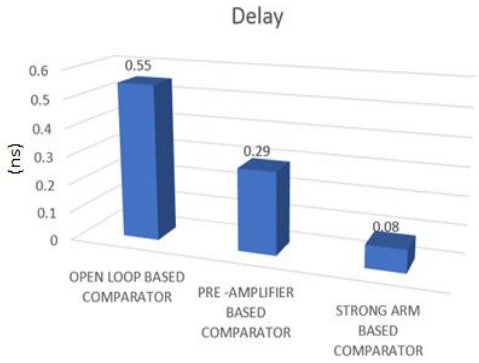


Fig 17. Comparison of propagation delay of Conventional CMOS based several comparators

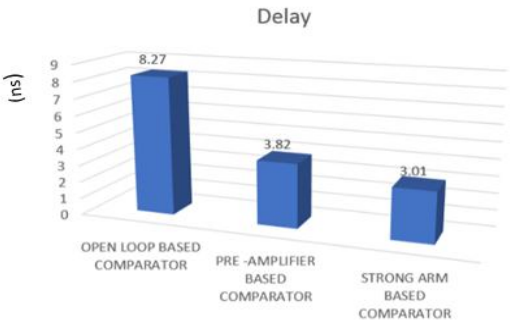


Fig 18. Comparison of propagation delay of Proposed DTMOS based several comparators

V. CONCLUSIONS

In this era of advanced VLSI applications, the property of the comparator largely defines their performances that are employed in various systems. In this paper three comparator designs i.e. open loop based, preamplifier based and strong arm based comparators have been simulated using two technologies i.e. conventional CMOS based and the proposed work of DTMOS technology based to obtain the low power and also high speed parameters. The circuits have been implemented in Cadence Virtuoso tool at 65nm technology and from comparison results it has been proved that the DTMOS based comparator shows a good many advantages over CMOS based comparator in terms of power and delay.

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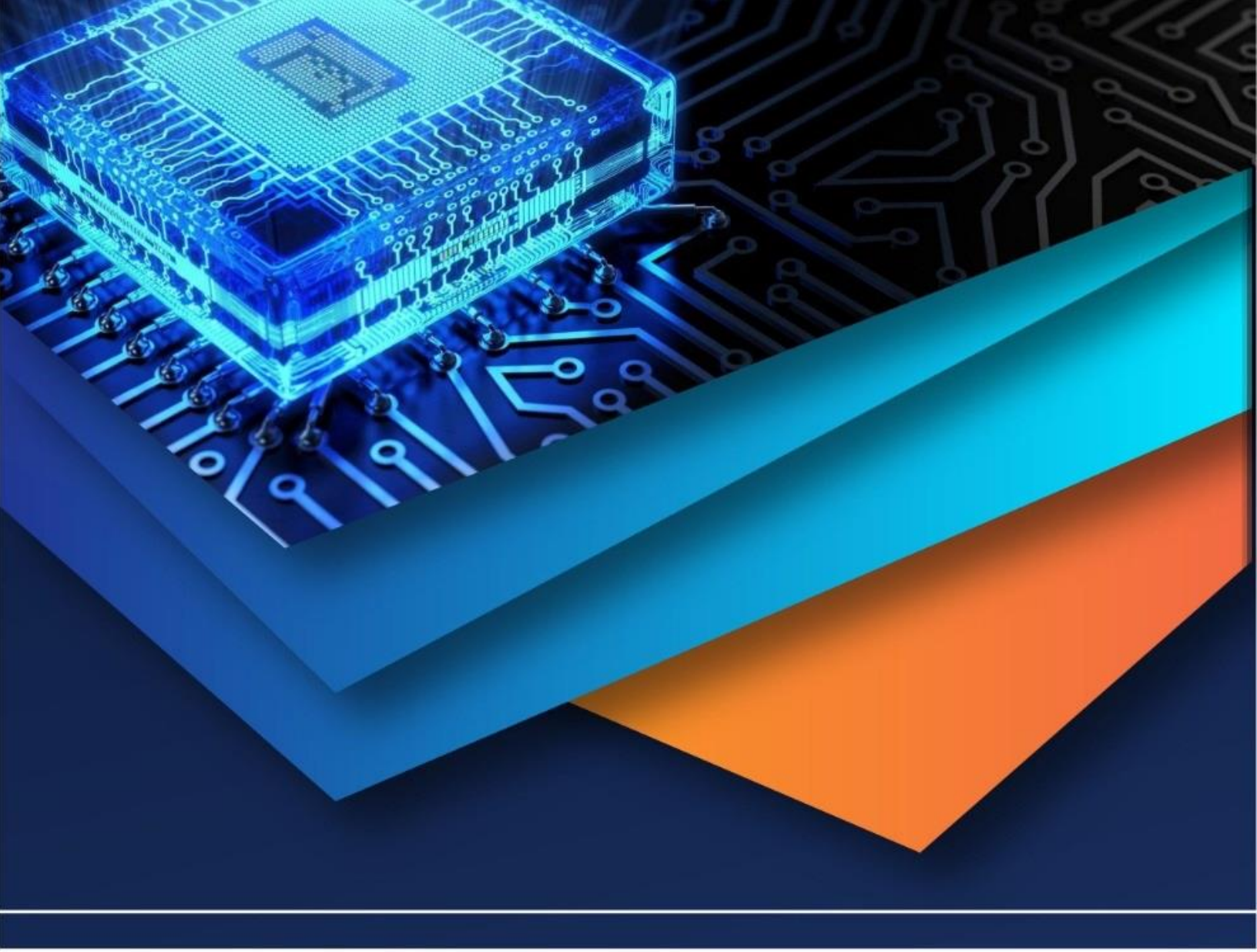

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