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# Multiple Logic Styles for Low Power VLSI

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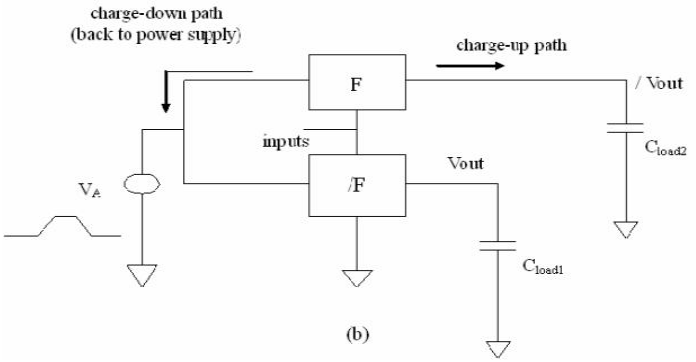
***Abstract:*** ***In this review paper, full adder was designed using CMOS logic, pass transistor logic (PTL), transmission gate logic (TG) styles. We are going to compare adiabatic full adder using ECRL & PFAL logics with conventional designs and they are simulated using Tanner software. It is finding that adiabatic technique is good choice for low power applications in specific frequency range. The power dissipation in conventional CMOS circuit can be reduced through energy recovery principle.***
***Keywords: Adiabatic logic, TGL, PTL, ECRL Adder, PFAL Adder.***

## I. INTRODUCTION

The main objective of this paper is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. In this paper work, a new CMOS logic family called *ADIABATIC LOGIC*, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation [2].

### *A. Adiabatic Process*

The adiabatic switching technique can achieve ,but at the expense of circuit complexity. The adiabatic logic offer a way to reuse the energy stored in the load capacitors rather than traditional way of discharging the load capacitors to the ground and wasting of this energy. It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down.




"Figure.1: Adiabatic Process".

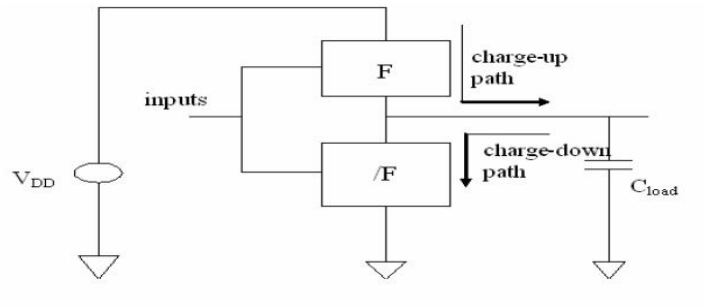
In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems [3].

### *B. CMOS*

The latest technology used for constructing integrated circuits is Complementary metal oxide semiconductor. The technology is being used in various digital and analogy logic circuits such as image sensors (CMOS sensor), data, converters, and highly integrated transceivers for many types of applications.

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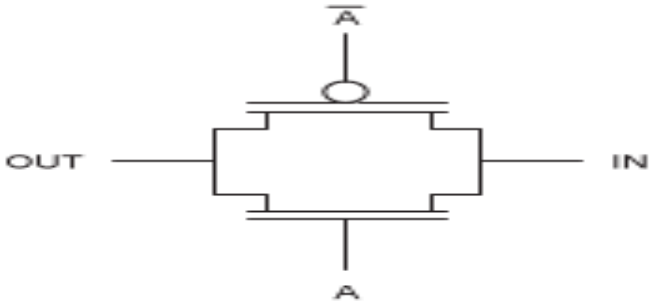

"Figure.2: Conventional CMOS".

It is also known as complementary-symmetry metal oxide–semiconductor (COSMOS) because it uses complementary and symmetrical pairs of both p& n type semiconductor field effect transistor. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power for short duration of time only while switching between on and off states. Also, CMOS devices produce lesser heat in comparison to other forms of logic, e.g., PMOS or NMOS logic[2]. The main reason which made CMOS the most used technology to be The main reason which made CMOS the most used technology to be implemented in VLSI chips is that, it allows large number of logic functions on a chip.

The basic approaches that we used for reducing energy/power dissipation in conventional CMOS circuits include reducing the supply voltages, on decreasing node capacitances and minimize the switching activities with efficient charge recovery logic.

*C. Transmission Gate*

A CMOS transmission gate is constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals. It gives full swing output so, its use give better speed in CMOS circuit but there is no isolation between input and output[7].




"Figure.3: Transmission Gate Logic".

## II. LOGIC STYLE

The CMOS logic circuits are categorised into two categories:- static and dynamic logic circuits. These different logic styles are used according to design requirements such as power consumption, speed and area. In a static logic circuit a logic value is retained by using the circuit states while in a dynamic logic circuit a logic value is stored in the form of charge[7]. Different logic styles can be used to reduce the full-adder such as (regular CMOS [2], Pass transistor logic (PTL)[9],transistor logic (TG)[1], Complementary Pass Transistor Logic (CPL) [4].

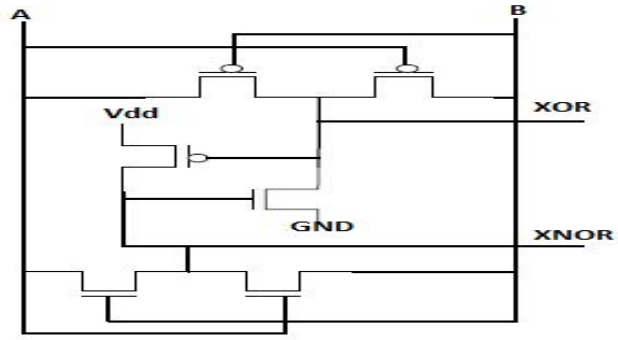
*A. Pass Transistor Logic*

This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input[9].By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease.

In this logic either nMOS or Pmos is sufficient to perform logic operation, so, number of transistors and i/p load decreases and also the Vdd to gnd paths are eliminated [7]. It is used for low power applications. In electronics, pass transistor logic (PTL) describes

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several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages




"Figure.4: XOR and XNOR gate using PTL logic."

*B. ComplementaryPass Transistor Logic (CPL)*

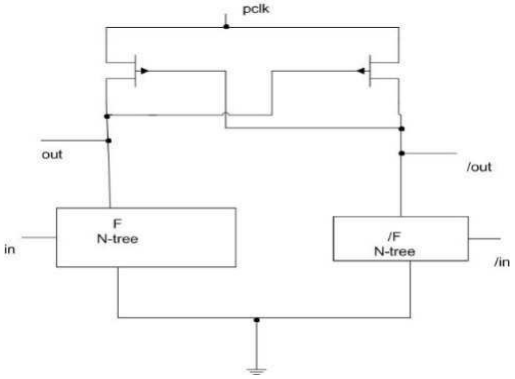
The full adder circuit designed by using complementary pass transistor logic (CPL) has swing restoration ability. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function, which results in smaller number of transistors and input loads especially when NMOS network used.

*C. Adiabatic Logic*

In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS [3]*.The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle.

*D. ECRL Logic*

In the above **"fig 5",** basic structure of adiabatic ECRL logic is shown. In the adiabatic ECRL logic cross coupled PMOS transistors are used for evaluate, precharge and recovery. By using basic structure of adiabatic ECRL logic we can design the any circuit [6]. It consists of two cross-coupled transistors *M1* and *M2* and two NMOS transistors, in the AC power supply *pwr*is used for ECRL gates, so as to recover and reuse the supplied energy. Both *out* and */out* are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. ECRL always pumps charge on the output with a full swing [3]

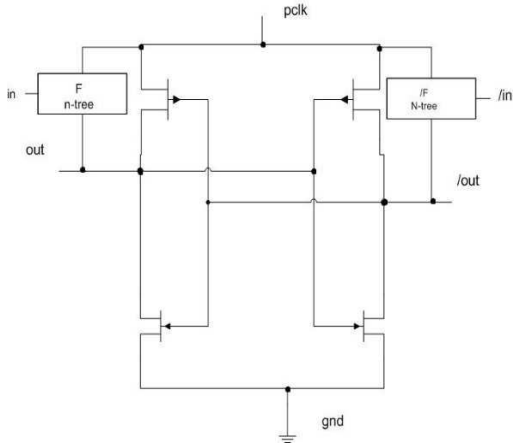



"Figure.5: Basic Structure of adiabatic ECRL logic."

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*E. PFAL Logic*

In the above "**fig 6"**, basic structure of adiabatic PFAL logic is shown. In the adiabatic PFAL logic having two cross coupled pmos transistors are used for evaluate, and precharge. By using basic structure of adiabatic PFAL logic we can design the any circuit. Based on the structure I can designed adiabatic PFAL full adder For designing the adiabatic full adder 4-PMOS,36-NMOS gates are required. In the adiabatic circuits power clock play a Very important role to reduce the power dissipation across the PMOS gates. [6].




"Figure.6: Basic structure of adiabatic PFAL logic"

## III. CONCLUSION

Adiabatic PFAL and ECRL methodology is better as compared to conventional in terms of power dissipation and delay. In adiabatic circuit power clock plays a very important role to reduce the power dissipation during switching process and reuse the some of power by recycling from the load capacitance. Hence the power dissipation across the PMOS gate minimized by using adiabatic technique. Future work for this paper is calculating the figure of merit.

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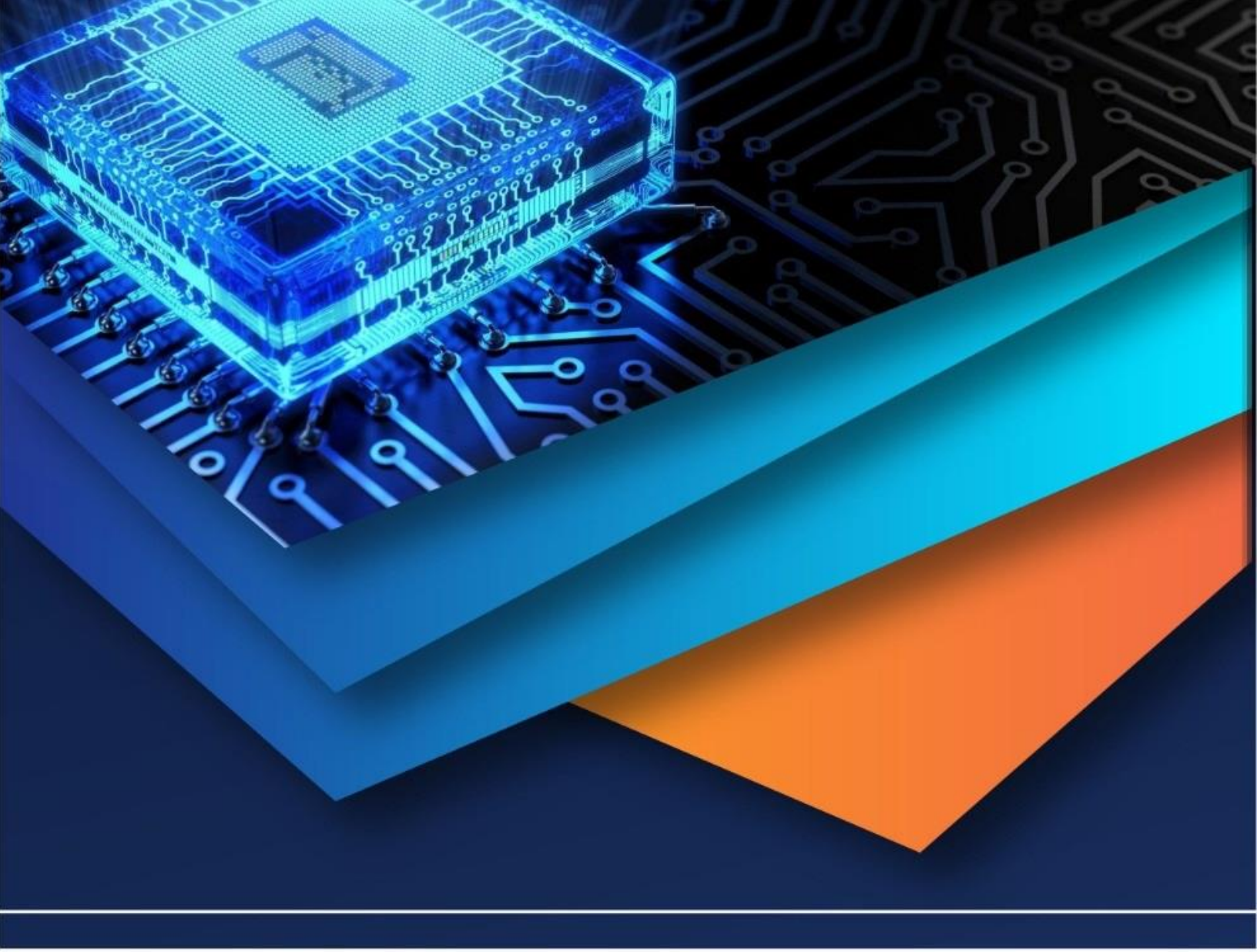
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