iJRASET
International Journal For Research in Applied Science and Engineering Technology

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

**Volume:** 2 **Issue:** IV **Month of publication:** April 2014

**DOI:**

www.ijraset.com

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Vol. 2 Issue IV, April 2014
ISSN: 2321-9653

INTERNATIONAL JOURNA L FOR RESEARCH IN AP PLIED SCIENCE
AND ENGINEERING TECHNOLO GY (IJRASET)

# Efficient Design of Power and Clock network for Large Chip Design Using Energy Recycling Technique

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***Abstract*— This project aim is to develop a low-skew in multigiga hertz clocks circuit in operation with giant digital chips. A capacitance are often charged from the availability then discharged to ground. In giant digital chips quantity of wastage in electrical condenser is high owing to range of connections. Hence we are able to use associate energy use idea to cut back the general power consumption. By this energy use the wastage energy is employed by the opposite a part of the chip. For this energy use integrated clock driver and device network square measure incorporated. With exploitation of multigiga hertz the reduced size obtained within the inductance and electrical condenser while not loss and forty second of energy saving can occur. This idea is enforced by the 180nm cadence tool. We are able to additionally use clock buffer for ordered circuits.***

***Keywords*— Energy Recycling, Multigiga hertz clocks, Clock Driver,Buck Converter and Electrical Condenser**

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## I. INTRODUCTION

The energy consumption in massive chips area unit stick with it increasing and wish of the massive chips with skinny gate oxides area unit takes a necessary half within the style and applications.

It will cause increasing within the frequency usage. In the integrated clock and buffer construct [1] is well and reducing the facility. However in massive chips it'll increase the chip space as a result of we've to done multiple range of integrated clock driver and buffer network.

So we have a tendency to area unit within the like of answer to the present drawback. To deal with and clear this tough in massive chips our driver/converter circuit with energy recovery idea area unit all right use.

To reduce the clock energy in circuits heap of inventions keep it up going a number of area unit, double edge triggered flip-flops, low-swing signalling ,clock gating, adiabatic change [2], and resonant duration [3], [4].

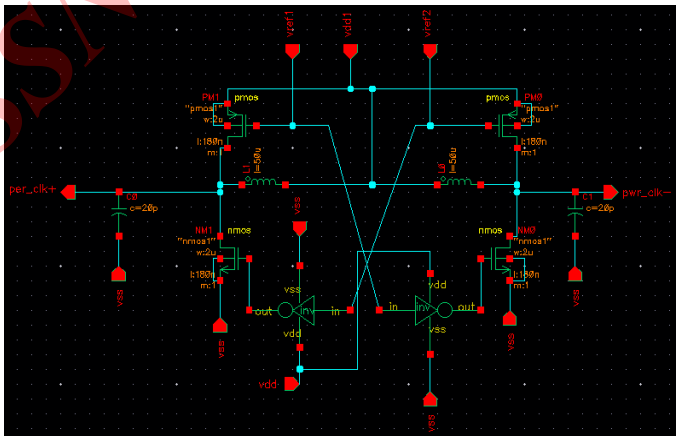


Fig.1 Existing method clock driver schematic

Compare to the on top of strategies our idea will scale back the general energy. for recover and redeploying this electrical phenomenon hold on energy, we have a tendency to develop a unified buck convertor circuit and clock driver. one in all the most advantage is on chip recover voltage is dissent from the ability providing with low.

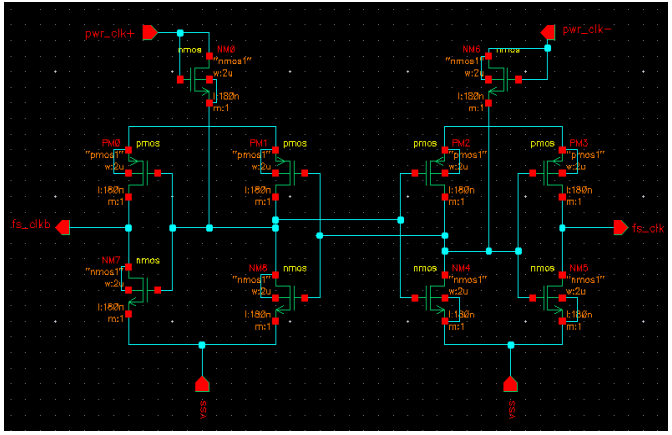


Fig.2 Method of clock buffer schematic

We can also use this clock buffer schematic for sequential circuits.

To accelerate our goal shift frequencies are increasing steady to shrink the scale of the specified passive output filters. During this approach clock node is directly use since justification of high frequency, high capacitance and power overhead is occurred.

The clock driver and a device are similar however each act as a tapered chain electrical converter to drive giant final electrical converter.

The vital distinction is that clocks usually maintain a hard and fast duty cycle, whereas duty cycle to output voltage varies by the device. to supply a dc output undulation with low ripple device attach an oversized lc output filter however clock output may be a top quality sq. undulation.

Usually giant chips/circuits are employing a multiple clock buffer and driver circuits, rather than employing a giant network of it. Therefore our approach is doing an honest issue in in multiple clock buffer and driver circuits. it will scale back the general power consumption and want of multiple clock circuits.

Gating is one in all the clock ideas however it needs native clock that's known as gaters. Our convertor covers roughly 1mm*mm of space with native gated regions. from the fig one and a couple of we are able to simply grasp the sensible chip space, power and delay increasing whereas they implement in massive chips. our project is formed a compatibility and lap between dc-dc convertor and change converters.

## II. SIMPLIFIED CIRCUIT

A converter diagram shown in fig 3. The delay component is introduced to supply zvs throughout the high to low transition attributable to great amount of capacitance cclk.

If supply drain voltage reaches 0v, zvs saves energy if mn is turned on. The operation of buck convertor by average pulse dimension modulated voltage through an occasional passive filter. the capacitance of a clock node and stray capacitance of mn and mp embody within the overall capacitance cclk.

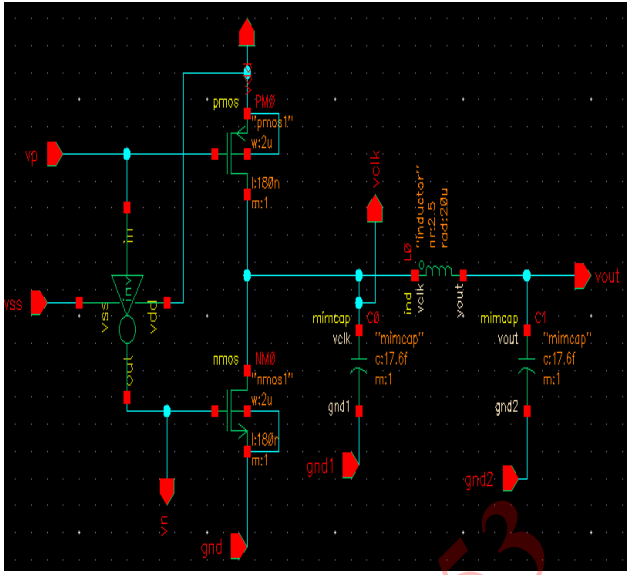


Fig.3 Proposed clock driver/converter schematic

The idealised temporal arrangement diagrams showed the operation of the circuit. clock duty d, switch amount tsw , and zvs delay time tdelay square measure calculated by cadence output waveforms.

## III.OPERATION

*A) Phase -1*

Time limit- zero to D×Tsw the load is drive via radio frequency and Cf, charged through Cclk Mp. The voltage across the inductance is constants whereas current increrserses in it.

*B) Phase -2*

Tile limit- D×Tsw to D×Tsw+Tdelay this can be for energy utilization, Mn and Mp each square measure off throughout this point, radio frequency because the inductance current cannot discontinuous dead by this fast drop of Vclk is achived. Cclk would be discharged to ground at time D×Tsw through mn if no delay is gift.

*C) Phase -3*

Time limit- tD×Tsw+Tdelay to Tsw This section can act once voltage across Mn is near zero. However Mn offer virtual ground at node Vclk whereas conducting in rerverse. Whereas supply drain voltage usually near zero, Zvs operation occurred once Mn is turned on, thereby reducing dynamic power loss. Mp is turned on –ve inductance current charging in C clk. No ZVS operation is enforced for Mp. The device forever operates in physical phenomenon mode.

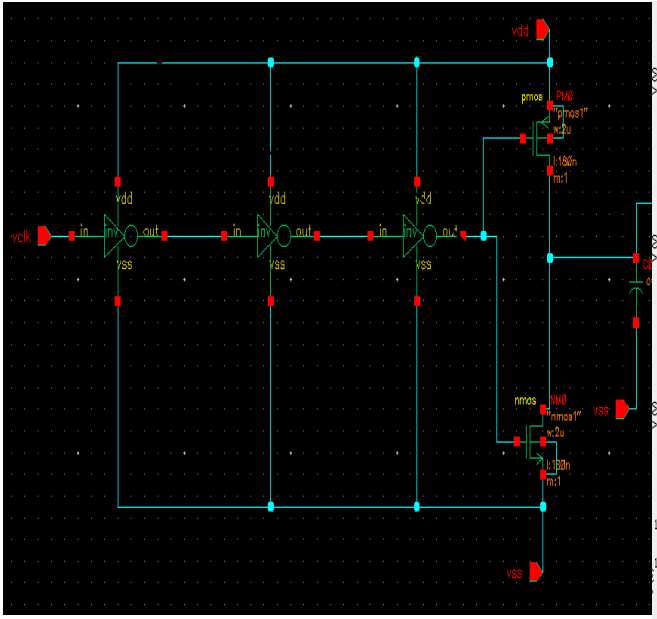


Fig.4 Reference clock driver

*D) Timing Diagrams*

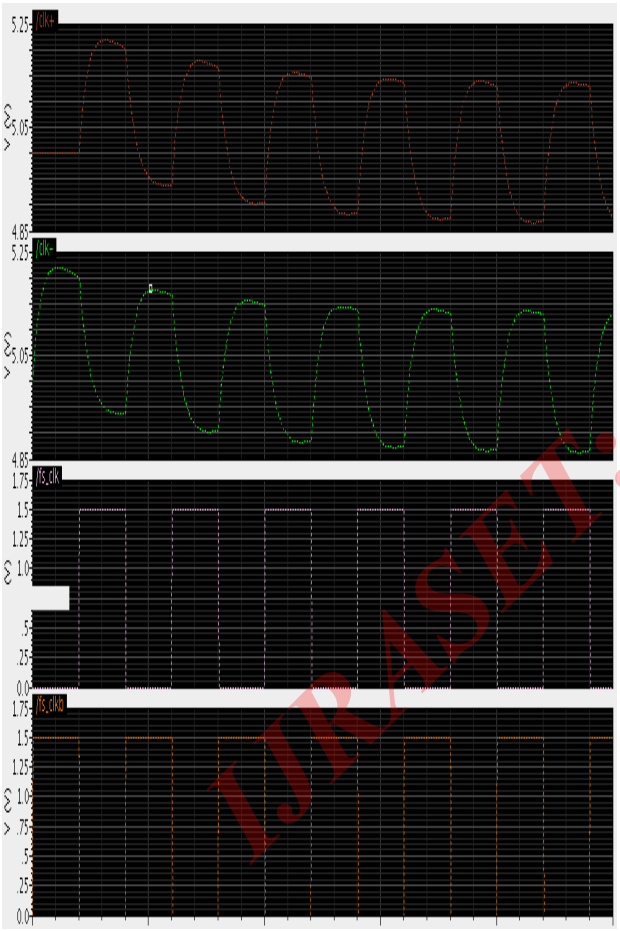


Fig.5 Timing diagram

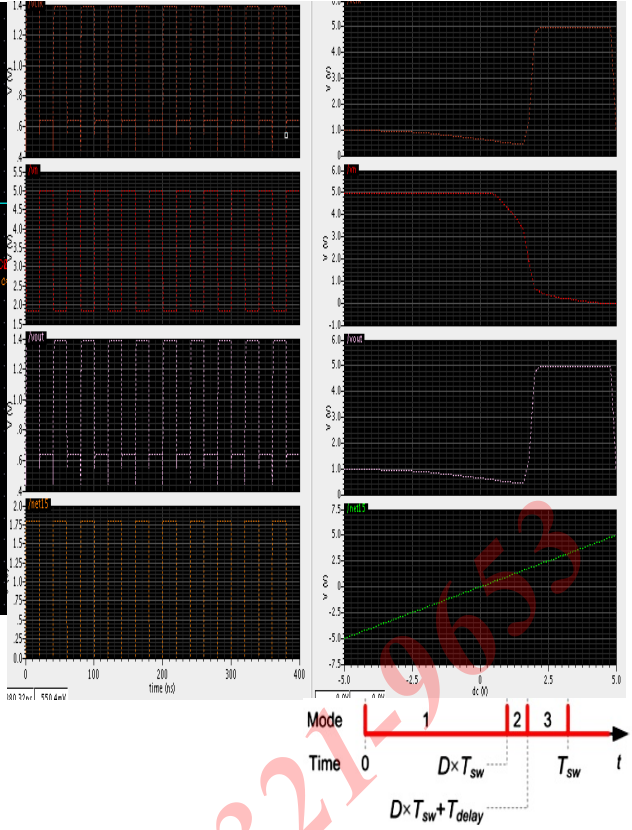


Fig.6 Proposed Timing Diagram

TABLE I

Comparison Statement of Inverter with IPDCN

| System Characteristics | Existing System | Proposed System |
|---|---|---|
| Power | 581mw | 289mw |
| Delay | $-203.21*10^{-12}$ s | $-143.1*10^{-12}$s |
| Supply Voltage | 1.8v | 1.3v |

In the existing methodology so as to satisfy high current needs, many LC drivers ought to be drive differential blocks to perform properly.

This will increase the realm overhead related to the inductors. We will implement inductors on prime to cut back the realm overhead however it'll cause reduction in quality issue.

From this idealized diagrams we will simply calculate the temporal arrangement values. The comparison between the projected and existing theme shows that reduction in overall power, chip space and clock amount minimization area unit achieved. The table higher than shows that power delay and provide reduction.

We have a tendency to additionally get decreasing within the space compare to the prevailing methodology. To calculate the realm and different details accurately layout implementation ought to want.

## III. CONCLUSIONS

Merging the practicality of the change dc–dc device with the clock driver energy recovery from a clock load has been shown to be doable. Integrated clock driver and device circuit employment the clock energy by using the clock capacitance as a ZVS capacitance for the most electrical converter.

The outputs filter taking solely atiny low space of chip calculable to be 15 of the practical island space, such united clock and dc–dc converters. The clock driver and device to share the tapered driver chain, vital energy is achieved. Retentive the quick change edges necessary for a high-quality sq. wave clock wave shape as a result of the tapered driver used here provides enough drive to the most MOSFETs.

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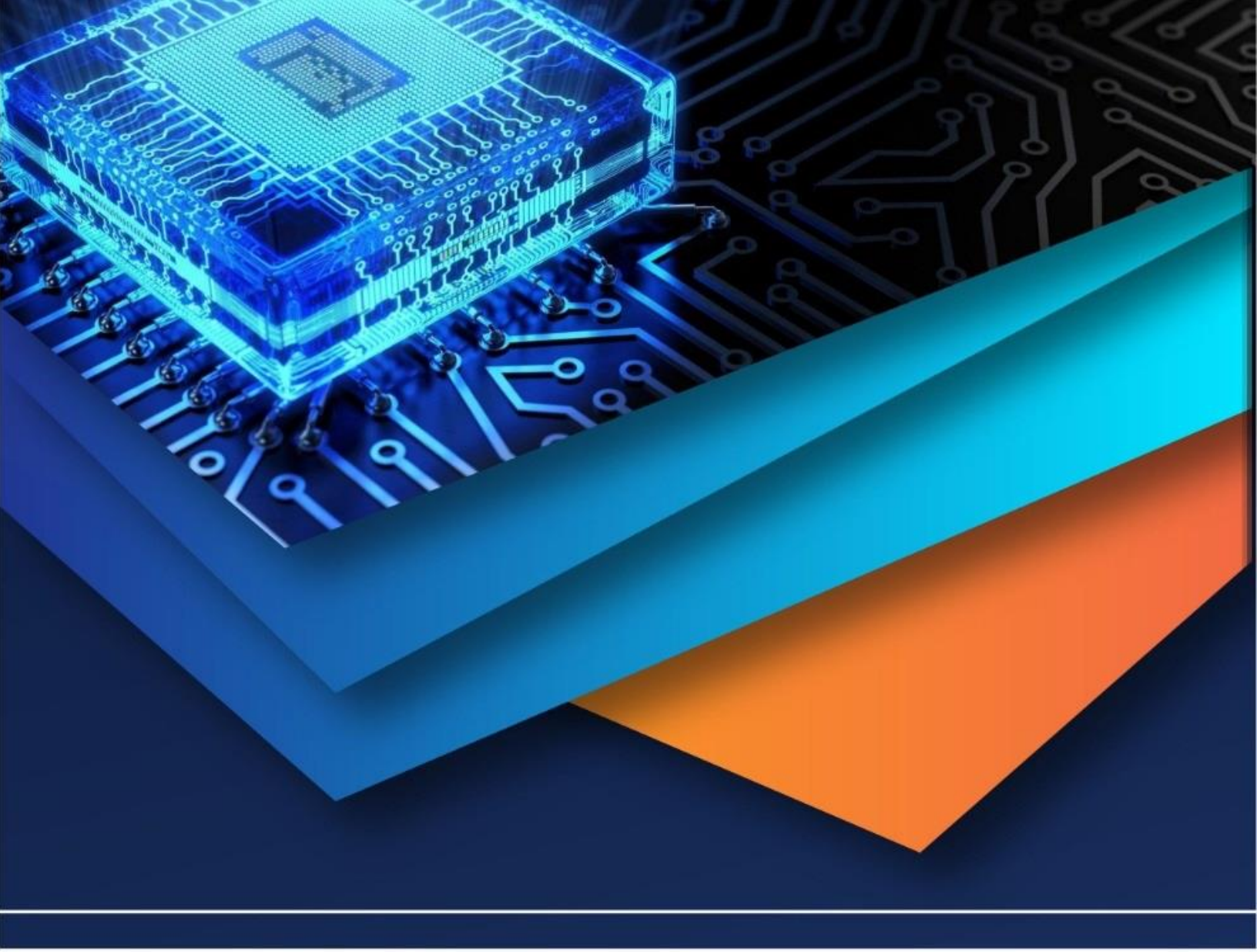

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