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Low Latency Corrective Feedback Algorithm for Binary Compressed Sensing

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Abstract: ***Compressed sensing takes advantage of the redundancy in many interesting signals. Compressed sensing typically starts with taking a weighted linear combination of samples also called compressive measurements in a basis different from the basis in which the signal is known to be sparse. In the existing system, low density parity check codes are used for the process of predicting the compressed sensing scheme through metric matching. The proposed architectures offer high frequency of operation and low reconstruction time when compared to the state-of-the-art designs. Specifically, the 65-nm ASIC realization operates at a maximum frequency of 500 and 666.67 MHz and offer a reconstruction time of 6.3 and 4.7 ns, respectively, for a 64 × 256 deterministic measurement matrix. In the proposed system, design of low latency corrective feedback algorithm (LLCF) is developed. The algorithm is focused on correcting the binary dead codes and utilizes it to self-repair through a corrective iteration process. The system, performs better compared to the existing interval passing algorithm in terms of latency. These codes are encrypted through LDPC encoder. The proposed system is simulated in MODELSIM and implemented in XILINX ISE.***

Keywords: Compressed sensing, low density parity check, interval passing algorithm, modelsim, Xilinx ISE

I. INTRODUCTION

Compressed sensing (CS) has drawn considerable attention in recent years. Introduced by Donoho, it is a technique for reconstructing sparse signals from a small set of measurements. Let x ∈ RN be a K-sparse signal with at most K nonzero entries, K, N. Let A ∈ RM×N be a measurement matrix which maps x into a smaller measurement vector y ∈ RM as given by the following equation: y = Ax. One method of recovering x from y is to find x with the smallest l0-norm, which is a NP-hard technique. Another method is to find x with the smallest l1-norm. The l1- norm minimization based on linear programming (LP) for CS, called basis pursuit (BP), has an excellent performance in the recovery of the sparse signals. The high complexity of BP makes it impractical when the matrix dimension is large. There exist relatively less complex greedy algorithms such as orthogonal matching pursuit (OMP), CoSaMP, iterative hard thresholding (IHT) which iteratively compute an approximation to the original signal. Several hardware realizations of OMP have been reported in the literature, which exhibit trade off between complexity and accuracy.

II. EXISTING SYSTEM

In the existing system, low density parity check codes are used for the process of predicting the compressed sensing scheme through metric matching. The proposed architectures offer high frequency of operation and low reconstruction time when compared to the state-of-the-art designs. Specifically, the 65-nm ASIC realization operates at a maximum frequency of 500 and 666.67 MHz and offer a reconstruction time of 6.3 and 4.7 ns, respectively, for a 64 × 256 deterministic measurement matrix.

A. Drawbacks of Existing System

1) Processing delay is more.
2) Complex steps involved.

III. PROPOSED SYSTEM

The algorithm focuses on correcting the binary dead codes and utilizes it to self-repair through a corrective iteration process. The system performs better comparing to the existing interval passing algorithm in terms of latency. These codes are encrypted through LDPC encoder. The proposed system is simulated in MODELSIM and implemented in XILINX ISE.

1) Advantages of proposed system
2) Low Latency and Low Complexity

A. Block Diagram of Proposed System

Figure 1: Concept of the Proposed system

The input data sequence is provided and the corrective feedback mechanism corrects the incoming signals and based on the sparsity of the signal, only a portion of the signal is concentrated. The signal is encoded using the Low Density Parity Check mechanism and sent for compressed sensing. After the signal is compressed, and the performance measurement of the signal is measured using get metrics. Then finally, the noise is removed from the signal. This process is explained in the figure 1. Let x=[x1 ,x2,…..xn] be a k-sparse signal with k non zero entries k<<N. In BCS, each entry xi of vector x is binary valued, that is xi belongs to {0,1}. The sparsity of the given signals are checked. For each sparsity atleast 100 random signals are generated and 50 reconstruction iterations takes place.

IV. RESULTS AND DISCUSSION

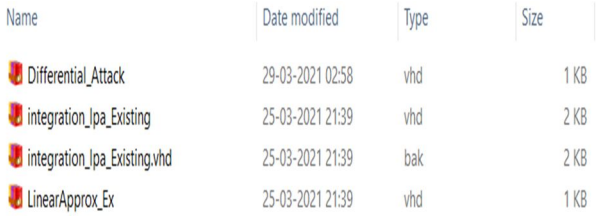
The software that is used in the project is mainly Modelsim 6.3G altera and Xilinx ise.

A. Creation And Simulation Of Attack Files

The attack files are programmed and executed in modelsim. After the computation and execution of these attack files, they are dumped into the hardware for further operations. Two attack files are coded namely,

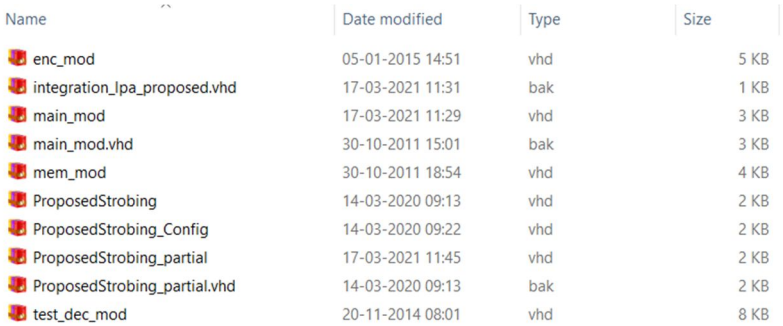
1) Linear attack
2) Differential attack

Are shown in the figure 3. Similarly the proposed system files are also created and simulated as shown in the figure 4.



Name	Date modified	Type	Size
Differential_Attack	29-03-2021 02:58	vhd	1 KB
integration_lpa_Existing	25-03-2021 21:39	vhd	2 KB
integration_lpa_Existing.vhd	25-03-2021 21:39	bak	2 KB
LinearApprox_Ex	25-03-2021 21:39	vhd	1 KB

Figure 3 Attack files



Name	Date modified	Type	Size
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main_mod	17-03-2021 11:29	vhd	3 KB
main_mod.vhd	30-10-2011 15:01	bak	3 KB
mem_mod	30-10-2011 18:54	vhd	4 KB
ProposedStrobing	14-03-2020 09:13	vhd	2 KB
ProposedStrobing_Config	14-03-2020 09:22	vhd	2 KB
ProposedStrobing_partial	17-03-2021 11:45	vhd	2 KB
ProposedStrobing_partial.vhd	14-03-2020 09:13	bak	2 KB
test_dec_mod	20-11-2014 08:01	vhd	8 KB

Figure 4 Proposed system files

The hardware used in this project is XILINX-XC9572XL based CPLD trainer kit is shown in the figure 5.

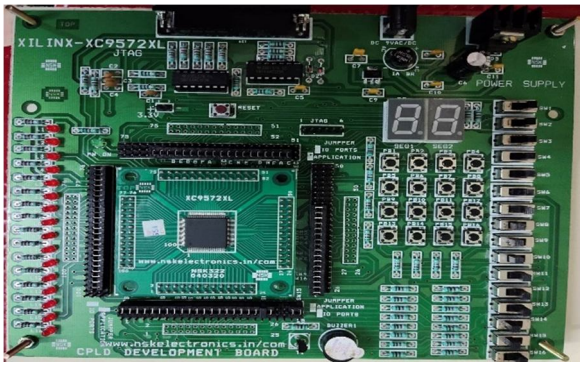

Figure 5 XILINX – XC9572XL based CPLD trainer kit

The proposed VLSI architectures of IPA and LLCF algorithms are implemented both in ASIC and FPGA environments. Since there are no prior implementation for BCS in the literature, we compare the proposed designs with implementations of OMP from the literature. The sparsity of an LDPC matrix which is equal to 64. The results are compared with those of some instances of existing related architecture. The computations involved are all integer operations and the hardware consumption of the proposed designs independent of the sparsity level K unlike OMP. Since the proposed architecture is fully parallel, each iteration takes a single clock cycle. So, the number of clock cycles the design takes to reconstruct the signal is equal to the number of iterations.The waveform of the existing method with the IPA algorithm is being synthesized. Thus this output is result of the existing method have less accuracy and require more time.Thus, the waveform of the binary compressed sensing has been synthesized with the help of the MIPA the time efficient and less complex result have been obtained.

Thus from the below given figures 6 and 7 it can be inferred that the time interval of the waveforms in the proposed system signals are significantly reduced when compared with the existing system signal.

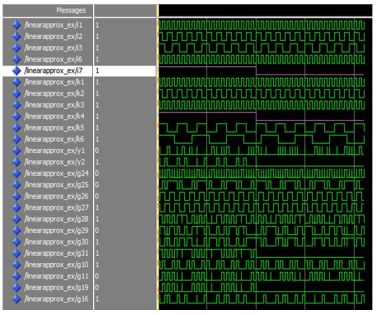

Figure 6 Result waveform of existing system

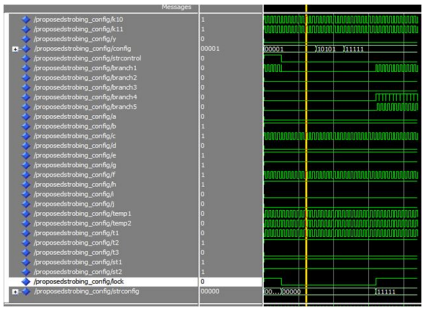

Figure 7 Result waveform of proposed system

V. CONCLUSION

VLSI architecture to realize IPA for BCS has been proposed. The algorithm is further modified to reduce its complexity for which VLSI architecture has been developed. The recovery performance of the proposed MIPA algorithm has been demonstrated on a standard LDPC measurement matrix. The proposed designs are implemented on both ASIC and FPGA platforms, demonstrating their high frequency of operation and low reconstruction.

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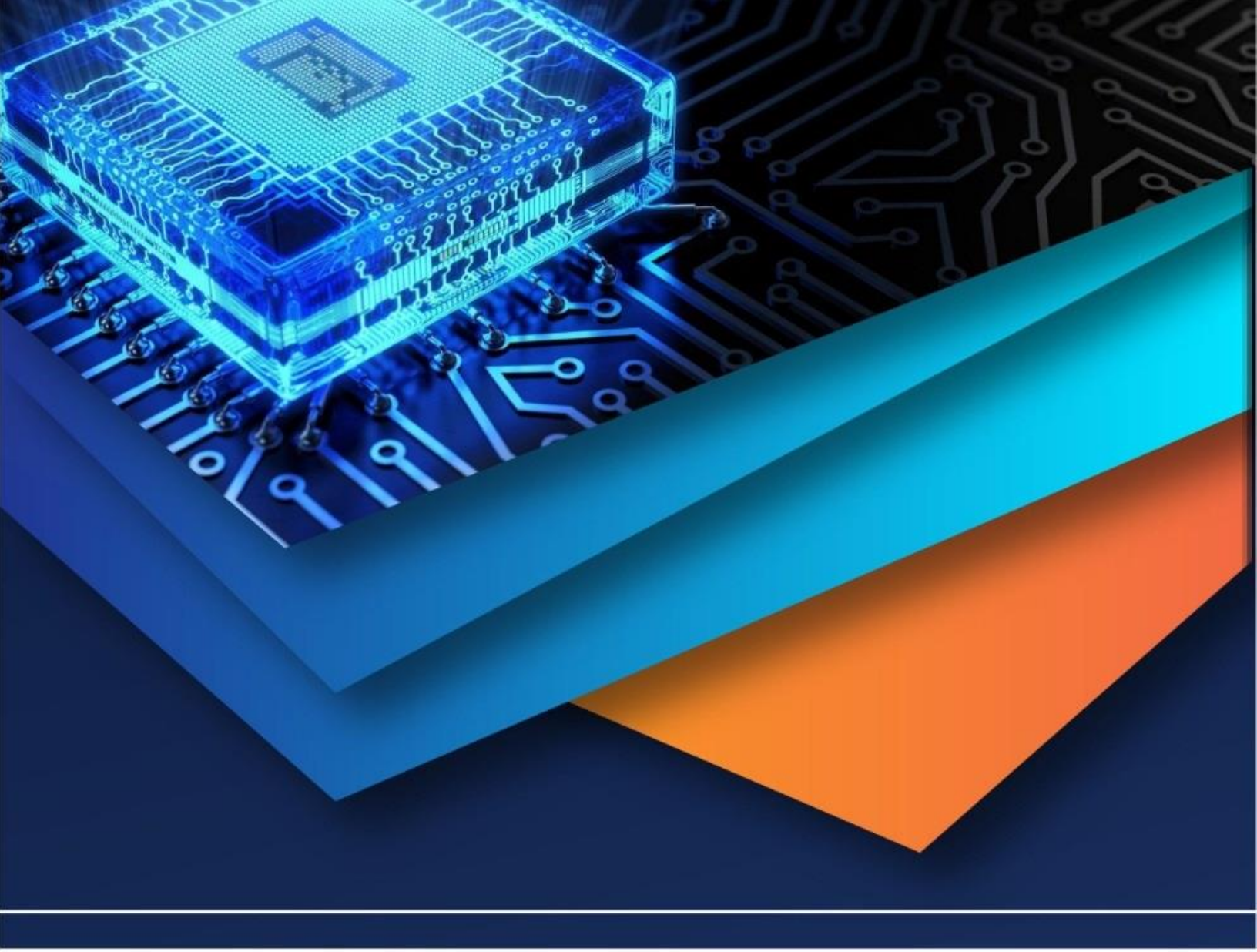

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