iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 3 **Issue:** X **Month of publication:** October 2015

DOI:

www.ijraset.com

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Volume 3 Issue X, October 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Fuzzy Controlled Multi Carrier Based Voltage Balancing Regulator for Five-Level Diode Clamped Inverter to Mitigate Switching Losses

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Abstract*— Multi-level inverters have drawn attention in the recent years when compared to conventional bridge converters to achieve reduced harmonics, high-voltage and high-power capability but switching loses are added on because of increased device count. Many modulation techniques were employed to reduce switching losses. This paper presents design of simple fuzzy controlled neutral point voltage [NP] regulator for five-level DCMLI using a carrier based closed-loop control technique. The regulator principle is based on adding continuous variable offset voltage which rectifies the midpoint potential of the dc bus. Aside from maintaining dc-bus voltage balance the proposed regulator leads to a significant decrement in the voltage ripple at the Neutral node point, results the minimization of the dc-bus capacitance required. It also cutbacks the switching losses of inverter by placing the "no-switching" zone in each and every half cycle of the fundamental voltage wave. The circuit is simulated in Matlab/Simulink the results obtained are compared with that of the three-level DCMLI and it is shown that the effective balancing in line voltage & reduced THD is achieved.

Keywords*— Multilevel inverters, Neutral point potential [NPP], Total harmonic distortion [THD], Fuzzy logic controller, Sinusoidal Pulse width modulation (SPWM).

I. INTRODUCTION

Nowadays Multilevel inverters have been found wide spread acceptability in medium/high voltage, high power applications like Steel rolling mills and other variable speed drive with improved power quality of the supply. Despite of many advantages like harmonic reduction, reduced stress across switching device without problematic series-parallel connections. Neutral point clamped [NPC] inverter has downside of the unbalanced voltages across dc link capacitors because of non-identical properties of the dc link capacitors provided by manufactures [1], [3]. The imbalance in dc link voltage leads to disturbance in the Neutral point [NP] voltage and needs inflated dc bus capacitance; it also distorts the output voltage of the inverter. To operate the circuit accurately a simple control technique is used and voltage across dc bus capacitance was shared equally. It has been proposed that maintaining the voltage across dc bus balance by means of two ways one is of voltage balancing based upon the modification of hardware circuitry which changes the charging and discharging of dc link capacitors [3]-[10]. Second way of voltage balancing is based upon modifying the PWM technique to the inverter [13, [15], [18].

A closed loop control technique which reduces the harmonic content and maintains balanced voltage across neutral point is presented in this paper. Several carrier and SVPWM based strategies have been introduced for the modulation of these inverters. In the SVPWM technique [5]-[15], redundant switching states of the inverter are used for controlling the NPP. Moreover the relationship between NPP and inverter switching states is extremely sophisticated, so it's tough to balance the NPP accurately based on redundant switching state selection.

Another issue in multilevel inverters is switching losses. Recent advance in power semiconductor technology made a possible to incorporating the high frequency switching modulation techniques in power inverters to decrease the harmonic content in output voltage [18]-[21]. As a result switching frequencies are increased to reduce the filtering constraint in almost all the inverter topologies which increases the losses, thus dipping system efficiency. A soft-switching technique for multilevel inverters was proposed to decrease the losses. Various carrier based PWM techniques [11] such as constant switching frequency, variable switching frequency and phase shifted PWM are there which can reduce the THD and improves the output voltages.

Multilevel inverters have become an effective and practical solution for increasing power capability & reducing harmonics of AC load. The main multilevel inverters are classified into three categories they are diode clamped inverter, flying capacitor inverter, cascaded inverter. In all these DCMLI is widely used topology. In three phase inverters, the number of main switches of each

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Volume 3 Issue X, October 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

topology is equal. However there would be a limitation to application beyond four-level DCMLI for the reason of reliability and complexity considering dc-link balancing & the prohibitively high number of clamping diodes, because it works on concept of diodes to limit voltage stress across the power devices connected to the various dc levels. Three-phase five level DCMLI dc-bus consists of four capacitors which are connected to the neutral point at centre, the order of numbering of the switches for phase A is $S_{a1}, S_{a2}, S_{a3}, S_{a4}, S'_{a1}, S'_{a2}, S'_{a3}, S'_{a4}$. similarly for the remaining two phases.

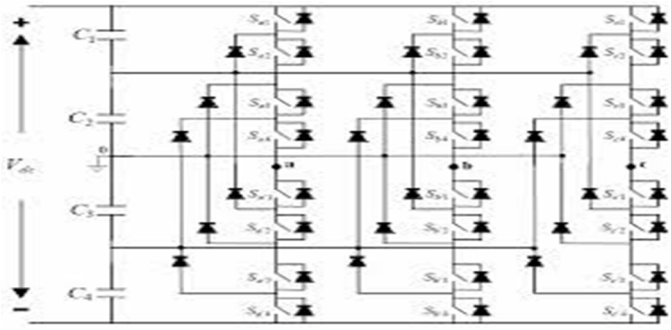


Fig.1.Structure of three-phase Five-level diode clamped inverter

TABLE 1
Switching states of Five-Level Diode clamped inverter

Sa1	Sa2	Sa3	Sa4	Sa1'	Sa2'	Sa3'	Sa4'	Van
1	1	1	1	0	0	0	0	Vdc/2
0	1	1	1	1	0	0	0	Vdc/4
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-Vdc/4
0	0	0	0	1	1	1	1	-Vdc/2

This paper proposes the design, simulation of a carrier-based NPP regulator for a three-phase five-level diode clamped inverter employing a sine-triangle modulator in conjunction with a closed-loop controller. A continuous variable offset voltage regulates the midpoint potential of the dc bus and corrects any existing imbalance in the dc-link. A real time carrier-based capacitor voltage balancing algorithm is proposed which is easier to be implemented without the need of information about the load power factor angle.

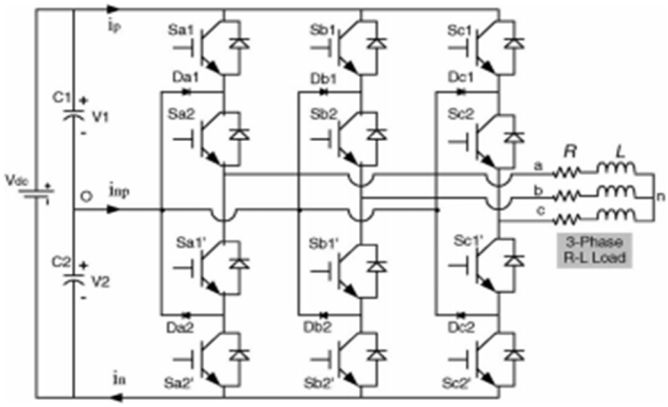


Fig.2. Structure of three-phase three-level diode clamped inverter

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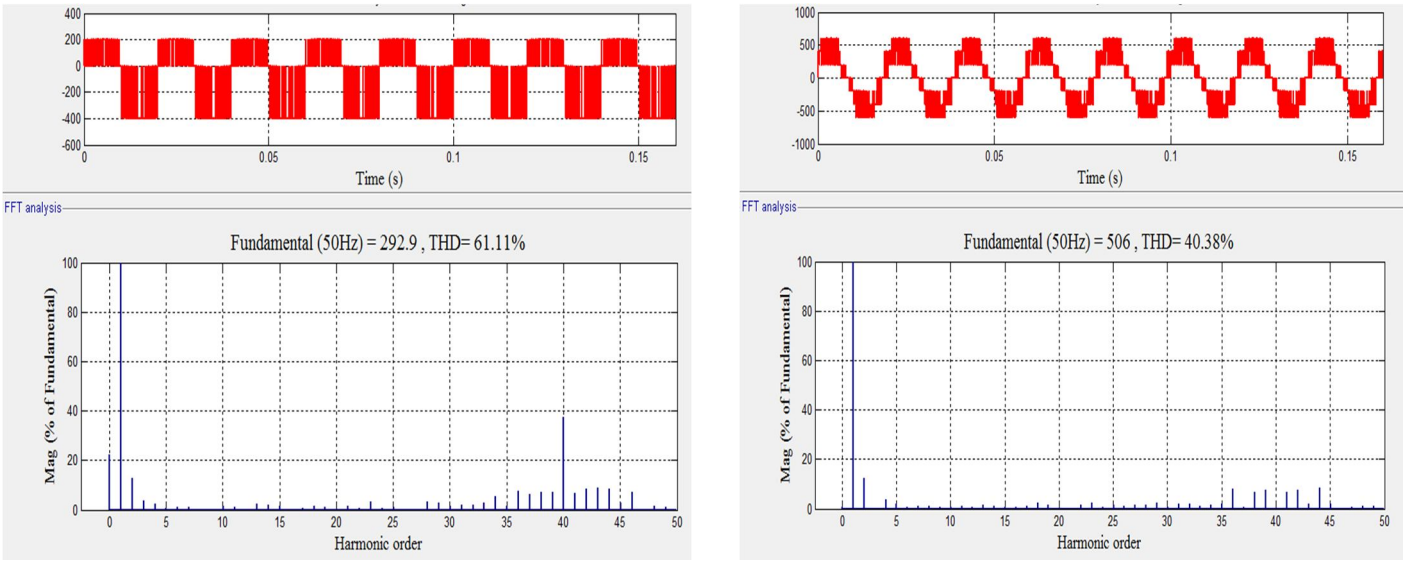
TABLE 11
Switching States of Three-Level Diode-Clamped Inverter

Sa1	Sa2	Sa1'	Sa2'	Switching States	Output Phase Voltage(V)
1	1	0	0	+	+Vdc/2
0	1	1	0	0	0
0	0	1	1	-	-Vdc/2

The novelty of the proposed NPP regulator is in the determination of the magnitude of offset voltage. This not only regulates the NPP but also reduces the output voltage and current harmonics of the inverter, which effectively reduces the losses of inverter without any complex mathematical expressions, as in SVPWM based techniques by suitably modifying the modulating signal. Section II gives the effects of unbalanced dc-link voltage and NPP variations need to balance it. Section III presents the basic model of the inverter and regulator with guidelines for design of the NPP regulator. Simulation results are proposed in Section IV.

II. NEED OF NEUTRAL POINT BALANCING

Fig 2 shows the structure of the Three-level diode clamped inverter and TableII gives the switching sequence to generate the Three-level output voltage for phase "A". Due to unbalanced dc-link (i.e. unequal voltages across two dc-link capacitors), PWM inverter output voltage and current waveforms get distorted.



(a) (b)

Fig.3. Phase voltage and line voltage with large imbalance at dc-link. (a) Phase voltage. (b) Line voltage.

Voltage stress on switching devices also increases. If the voltage imbalance across dc-link capacitors is excessive, it may cause failure of devices. Therefore NPP control is necessary without sacrificing the harmonic performance of the inverter. Fig.3 (a) and (b) shows the waveforms and harmonic spectrums of phase voltage and line voltage under burst condition of large imbalance at dc-link with Vdc1=200V and Vdc2=400V. Under this condition, the dc component and even-order harmonics are more significant which are dangerous for drive and other applications.

Table III gives the effect of dc-link imbalance condition with a total dc-link voltage of 600V. For this study, the dc link was intentionally made unbalanced.

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Volume 3 Issue X, October 2015
ISSN: 2321-9653
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TABLE III
EFFECTS OF DC-LINK IMBALANCE (VDC=600V)

Vdc1 (Volts)	Vdc2 (Volts)	% THD Line Voltage
200	400	40.38%
210	390	39.54%
220	380	38.64%
230	370	37.83%
240	360	37.12%
250	350	36.52%
300	300	35.01%
350	250	36.95%
400	200	41.31%
450	150	47.63%
500	100	55.22%

It is clear that the line voltage THD has the minimum value for the balanced dc link and they are increasing with increased unbalancing.

III. DESIGN OF CLOSED LOOP CONTROL TECHNIQUE FOR NPP REGULATOR

The main issues of concern in devising a control strategy for a three-phase NP-clamped inverter are follows:
Ensuring dc-link capacitor voltage balancing and regulating dc-link voltage, Minimization of inverter voltage and current harmonics, ensuring less and uniform switching stress on switching devices. Results in increased switching losses.
It consists of both a dc-link voltage control loop and a load voltage control loop. Three-phase load voltages are sensed and converted into a per-unit system. These per-unit voltages are converted into dqo-axis using the following three-phase to two-phase conversion:

$$V_d = \frac{2}{3}[V_a \sin(wt) + V_b \sin(wt - 120^0) + V_c \sin(wt - 240^0)]$$

$$V_d = \frac{2}{3}[V_a \cos(wt) + V_b \cos(wt - 120^0) + V_c \cos(wt - 240^0)]$$

$$V_o = \left[\frac{V_a + V_b + V_c}{3}\right] \quad (1)$$

These dqo voltages V_{dqo} are compared with preset values of dqo voltages. It results in voltage error which is processed through a PI controller to generate two axis command signals are synthesized using the following two-phase to three-phase conversion:

$$V_a = [V_d \sin(wt) + V_q \cos(wt) + V_o]$$

$$V_b = [V_d \sin(wt - 120^0) + V_q \cos(wt - 120^0) + V_o]$$

$$V_c = [V_d \sin(wt - 240^0) + V_q \cos(wt - 240^0) + V_o] \quad (2)$$

These are the reference sinusoidal modulating signal $V*_{abc}$ the amplitude of modulating index m is defined as

$$m = \sqrt{Vd^2 + Vq^2} \quad (3)$$

From the dc voltage loop difference between two dc-link voltages (i.e.$V_{np} = V_{dc1} - V_{dc2}$) is calculated and the error is processed through PI controller. Then the variable offset voltage V_{off} is calculated in the offset calculator the frequency of V_{off} is three times the fundamental frequency.

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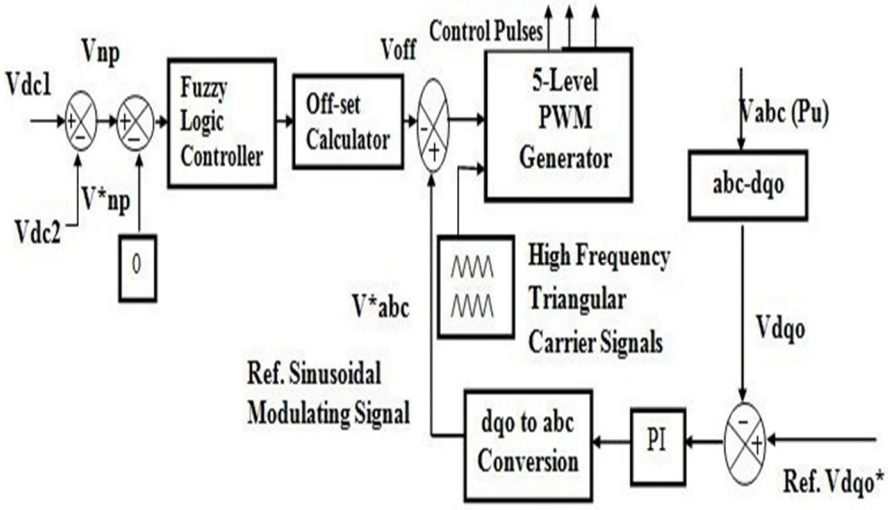


Fig.4.Control scheme for proposed closed loop PWM technique

The variable offset voltage signal determined is subtracted from the reference modulating signal ($V*_{abc}$) resulting a new modulating signal to be compared with high frequency triangular carrier signals of "5-Level PWM Generator" to provide the control signals for the insulated-gate bipolar transistors (IGBTS) of the Five level inverter.

IV. FUZZY LOGIC CONTROLLER

In a fuzzy logic controller, the control action is determined from the evaluation of a set of simple linguistic rules. The development of the rules requires a thorough understanding of the process to be controlled, but it does not require a mathematical model of the system. The objectives include excellent rejection of input supply variations both in utility and in generating system and load transients. Expert knowledge can also be participated with ease that is significant when the rules developed are intuitively inappropriate. The rule base developed is reliable since it is complete and generated sophistically without using extrapolation. In this project, fuzzy control is used to control the firing angle for the switches of the inverter. In this design, the fuzzy logic based NPP regulator has two inputs 'error' and 'change in error' and one control output. Firstly the input values will be converting to fuzzy variables. This is called fuzzification. After this, fuzzy inputs enter to rule base or interface engine and the outputs are sent to defuzzification to calculate the final outputs. These processes are demonstrated in Fig. Here seven fuzzy subsets have been used for two inputs. These are: LP (large positive), MP (medium positive), SP (small positive), ZE (zero), SN (small negative), MN (medium negative) and LN (large negative). We use Gaussian membership functions and 49 control rules are developed, which are shown in table 1.

Fuzzification: It is the process of representing the inputs as suitable linguistic variables .It is first block of controller and it converts each piece of input data to a degree of membership function. It matches the input data with conditions of rules and determines how well the particular input matches the conditions of each rule.

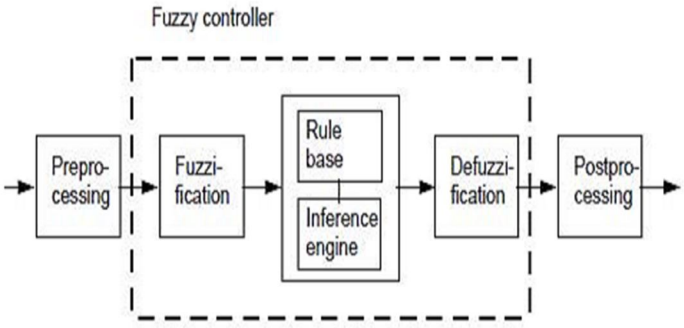


Fig.6. Fuzzy control block diagram.

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Volume 3 Issue X, October 2015
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Table IV
Control Rules for the Fuzzy Logic Controller

$\Delta Cie \backslash \Delta e$	LN	MN	SN	ZE	SP	MP	LP
LN	LP	LP	LP	MP	MP	SP	ZE
MN	LP	MP	MP	MP	SP	ZE	SN
SN	LP	MP	SP	SP	SE	SN	MN
ZE	MP	MP	SP	ZE	SN	MN	MN
SP	MP	SP	ZE	SN	SN	MN	LN
MP	SP	ZE	SN	MN	MN	MN	LN
LP	ZE	SN	MN	MN	LN	LN	LN

The membership functions for the inputs (e and cie) are shown in Fig.4 and Fig.5. The number of fuzzy levels is not fixed and it depends on the input resolution needed in an application. The larger the number of fuzzy levels, the higher is the input resolution. The fuzzy control implemented here uses sinusoidal fuzzy-set values.

Decision making: The control rules that associate the fuzzy output to the fuzzy inputs are derived from general knowledge of the system behaviour. However, some of the control actions in the rule table are also developed using “trial and error” and from an “intuitive” feel of the process to be controlled. In this effort, the control rules for the inverter Switching pulses in Table 1 resulted from the understanding of NPP’s behaviour and experimental tests of its VSI’s performance.

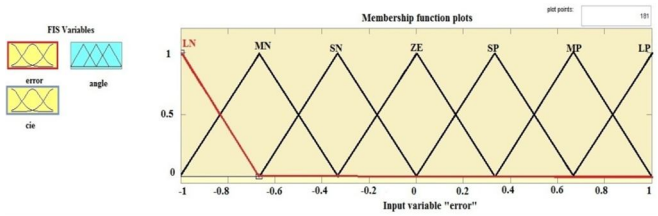


Fig.7. Membership function for error

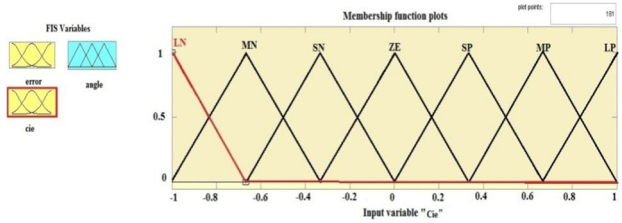


Fig.8. Membership functions for change in error.

Defuzzification: It is the Process of converting fuzzy flied output into a crisp value. In the defuzzification operation a logical sum of the results from each of the rules performed. This logical sum is the fuzzy representation of the change in firing angle (output). A crisp value for the change in firing angle is calculated.

TABLE V
SIMULATION PARAMETERS

DC Link Parameters	
DC Link Voltage	10.16KV
DC Link Capacitor	2200μF
Machine Parameters	
Type of Machine	Squirrel Cage Induction Machine
Rated Line-Line Voltage	6.6KV
Frequency	50Hz
Rated Power	2.45MW
Power Factor	0.84
Switching Frequency	2 KHz

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Volume 3 Issue X, October 2015
ISSN: 2321-9653
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V. SIMULATION RESULTS

A MATLAB/Simulink model of three-phase five-level DCMLI with the carrier-based NPP regulator is developed. The simulation parameters are shown in TableV. In the case of an inverter-fed induction motor drive system, the filter is not required, or a very small size filter will be sufficient to suppress the higher order frequency harmonics.

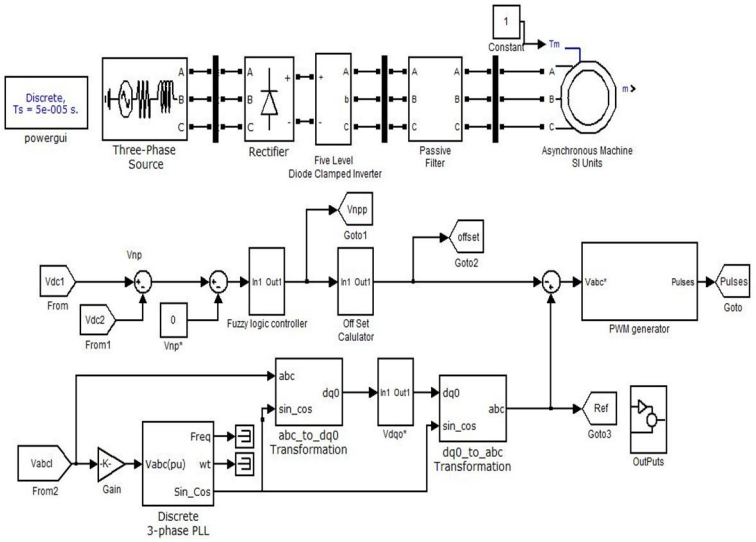
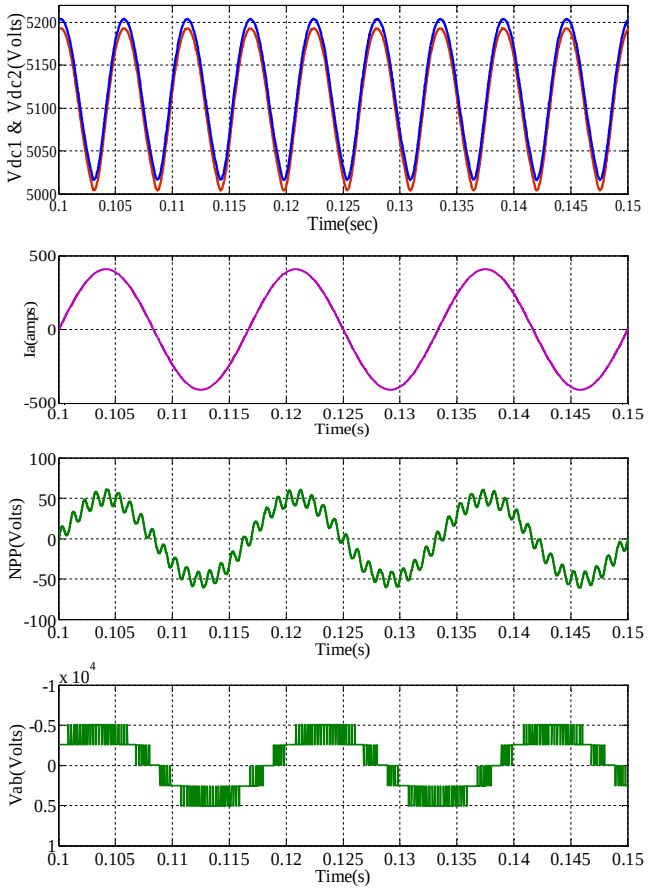


Fig.9.Simulink model of three-phase five-level DCMLI with carrier based NPP Regulator



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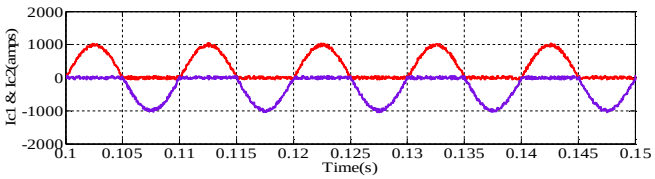


Fig.10.DC-link voltages (Vdc1 & Vdc2), NPP, invereter voltage, load current and capacitors currents PI with NPP regulator

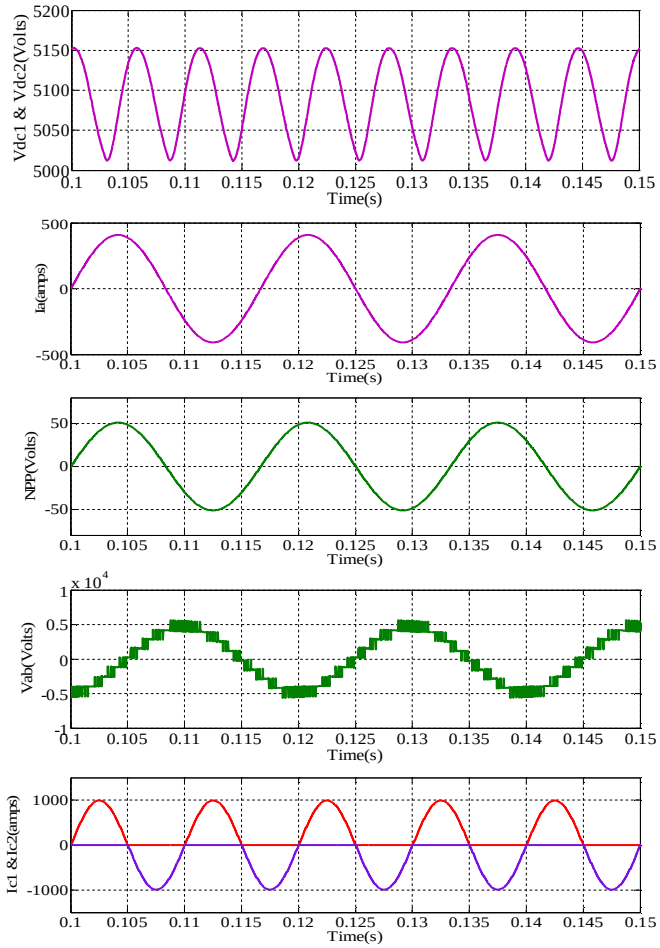


Fig.11. DC-link voltages (Vdc1 & Vdc2), NPP, invereter voltage, load current and capacitors currents Fuzzy with NPP regulator.

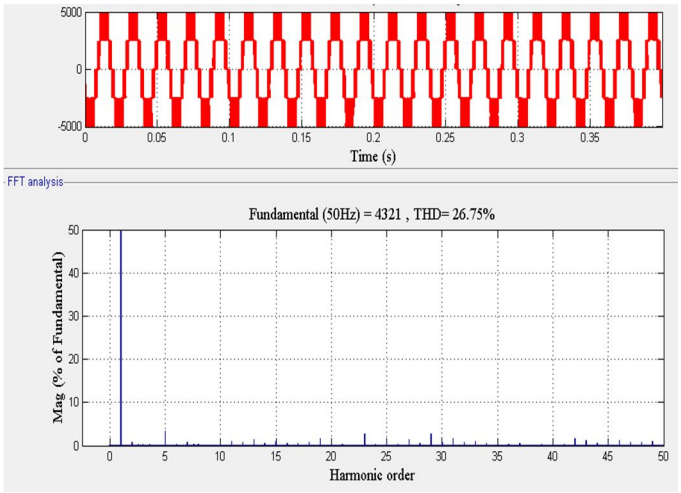


Fig.12.Simulated line voltage and its frequency spectrum of three level DCMLI with PI controlled NPP regulator

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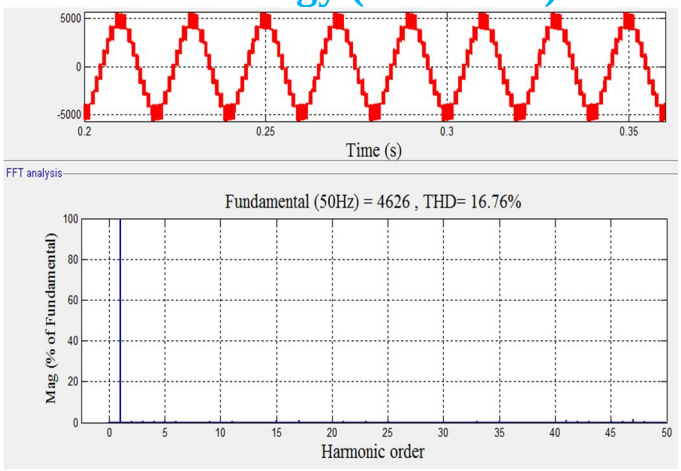


Fig.13.Simulated line voltage and its frequency spectrum of five levels DCMLI with fuzzy controlled NPP regulator.

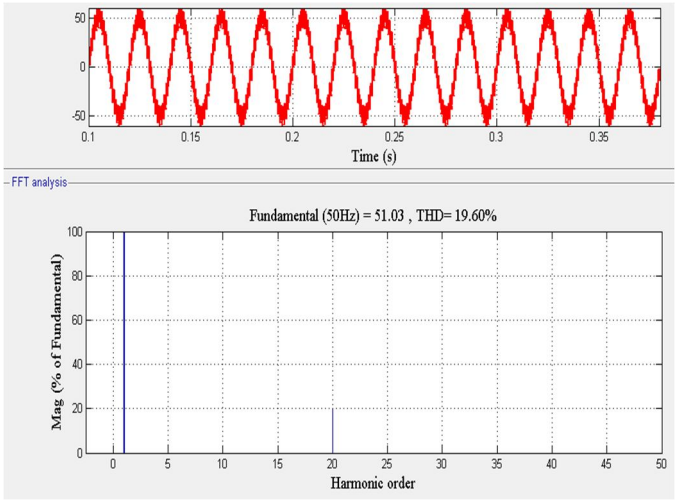


Fig.14.Simulated NPP and its frequency spectrum with PI Controlled NPP regulator.

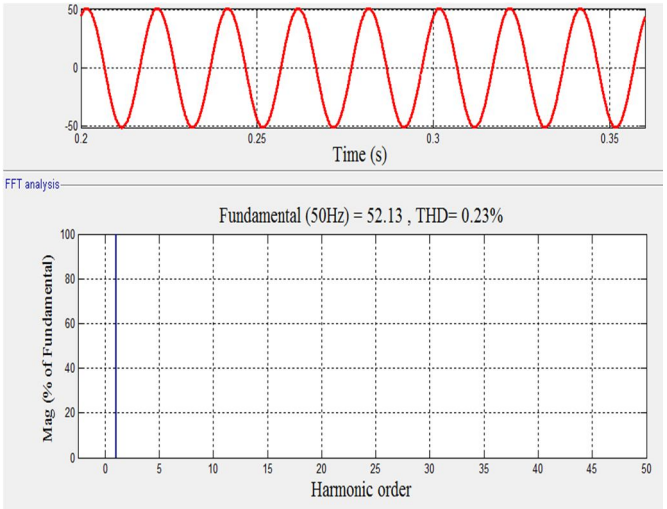


Fig.15.Simulated NPP and its frequency spectrum with fuzzy Controlled NPP regulator

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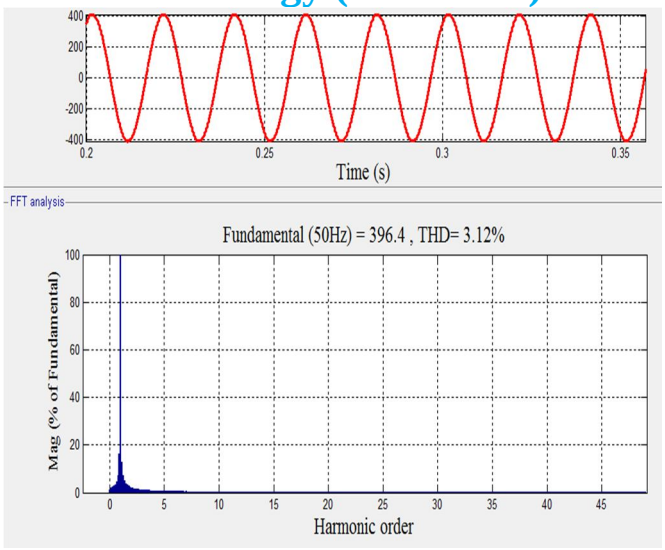


Fig.16.load current (ia) with PI controlled NPP regulator

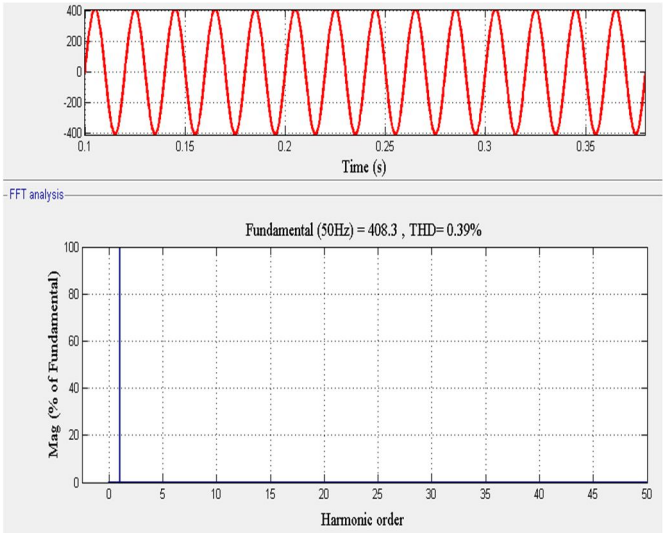


Fig.17.load current (ia) with fuzzy controlled NPP regulator

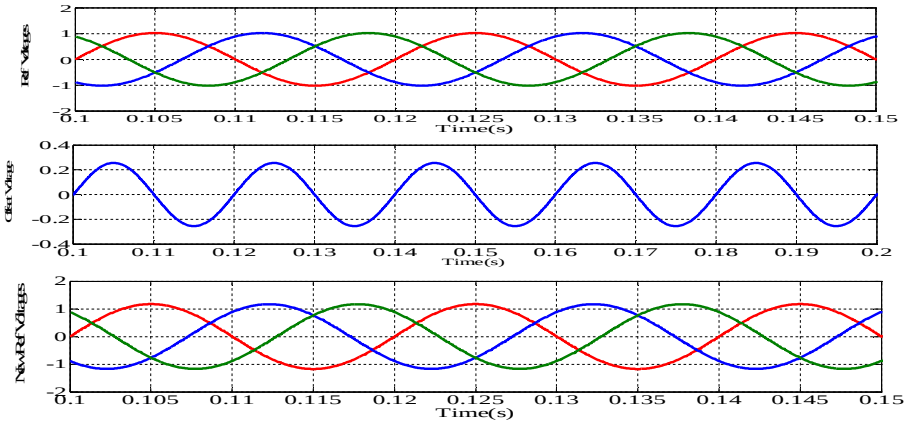


Fig.18. Actual modulating signal, offset voltage signal, and modulating signal with reduced-switching frequency NPP regulator

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Volume 3 Issue X, October 2015
ISSN: 2321-9653
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DC-link voltages (*V*dc1 and *V*dc2), NPP, load voltage, load current, and capacitor currents with pi and with the proposed NPP regulator are shown in Figs.10 and 11. It clearly indicates that ripple content in the NPP during balancing with high switching density in the capacitor current profile with PI controller for NPP regulator and an almost zero ripple content in NPP with reduced switching density in the capacitor current profile with Fuzzy controler.The imbalance presented in dc link with the proposed NPP regulator is symmetrical and having no offset. The actual reference signal, variable offset voltage signal, and new modulating signal are shown in Fig. 18 with the proposed NPP regulator. The objective of the present work is to control %THD. NPP with PI the regulator has a ripple and contains THD. The distortions present in NPP also affect the inverter performance. The waveform and harmonic spectrum of NPP with the regulator is shown in Fig. 14 which contains THD of 19.60%.

Inverter output voltage and load current get influenced during the balancing process. Fig.12 clearly indicates that, due to unbalanced dc-link capacitor voltages. Line voltage THD is 26.75%. Fig.13 shows the inverter line voltage with the proposed NPP regulator.

The load current THD is observed to be 3.12% PI with NPP regulator, as shown in Fig. 16, and 0.39% Fuzzy with NPP regulator change in fundamental value output indicates the reduction in power drawn from the source with the proposed regulator it is the indicative measure of switching loss reduction.

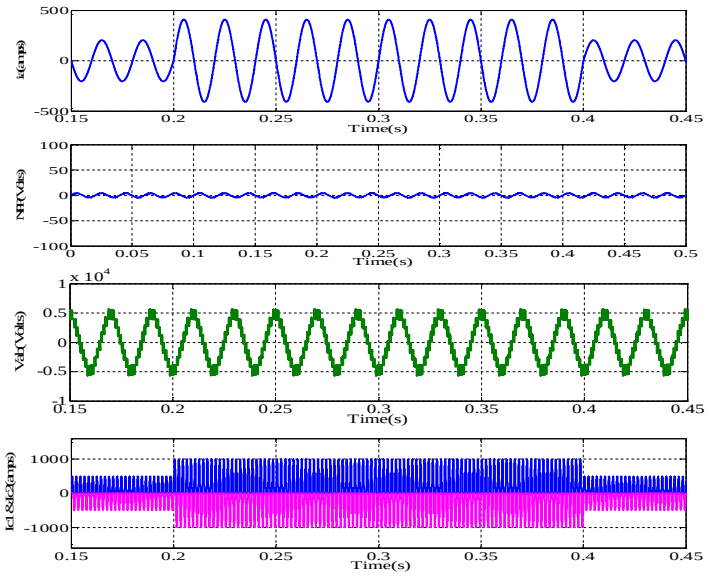
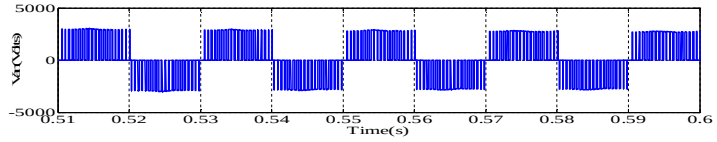
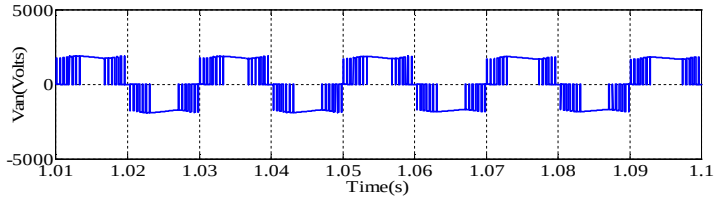


Fig.19.ia, NPP, Vab, Capacitor currents with regulator when load is doubled at 0.2s and restored at 0.4s.

The dynamic performance of the proposed regulator is studied by changing the load. Transient response of the controller is given in Fig. 13. By the increase/decrease in load at 0.2 and 0.4 s, respectively, NPP is seen to be unaltered during load changes. Switching loss reduction is achieved by inserting the “no switching” zone in each half cycle of the fundamental voltage wave.



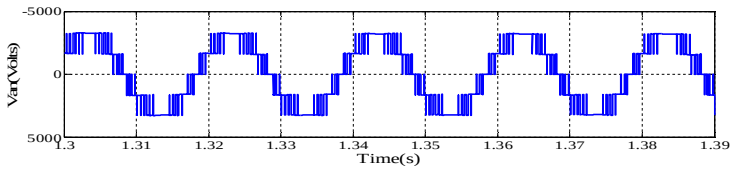
(a)



(b)

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(c)

Fig.20.Phase voltage (Van), (a) without regulator (b) PI with NPP regulator, (c) Fuzzy with NPP regulator.

This zone is created due to transition of inverter operation from the linear region to the slightly nonlinear modulation region, as shown in Fig.18. The magnitude and location of nonlinear modulation are controllable from controller parameters in PI controller and is eliminated with proposed regulator. Fig.20 shows phase voltage (Van) without, with PI and Fuzzy NPP regulator. It clearly indicates the reduced number of switching's per half cycle of phase voltage. The performance of the proposed regulator is summarized in Table VI.

Table VI
SIMULATION PERFORMANCE OF NPP REGULATOR

parameter	PI With Three level NPP Regulator	Fuzzy With Five level NPP Regulator
THD in Vab_inverter	26.75%	16.76%
THD in ia	3.12%	0.39%
THD in NPP	19.60%	0.23%

VI. CONCLUSION

A Complete simulation of simple carrier based neutral point voltage balancing regulator for a three phase five level diode clamped multi level inverter with fuzzy controlled closed loop controller has been carried out in this paper. The proposed regulator improves the inverter performance by balancing dc bus capacitance, NPP harmonic profile which doesn't require additional dc bus capacitance to balance the voltage. This paper has presented the absolute analysis for the total harmonic distortion for three phase PWM inverters with reduced value using FLCs.

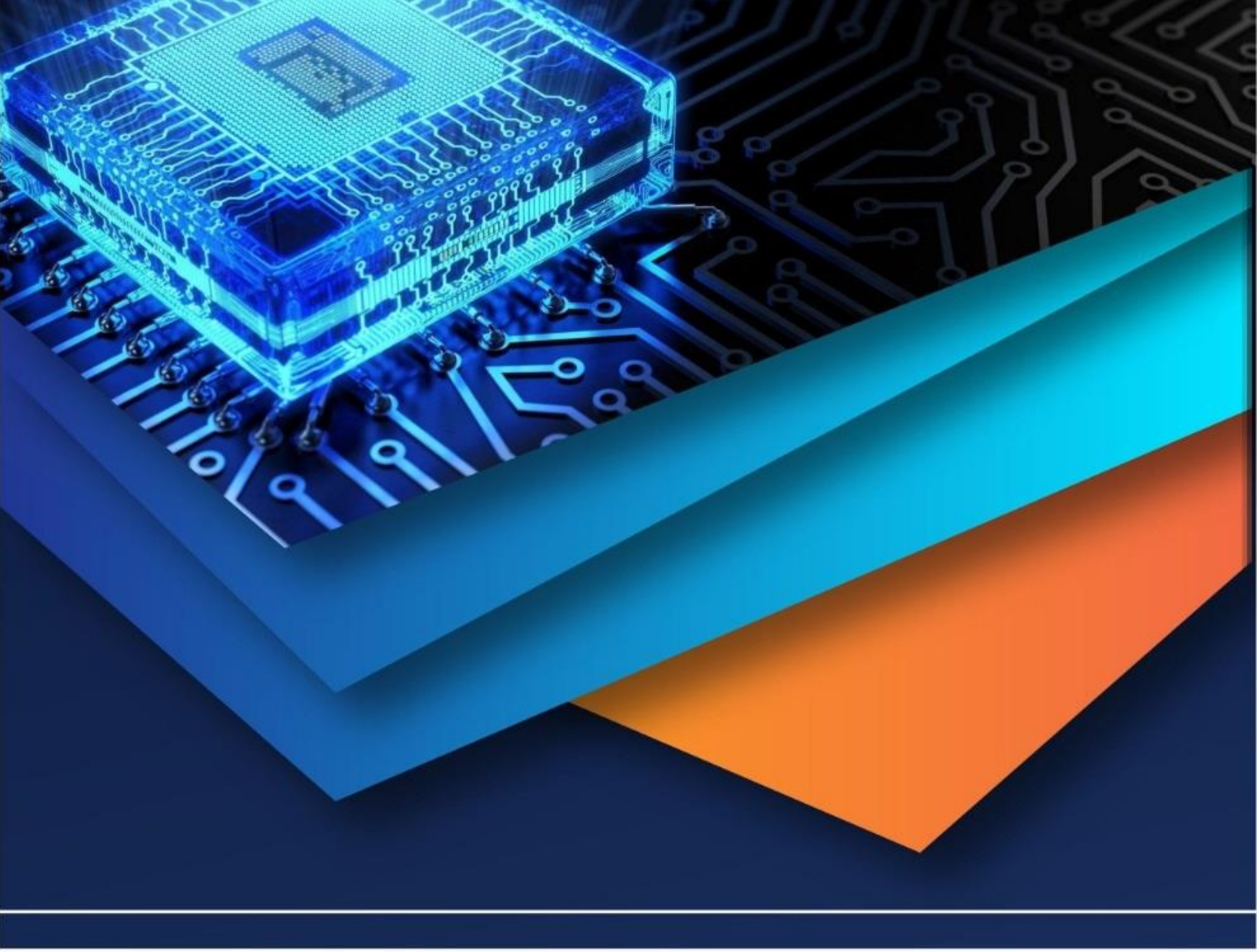
REFERENCES

[1] J. R. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S.Kouro," Multilevel voltage source converter topologies for industrial medium voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2830–2945, Dec. 2007..
[2] Peter, K., Lenke, R.U., Schroder, S., Doncker, R.W.D. "Design of a flexible control platform for soft-switching multilevel inverters", IEEE Trans. Power Electron,vol. 2, no.5, pp. 1778– 178, 2007.
[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral- point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA- 17, pp. 518–523, Sept./Oct. 1981.
[4] J. R. Rodriguez, J.-S.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.
[5] E. Sakasegawa and K. Shinohara, "Compensation for neutral point potential in three-level inverter by using motor currents," Trans. Inst. Elect. Eng. Jpn. vol. 121-D, no. 8, pp. 855–861, 2001.
[6] Q. Song, W. Liu, Q. Yu, X. Xie, and Z. Wang, "A neutral point potential balancing algorithm for three-level NPC inverters using analytically injected zero sequence voltage," in Proc. IEEE APEC, Feb. 2003, vol. 1, pp. 228–233
[7] A.Bendre, G. Venkataramanan, V. Srinivasan, and D.Rosene, "Modeling and design of a neutral point voltage regulator for a three level diode clamped inverter using multiple carrier modulation," IEEE Trans.Ind. Electron. vol. 53, no. 3, pp. 718-726, Jun. 2006.
[8] A. A.M. Bento, K. V. D. de Almeida, A. R. M. Oliveira, E. R. C. da Silva, and C. B. Jacobina, "A high power factor three-phase three-level rectifier," in Proc. IEEE PESC, Jun. 17–21, 2007, pp. 3040–3045.
[9] G. Bhuvaneswari and Nagaraju, "Multi-level inverter—A comparative study," IETE J. Res., vol. 51, no. 2, pp. 141–153, Mar./Apr. 2005.
[10] A. Yazdani and R. R. Iravani, "A generalized state space averaged model of the three-level NPC converter for systematic DC voltage balancer and current controller design," IEEE Trans. Power Del., vol. 20, no. 2, pp. 1105–1114, Apr. 2005.
[11] Mahesh A. Patel et al, "Use of PWM Techniques for Power Quality Improvement", IEEE press Series on power engineering, Wiley Interscience Publication,

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2003.
[12] D.G. Holmes and T.A. Lippo, “Pulse Width Modulation for Power Converters - Principles and Practice”, IEEE press Series on power engineering, Wiley Interscience Publication, 2003.
[13] C. Newton and M. Summer, “Neutral point control for multilevel inverters: Theory, design and operational limitations,” in Conf. Rec. IEEE IAS Annu. Meeting, New Orleans, LA, USA, Oct. 5–9, 1997, pp.1336–1343.
[14] Pradyumn Chaturvedi, Shailendra Jain, Pramod Agarwal “Carrier-Based Neutral Point Potential Regulator With Reduced Switching Losses for Three-Level Diode-Clamped Inverter”ieee transactions on industrial electronics, vol. 61, no. 2, february 2014.
[15] H. Akagi and T. Hatada, “Voltage balancing control for a three-level diode-clamped converter in a medium voltage transformer less hybrid active filter,” IEEE Trans. Power Electron., vol. 24, no. 3, pp. 571–579, Mar. 2009.
[16] S. Alepuz, J. Bordonau, and J. Peracaula, “Dynamic analysis of three-level voltage-source inverters applied to power regulation,” in Proc. 30th IEEE PESC, 1999, vol. 2, pp. 721–726.
[17] D. Boroyevich, J. Pou, and R. Pindado, “New feed-forward space vector PWM method to obtain balanced ac voltages in a three level neutral point clamped converter,” IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1026–1034, Oct. 2002.
[18] D. Boroyevich, J. Pou, and R. Pindado, “Effects of imbalanced and nonlinear loads on the voltage balance of a neutral point clamped inverter,” in Proc. IEEE PESC, 2003, pp. 53–58.
[19] A. M. Trzynadlowski, “Space vector PWM technique with minimum switching losses and a variable pulse rate,” in Proc. IEEE IECON, Nov. 1993, pp. 689–694.
[20] A. Yazdani and R. Iravani, “An accurate model for the DC side voltage control of the neutral point diode clamped converter,” IEEE Trans. Power Del., vol. 21, no. 1, pp. 185–193, Jan. 2006.
[21] S. Ogasawara and H. Akagi, “Analysis of variation of neutral point potential in neutral point clamped voltage source PWM inverters,” in Conf. Rec. IEEE IAS Annu. Meeting, 1993, pp. 965–970.
[22] Wing-Chi So, Chi K. Tse, and Yim-Shu Lee, “Development of a Fuzzy Logic Controller for DC/DC Converters: Design, Computer Simulation, and Experimental Evaluation,” IEEE Trans. Power. Electron., vol. 11, NO. 1, pp. 24-32, 1996.
[23] P. K. Chaturvedi, S. Jain, and P. Agarwal, “Reduced switching loss pulse width modulation technique for three-level diode clamped inverter,” IET Power Electron., vol. 4, no. 4, pp. 393–399, Apr. 2011.
[24] R. Maheshwari, S. Munk-Nielsen, and S.Busquets-Monge, “Design of neutral point voltage controller of a three-level NPC inverter with small DC link capacitor,” IEEE Trans. Ind. Electron., vol. 60, no. 5,pp. 1861–1871, May 2013.
[25] Y.-H. Lee, R.-Y. Kim, and D.-S. Hyun, “A novel SVPWM strategy considering DC-link balancing for a multi-level voltage source inverter,” in Proc. I EEE APEC, 1999, vol. 1, pp. 509–514.
[26] P. Palanivel and S. S. Dash, “Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques,” IET Power Electron., vol. 4, no. 8, pp. 951–958, Sep. 2011.
[27] A. L. Batschauer, S. A. Mussa, and M. L. Heldwein, “Three-phase hybrid multilevel inverter based on half-bridge modules,” IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 668–678, Feb. 2012.

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