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Design of ADC in Time Constraint Based on Adders

T.Vanitha[1], S.Baskar[2]
[1] PG Scholar, VLSI Design, Dept. Of ECE ,Angel College of Engineering & Technology,Tirupur,Tamilnadu. India .[2] Assistant professor, Dept. Of ECE,Angel College of Engineering &Technology,Tirupur,Tamilnadu, India.

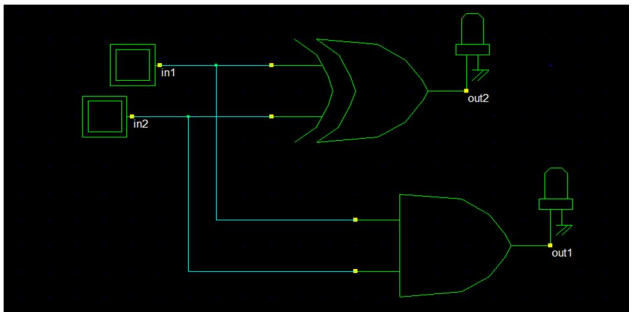
Abstract- In This paper the design of ADC based on adder's circuit is proposed. The adder circuit is a very important component in the design of digital circuits. The main motive of this paper is to determine the comparative study of time, surface area. The time delay is also important parameter to determine the performance of the design. In this paper, interesting full adder and half adder circuits are reviewed and compared concerning time consumption, and area. It is based on majority-NAND gates, multiplexer which are designed with new methods in each cell. Thus NAND gate and MUX has become a very popular and useful method to implement any circuits which help to less time, surface area.
Keywords: ADC, MUX, NAND, adders

I. INTRODUCTION

There are two basic type of converters, digital-to-analog (DACs or D/As) and analog-to digital (ADCs or A/Ds). Their purpose is fairly straightforward. In the case of DACs, they output an analog voltage that is a proportion of a reference voltage, the proportion based on the digital word applied . In the case of the ADC, a digital representation of the analog voltage that is applied to the ADCs input is proportional to a reference voltage. Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Applications such as wireless communications and digital audio and video have created need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors continually challenge analog designers to improve and develop new ADC and DAC architectures. There are many different types of architectures, each with unique characteristics and different limitations .One of the architecture which is used for converting continuous time varying signal to digital signal is Flash ADC .
In built of ADC which consists of adders, multipliers, amplifiers,rectifiers. We are implementing new adders that adders are constructing with MUX and NAND gates. In most of these systems, the adder is part of the critical path that determines the overall performance of the system and the full adder is the core element of complex arithmetic circuits. That is why enhancing the performance of the 1-bit full-adder and half adder cell (the building block of the binary adder) is considered a significant goal. The Full Adder and half adder is proven to use MUX construction have the minimum area and less delay product by simulation using Xilinx ISE 13.2i and schematic is proven by micro wind DSCH tool. A multiplexer is a combination of logic gates resulting into circuits with two or more inputs (data inputs) and one output. When compared to NAND gates MUX is faster and less time consuming.

II. HALF ADDER DESIGN

Half adder circuit needs two binary inputs and two binary outputs. The input variables designated the augends and added bits; the output variables produce the sum and carry



Volume 3 Issue X, October 2015
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Fig.1 half adder design

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table-1 Truth table of half adder

The simplified Boolean function according to the truth table is given as

S=A'B+AB'

C=AB

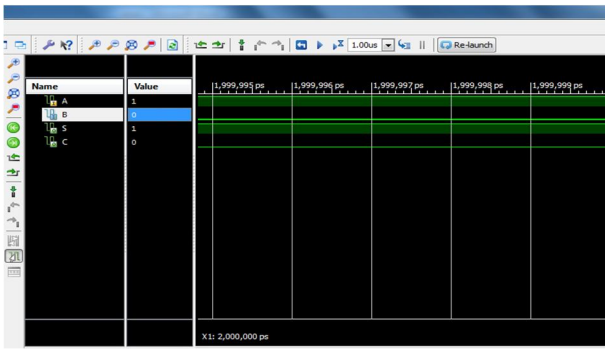

Fig.2 simulation result of half adder on ISE Design Suite

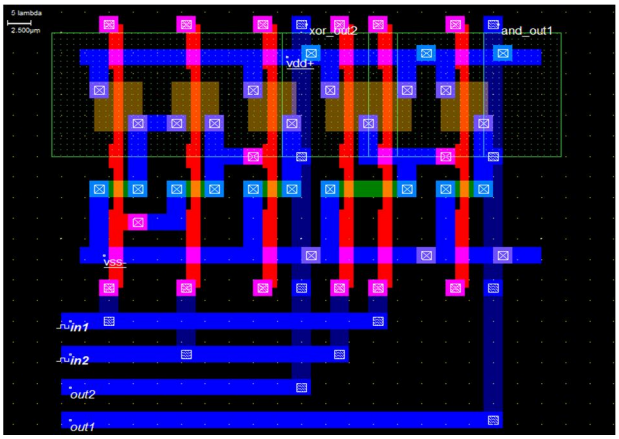

Fig-3: Full automatic layout design of half adder

III. HALF ADDER USING MUX DESIGN

Volume 3 Issue X, October 2015
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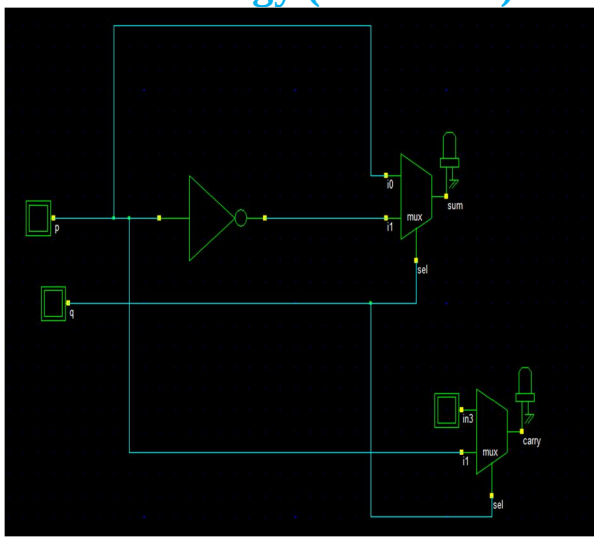

Fig-4: half adder using MUX design

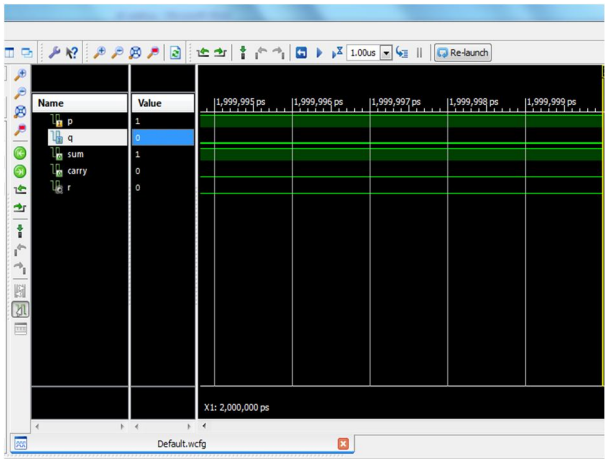

Fig.5 simulation result of half adder using MUX on ISE Design Suite

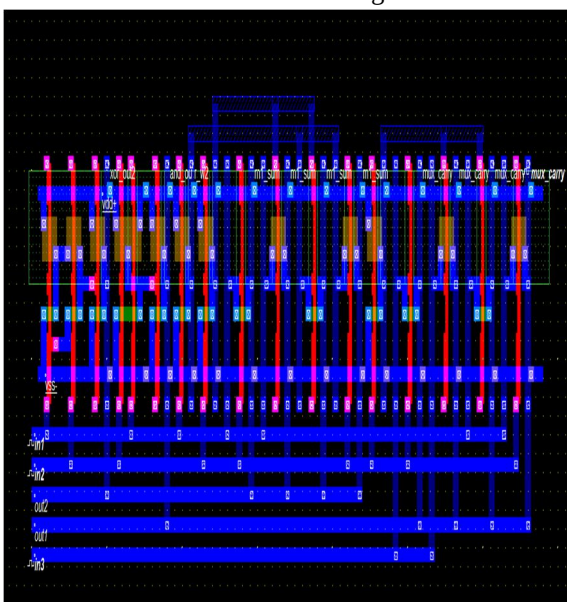

Fig.6 Full automatic layout design of half adder using MUX

Volume 3 Issue X, October 2015
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IV. HALF ADDER USING NAND GATES

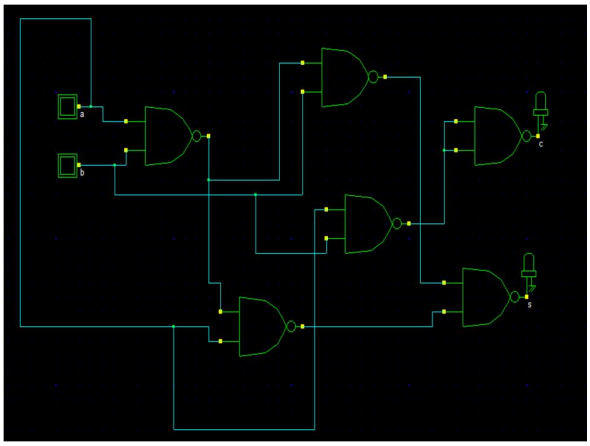

Fig-7 half adder using NAND design

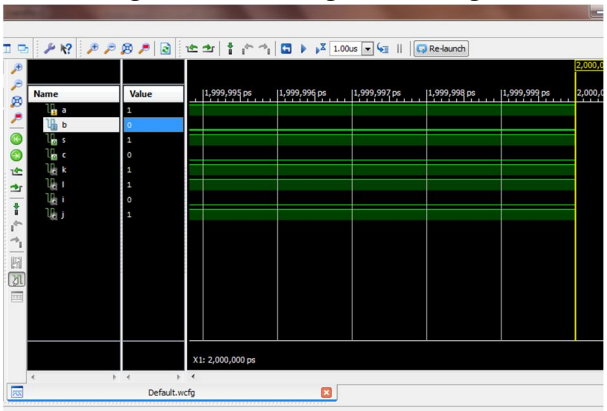

Fig.8 simulation result of half adder using NAND on ISE Design Suite

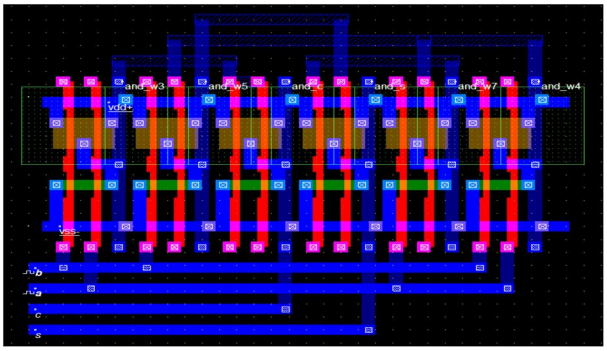

Fig.9 Full automatic layout design of half adder using NAND gate

V. FULLADDER DESIGN

A full adder can add a bit carried from another addition as well as the two inputs, whereas a half adder can only add the inputs together.

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$$Sum = A \oplus B \oplus C$$

$$Carry = AB + BC + CA$$

A	B	Carry-In	Sum	Carry-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table-2 Truth table of full adder

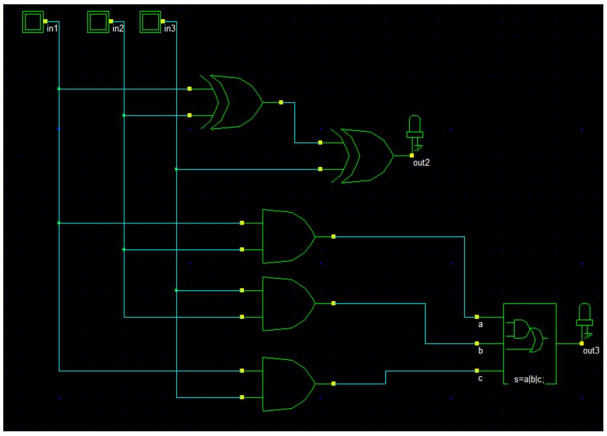

Fig-10: fulladder design

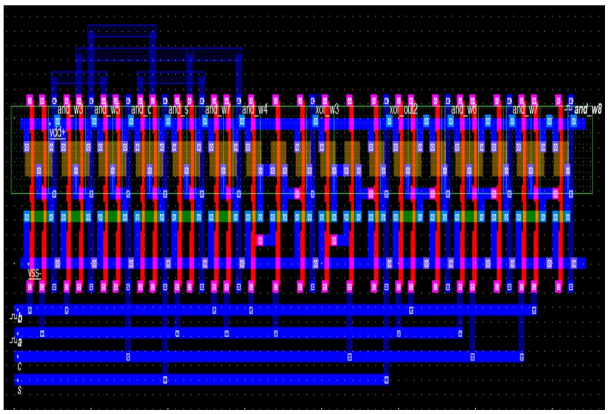

Fig11 Full automatic layout design of full adder

Volume 3 Issue X, October 2015
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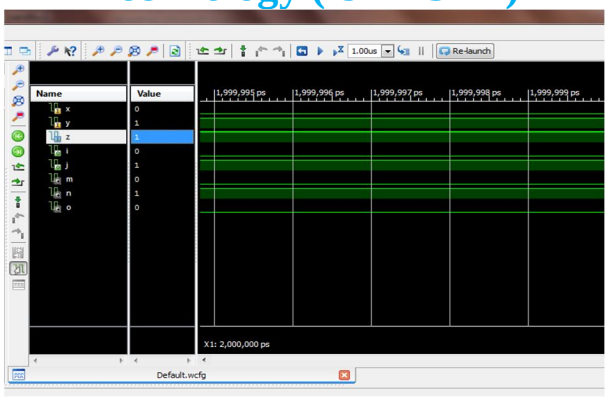

Fig.12 simulation result of full adder

VI. FULLADDER DESIGN USING MUX

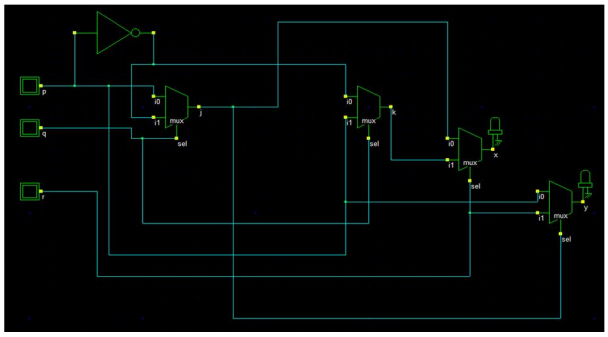

Fig13 full adder using MUX design

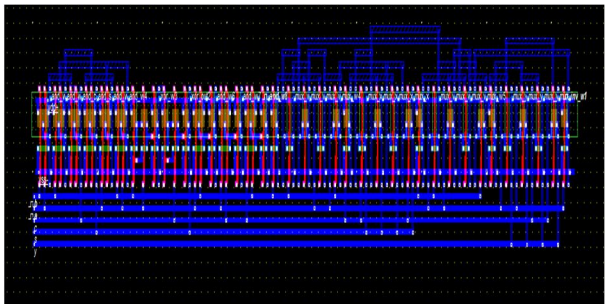

Fig.14Full automatic layout design of full adder using MUX

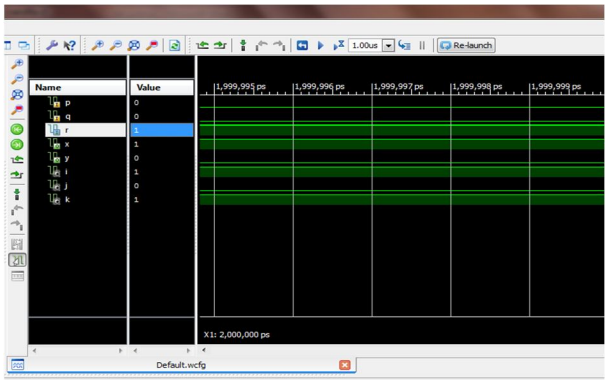

Fig.15 simulation result of full adder using MUX on ISE Design Suite

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VII. FULLADDER DESIGN USING NAND GATE

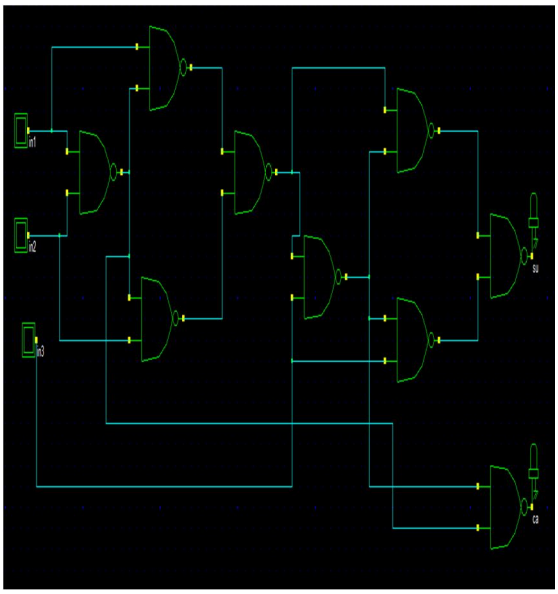


Fig.16 full adder using NAND design

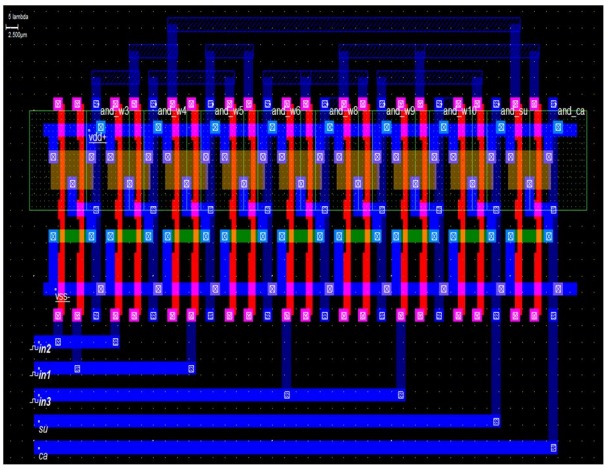
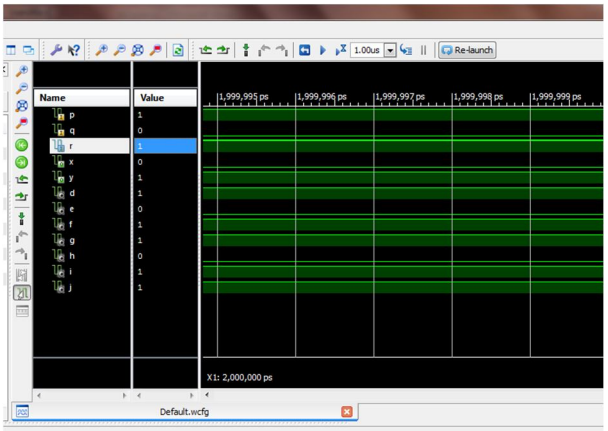


Fig.17 Full automatic layout design of full adder using NAND gate



Volume 3 Issue X, October 2015
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Fig.18 simulation result of full adder using NAND on ISE Design Suite

VIII. RESULT ANALYSIS

Comparative analysis is based on two types of design method Half adder and full adder using NAND gate and MUX is shown in table-2. Comparison aspects are based on CPU time, surface area used. Comparison shows that MUX based half adder and full adder is better than using gate.

Table-2 Comparative Analysis

	Ordinary HA		Using NAND		Using MUX	
Para-meters	LUT'S	CPU time (s)	LUT'S	CPU time (s)	LUT'S	CPU time (s)
HA	2	4.07	2	2.82	1	2.48
FA	3	4.40	3	2.58	2	2.43

Thus chart-1, chart-2 and show the comparison graph for CPU time consumption of half adder and full adder using NAND,MUX

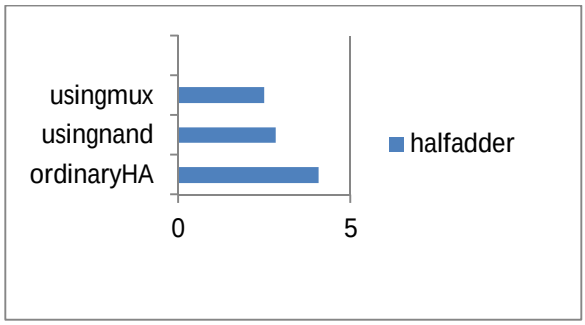


Chart-1: CPU time of half adder comparison between design-1, design-2 and design

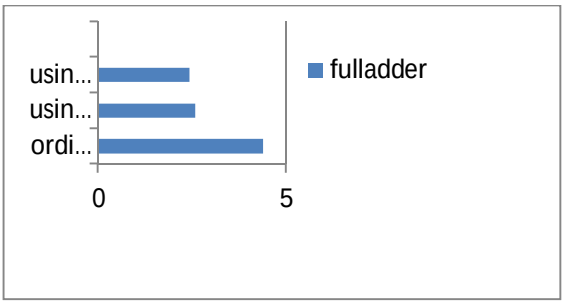


Chart-2: CPU time of full adder comparison between design-1 design-2 and design-3

IX. CONCLUSION

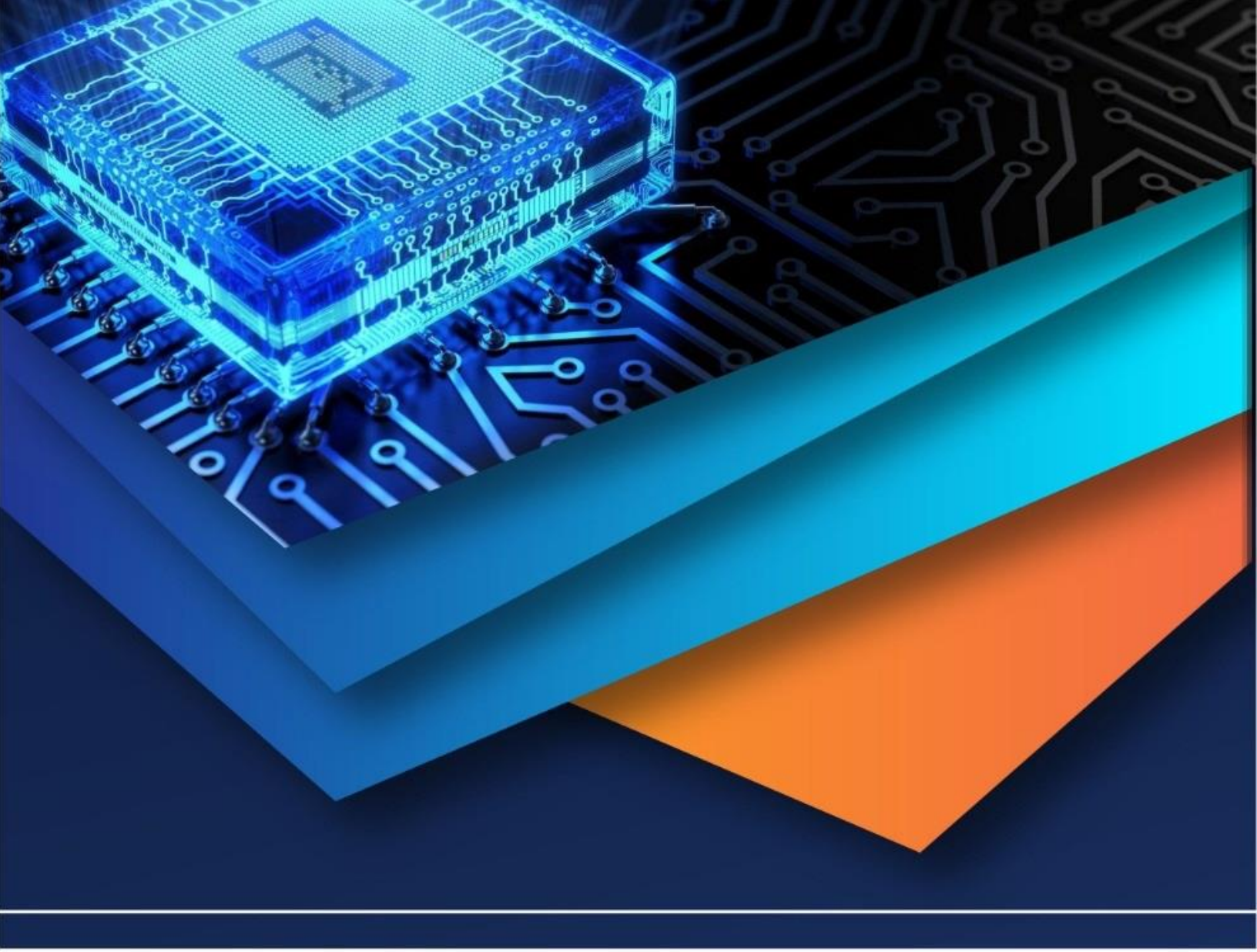
From the above discussion we can conclude that adders using MUX is very useful technique to reduce the surface area on a chip and time consumption. So i focus here for MUX design analysis and find better result for all parameters point of view. Numerically CPU time consumption and area is reduced by twice the amount.

REFERENCES

[1] Ravi Kumar Anand, Kartar Singh, Pankaj Verma, Ashish Thakur "Design of area and power efficient half adder using transmission gate" IJRET: International Journal of Research in Engineering and Technology eISSN: 2319-1163 | pISSN: 2321-7308.\
[2] Manju Devi,Arunkumar P Chavan,Dr. K N Muralidhara "A1.5v 3bit ,500m s/s low power cmos flash ADC" International Journal Of Engineering And Computer Science ISSN:2319-7242 Volume 3 Issue 3 March, 2014 Page No. 4044-4048.
[3] P. E. Allen and D. R. Holberg. "CMOS Analog Circuit Design" second edition oxford university press. ISBN 019 5116 445, 2002.
[4] Amol Inamdar, Anubhav Sahu, Jie Ren, Aniruddha Dayalu, and Deepnarayan Gupta, "Flash ADC Comparators and Techniques for their Evaluation", IEEE Transactions on Applied Superconductivity, Vol.23, no.3, ISSN No.1051-8223,pp. 1-8, Jan 2013.
[5] R. Jacob Baker "CMOS: Mixed Signal Circuit Design", Second Edition, Wiley-IEEE Press, ISBN 978 0470-29026-2, 2009.
[6] N. Weste and K. Eshraghian, Principles of CMOS VLSI Design, A System Perspective. Reading, MA: Addison-Wesley, 1988.
[7]P.Iyappan,P.Jamunaand,S.Vijayasamundiswary,"Design of Analog to Digital Converter Using CMOS Logic", IEEE International Conference on Advances in Recent Technologies in Communication and Computing, ISBN no. 978-0-7695-3845-7, pp. 74-76, 2009.
[8] Channakka Lakkannavar, Shrikanth K, Kalmeshwar.N, (2012)" Design implementation and analysis of Flash ADC architecture with differential amplifier as comparator using CD approach", International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, Vol-1 Iss-3.
[9] Nuzzo, P., et al.: 'A 10.6 mW/0.8 pJ power-scalable 1 GS/s 4b ADC in 0.18 mm CMOS with 5.8 Ghz ERBW'. Proc. 43rd Design Automation Conf. (DAC), San Francisco, CA, July 2006, pp. 873-878.
[10]. Saradindu Panda, A.banerjee, B.maji and Dr. A.K. Mukhopadhyay, "Power and delay comparison in between different types of full adder circuits", International Journalof advanced research in electrical, electronics and instrumentation engineering, volume 1, issue 3.pp.168-172, 2012.
[11]. S,Goel.M.A. Elgamel, M.A. Bayoumi, and Y.Hanarty. "Design methodologies for high performance noise-tolerant XOR-XNOR circuits," circuits and systems I:Regularpapers, IEEE Transactions on,vol.53,pp.817-878,2006.
[12]. Richa Singh and Rajesh Mehra , "Power efficient design of multiplexer using adiabatic logic", International Journal of advances in engineering and technology, pp 247-254,march 2013.
[13]. Neil H.E.Weste, David Harris and Ayan Banaerjee, "CMOS VLSI design". Pearson Education,Inc., pp. 11,Third Edition, 2005.
[14]. Nabihah Ahmad, Rezaul Hasan, IEEE "A New Design of XOR-XNOR gates for low power Electronic Devices", System and Applications(ICEDSA), pp.45-49, 2011.
[15]. I. Hassoune, D. Flandre, I. O'Connor and J.D.Legat:ULPFA: ANew Efficient Design of A Power Aware Full Adder", IEEE Transactions on Circuits and Systems I-5438,pp.2066-2074, 2008.
[16] A. Shams, T. Darwish, and M. Bayoumi, "Performance analysis oflow power 1-bit CMOS full adder cells," IEEE Trans. Very LargeScale Integr.(VLSI) Syst., vol. 10, no. 1, pp. 20-29, Feb. 2005.
[17] A. Shams and M. Bayoumi, "Performance evaluation of 1-bit CMOSadder cells," in Proc. IEEE Int. Symp. Circuit and Systems, Jul. 1999,pp. 27- 30.
[18] F. Frutaci, M. Lanuzza, P. Zicari S. Perri, P. Corsonello " LowPower Split Path Data Driven Dynamic Logic" published in Ie tCircuit Devices & Systems 20th April 2009.
[19] Abdoul M. Rjoub, Al-Mamoon Al-Othman "The influence of theNanometer Technology on performance of CPL Adders" Journal of computers, Vol. 5, NO. 3, March 2010.
[20]B. Ramkumar and Harish M Kittur "Low-Power and Area-Efficient Carry Select Adder" IEEE Trans. on very large scale integration systems 2012.

SPIN ABSTRACT

In this paper the design of ADC headquartered on adder's circuit is proposed. The adder circuit is an awfully principal factor in the design of application specified built-in circuits. The main purpose of this paper is to investigate the comparative be taught of time, surface discipline. .The time extend can be predominant parameter to assess the efficiency of the design. On this paper, intriguing full adder and 1/2 adder circuits are reviewed and in comparison regarding time consumption, and discipline. It is established on majority-NAND gates, multiplexer which might be designed with new ways in each cell..Therefore NAND gate and MUX has turn out to be an extraordinarily preferred and valuable technique to put into effect digital circuits which support to time, surface subject.



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