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Comparative Evaluation of Cascaded Half-Bridge Multilevel DC-Link Inverter and Conventional H Bridge Multilevel Inverter

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Abstract*—Multilevel inverters have been successfully adopted by industry for high power application because of their superior performance over two level inverter. But with increasing number of levels switching complexities and number of switches increase in conventional multilevel inverter (MLI). Multilevel dc-link inverter (MLDCLI) provides a solution to achieve same number of levels with reduced number of switches. This paper discusses the merits of MLDCLI over conventional MLI. A performance comparison of conventional cascaded H bridge MLI and cascaded half-bridge MLDCLI with square wave staircase switching and multicarrier sinusoidal pulse width modulation is presented using computer simulation.
Keywords*— Multilevel Inverter (MLI), multilevel dc-link inverter (MLDCLI), conventional cascaded H bridge MLI , cascaded half-bridge MLDCLI, THD, SPWM.

I. INTRODUCTION

Recently, the demand for high power application is increasing in industry. The demand easily reaches in megawatt range. Medium voltage (2.3kV to 6.6kV) high power (1 – 50MW) converters are currently in service in industry [1] [7]. For these high power applications semiconductors like IGBT, MOSFET etc. cannot be directly connected to high voltage supply, here multilevel inverters (MLI) have become an attractive solution for such applications [2]. Currently MLI have applications in HVDC transmission, steel rolling mills, railway traction, reactive compensators for power transmission and many more applications [1]. Multilevel inverters have a better performance than normal two level inverters in many aspects like lower harmonics, less bulky filters, lower stress across switch, lower EMI. Conventional MLI are better than two level but as the levels increase some complexities start creeping in conventional MLI like increase in number of switches, complexity in switching logic, capacitor voltage and balancing problems. The answer to these drawbacks of conventional MLI can be found in multilevel dc-link inverter (MLDCLI)[3]. The drastic reduction in number of switches and components with increase in number of voltage level (m) in MLDCLI as compared to conventional MLI. The switch count reduces to (m + 3) for MLDCLI from 2(m-1) for conventional MLI.

MLDCLI has similar topologies like conventional MLI but with reduced number of switches and component count. The different type of MLDCLI are diode clamped MLDCLI, flying capacitor MLDCLI, cascaded half-bridge MLDCLI. More emphasis on cascaded half-bridge MLDCLI is given in this paper as the number of extra components like dc splitting capacitors, diodes and flying capacitors are eliminated in cascaded half-bridge MLDCLI thus requiring least number of total components for same number of voltage levels.

In section II a brief description of cascaded half-bridge MLDCLI is given followed by simulation results and waveforms in section III , and conclusion in section IV.

II. CASCADED HALF-BRIDGE MULTILEVEL DC-LINK INVERTER

The cascaded half-bridge MLDCLI is made up of two units 1)the series cascaded half-bridge cells which produces a stepped dc voltage waveform on the dc bus and 2) the single phase full bridge inverter which inverts the dc to produce a stepped ac voltage at the output of inverter. A nine level cascaded half bridge MLDCLI is shown in Fig. 1. For the purpose of comparison a conventional nine level cascaded H bridge MLI is also shown in Fig. 2. The MLDCLI requires only (m+3) switches as compared to 2(m-1) for conventional MLI to achieve the same number of voltage levels. This is evident from Fig. 1 and Fig. 2 that nine level MLDCLI requires only twelve switches but conventional MLI requires sixteen switches. The component count comparison is shown in Table I. As the number of switches reduces the number of gate driver circuit also reduces. The switches Sa, Sb are complimentary in nature thus no extra logic is needed only delay is required between the switches to avoid shoot through of switches thus reducing the switching logic requirement even further. Fig. 3 gives the comparison in number of switches with increase in number of levels for

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conventional MLI and MLDCLI.

TABLE I
COMPONENT COUNT COMPARISON

	MLDCLI	Conventional MLI
No. of Switches	m + 3	2 (m – 1)
No. of Gate Driver circuit	m + 3	2 (m – 1)

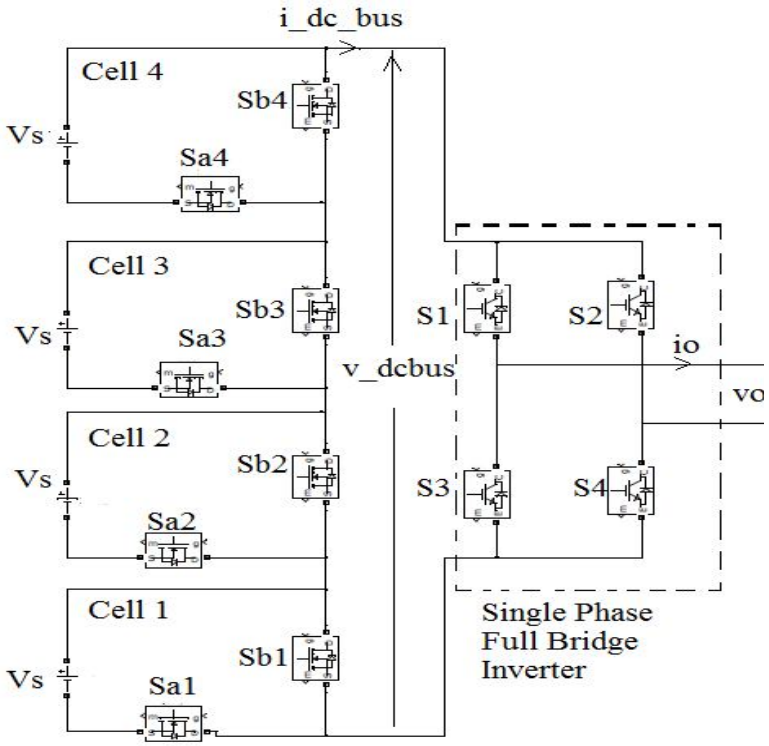


Fig. 1 Nine level cascaded half-bridge MLDCLI

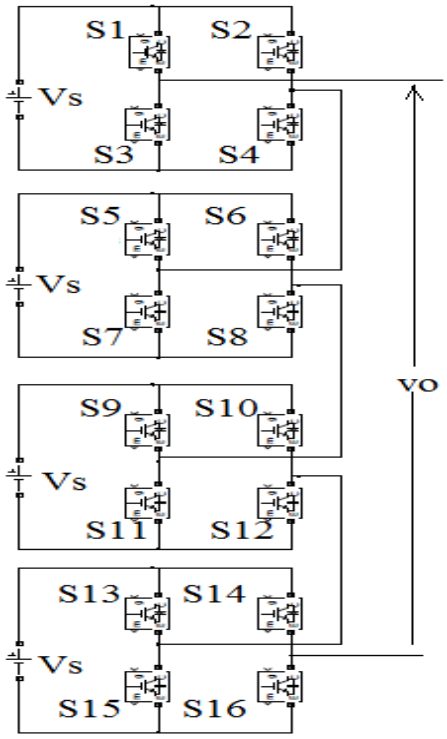


Fig. 2 Nine level conventional cascaded H bridge MLI

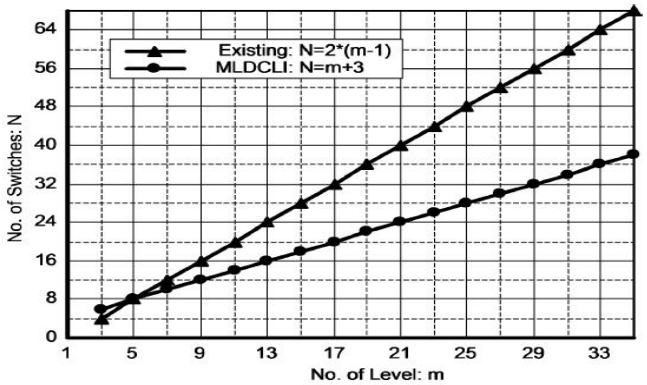


Fig. 3 Comparison of required number of switches required.

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III. SIMULATION WAVEFORMS AND RESULTS

For studying and comparison of performance of cascaded half-bridge MLDCLI and the conventional cascaded H bridge MLI, computer simulation for nine level cascaded half-bridge MLDCLI (Fig. 1) and nine level cascaded H bridge MLI (Fig. 2) is done. For simulation dc source Vs = 25V for each cell, maximum output voltage level =100V and resistive load of 20 ohm is used. Two types of switching schemes can be used for driving the MLI i.e. A) square wave staircase switching scheme and B) sinusoidal pulse width modulation scheme.

A. Square Wave Staircase Switching Scheme

In square wave switching scheme square wave of different duty cycle is used for producing a stepped voltage at the output of inverter. Fig. 4 shows square wave switching scheme for conventional nine level cascaded H bridge inverter. Fig. 5 shows the square wave switching scheme for nine level cascaded half-bridge MLDCLI. It can be observed from Fig. 4 and Fig. 5 that conventional MLI requires eight independent switching signals but MLDCLI requires only four independent switching signals. The output voltage and current waveforms for conventional nine level cascaded H bridge MLI is shown in Fig. 6.

The cascaded-half bridge MLDCLI first produces a stepped voltage waveform on the dc bus (see Fig. 7) which is then inverted to produce an ac output (see Fig. 8). It can be seen that the waveform produced is similar but it has been done with reduced number of switches in MLDCLI.

B. Multicarrier Sinusoidal PWM (SPWM) Switching Scheme

In multicarrier SPWM level shifted triangular carriers are compared with single sinusoidal waveform to produce switching pulses for the switches [4]. Here eight triangular carriers of frequency of 1MHz and sine wave of 50Hz is compared with modulation index of 0.8 is used for conventional MLI (Fig. 9) and four triangular carriers of frequency of 1MHz and rectified sine wave of frequency 100Hz with modulation index of 0.8 is used for MLDCLI (Fig. 10). Fig. 11 shows the output voltage and current for nine level conventional cascaded H bridge MLI with SPWM switching while DC bus voltage and current for nine level cascaded half-bridge MLDCLI with SPWM switching is shown in Fig. 12. The DC bus voltage is inverted to produce an ac at the output as shown in Fig. 13.

C. Comparison Of Results

A comparison of the nine level cascaded half-bridge MLDCLI with conventional cascaded H bridge MLI with different switching styles is presented in Table II And Table III. It can be seen in Table II and Table III that the values for THD, output voltage in both columns are approximately same. The MLDCLI can achieve the same number of voltage levels with reduced number of switches and lower switching complexities with a slight increase in switch rating can be observed.

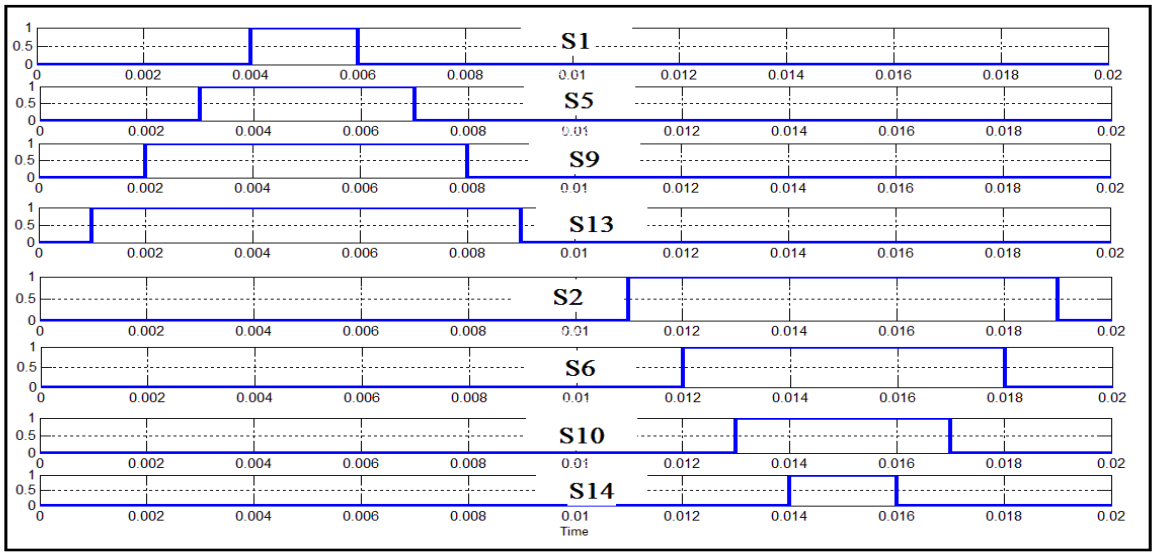


Fig. 4 Square wave switching signals for conventional nine level cascaded H bridge MLI.

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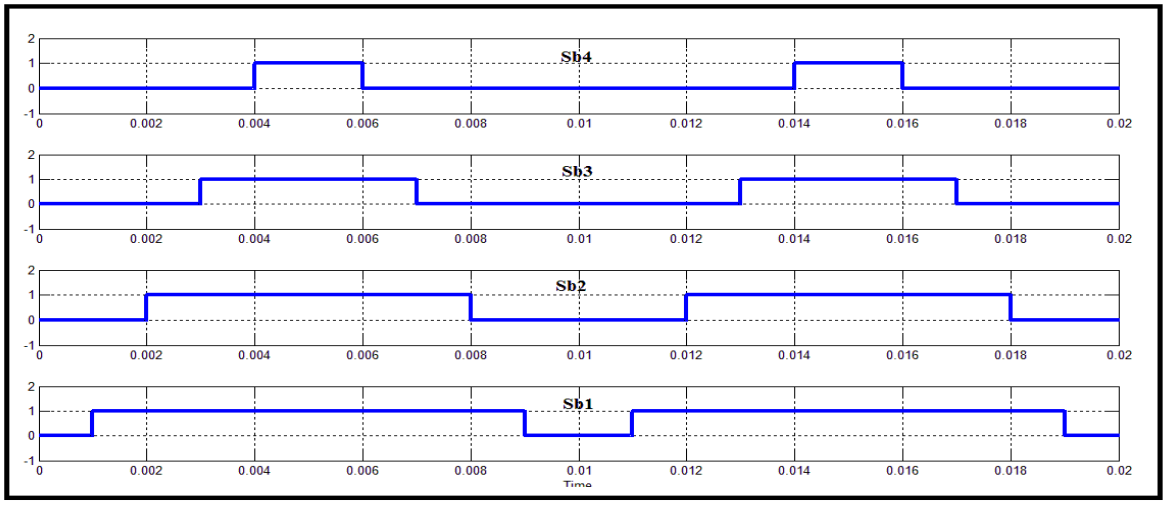


Fig. 5 Square wave switching signals for nine level cascaded half-bridge MLDCLI.

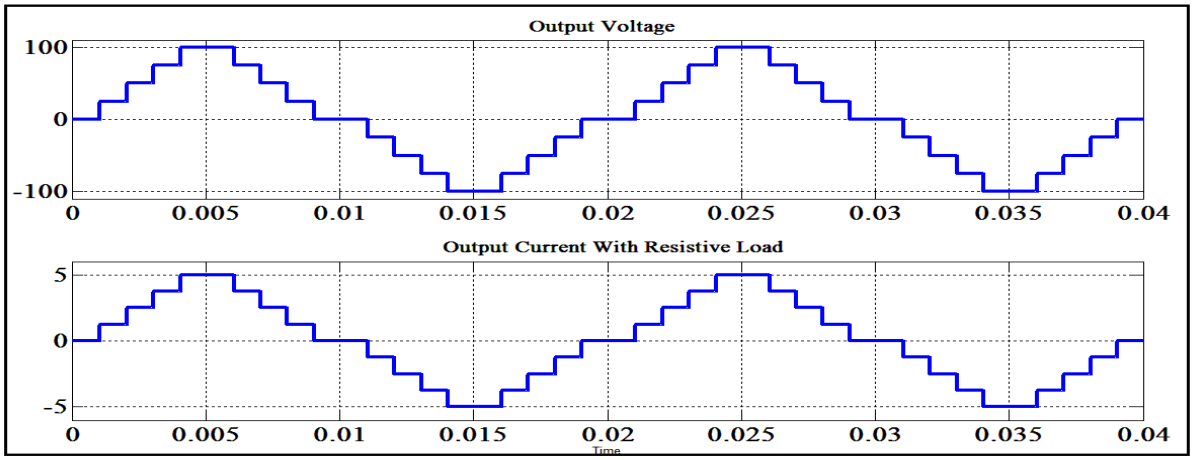


Fig. 6 Output voltage and current waveforms for nine level conventional cascaded H bridge MLI with square wave switching.

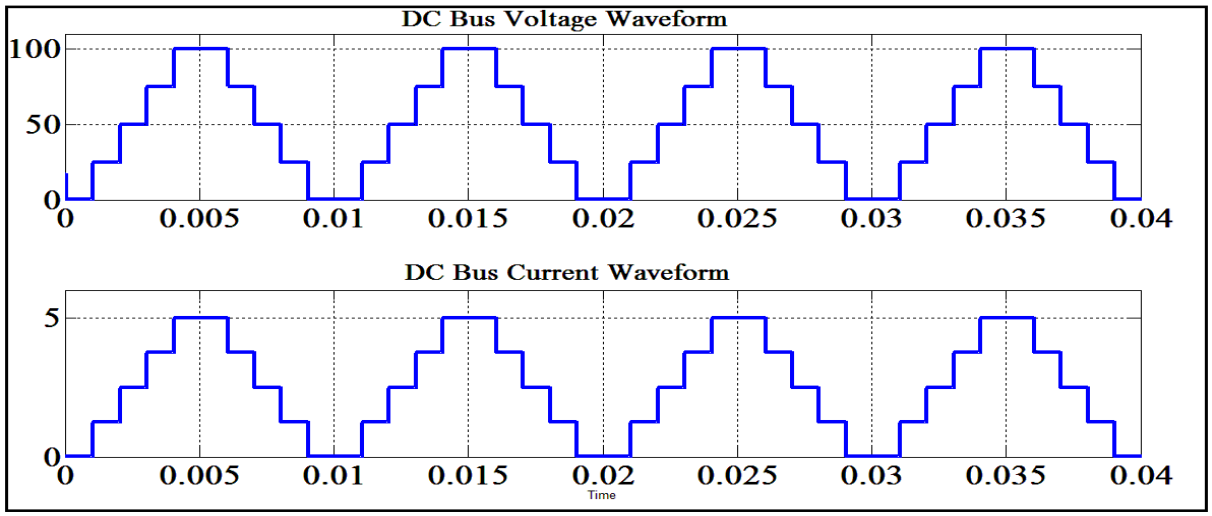


Fig. 7 DC bus voltage and current waveforms for cascaded half-bridge MLDCLI with square wave switching.

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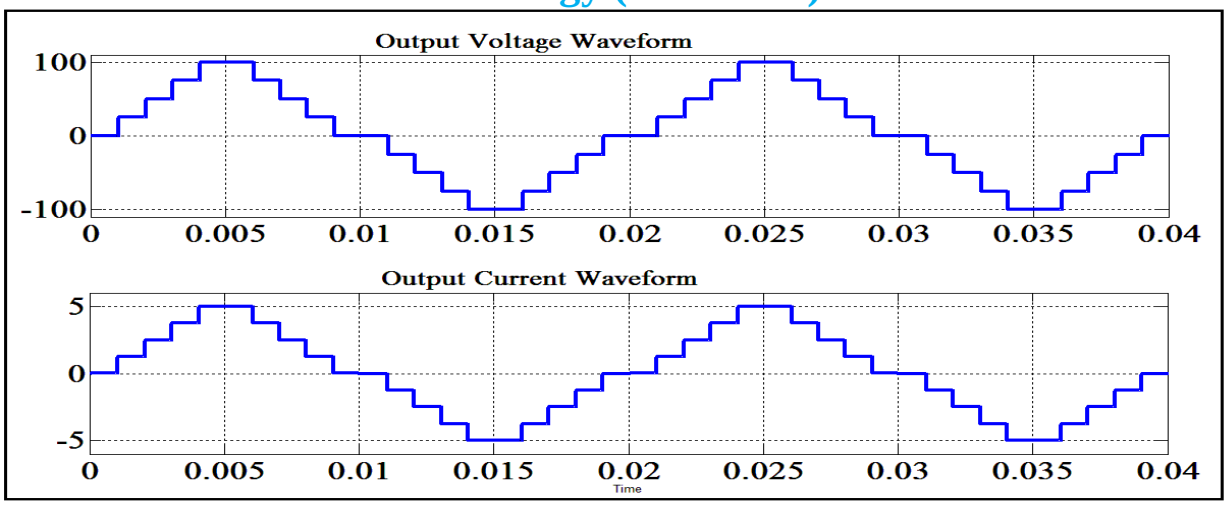


Fig. 8 Output voltage and current waveforms for nine level cascaded half-bridge MLDCLI with square wave switching.

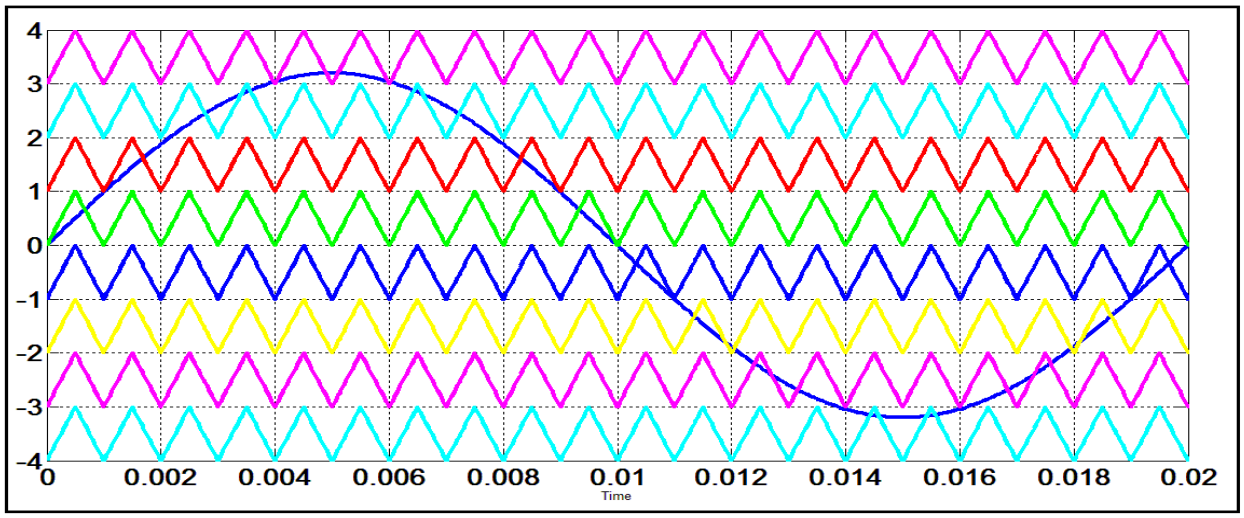


Fig. 9 SPWM switching for nine level conventional cascaded H bridge MLI

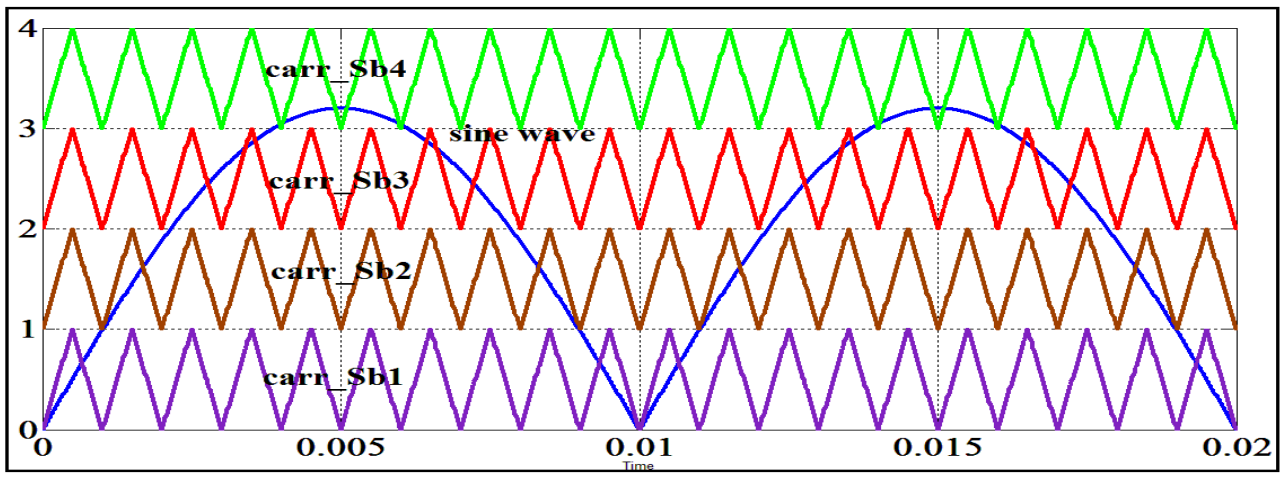


Fig. 10 SPWM switching for nine level cascaded half-bridge MLDCLI

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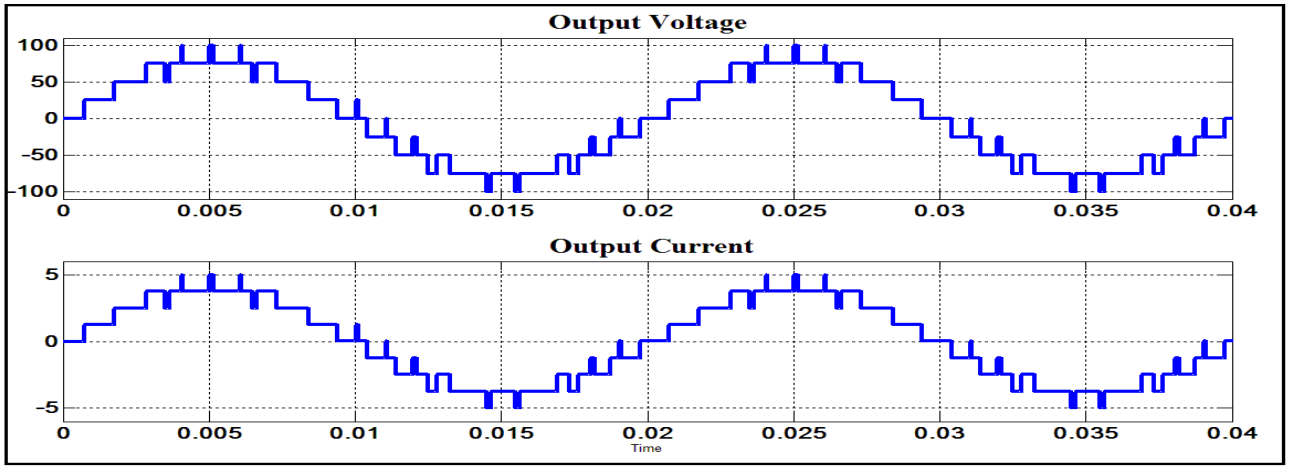


Fig. 11 Output voltage and current for nine level conventional cascaded H bridge MLI with SPWM switching

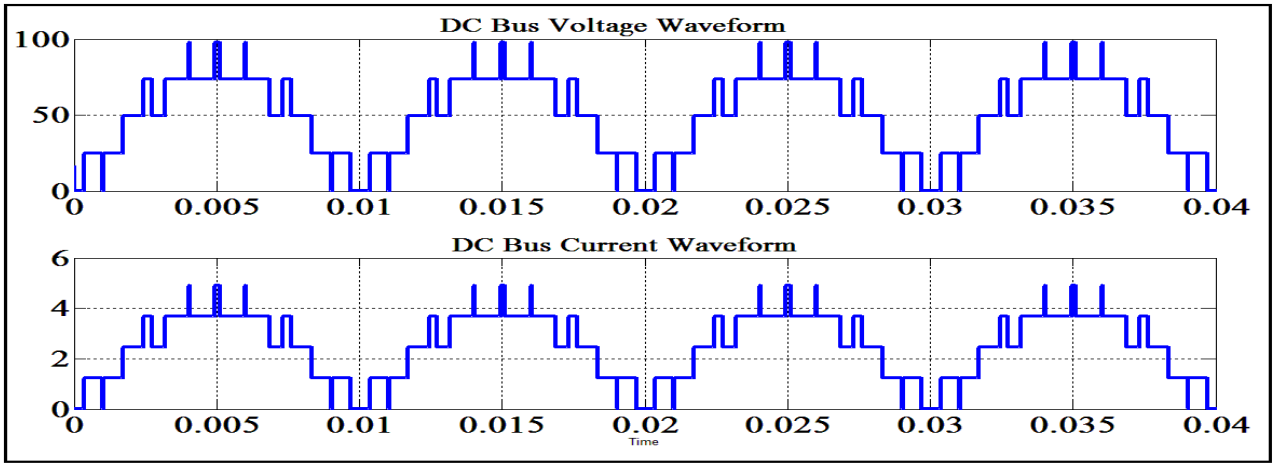


Fig. 12 DC bus voltage and current for nine level cascaded half-bridge MLDCLI with SPWM switching

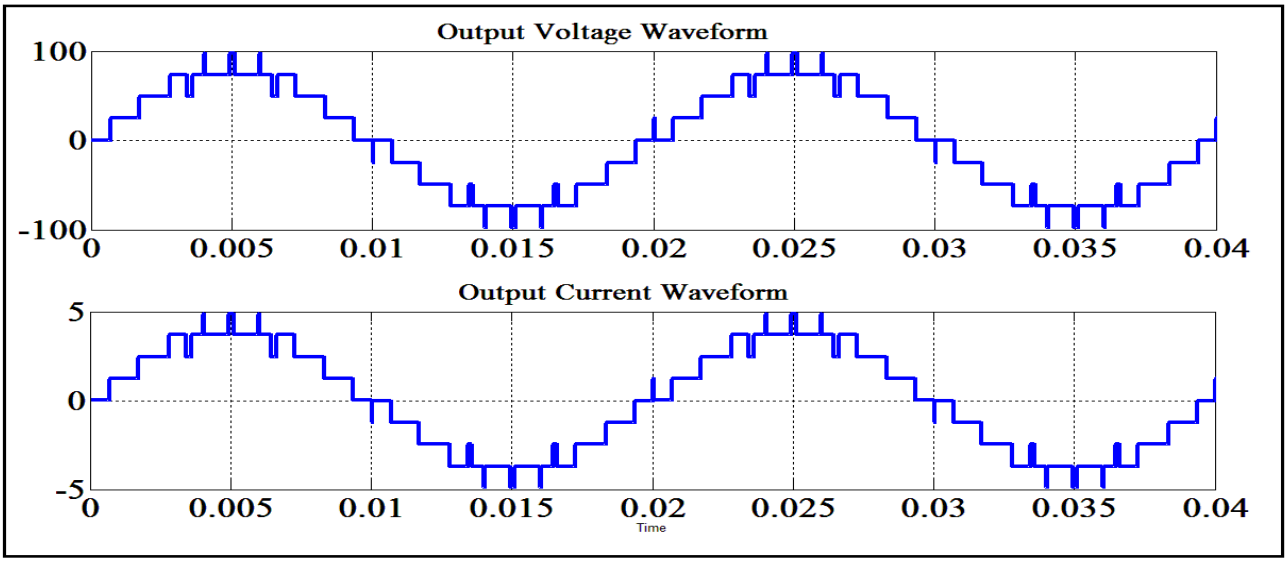


Fig. 13 Output voltage and current for nine level cascaded half-bridge MLDCLI with SPWM switching

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TABLE II: COMPARISON OF CONVENTIONAL MLI AND MLDCLI FOR SQUARE WAVE SWITCHING SCHEME

PARAMETER	CONVENTIONAL NINE LEVEL CASCADED H BRIDGE MLI	NINE LEVEL CASCADED HALF-BRIDGE MLDCLI
No. Of Switches	2(m-1) = 16	m+3 = 12
No. Of Independent Gate Triggering Circuit	8	5
No. of Voltage Sources	(m-1)/2 = 4	(m-1)/2 = 4
THD	22.05%	22.05%
Switch Voltage (Max)	25V	100V(SPFB) and 25V (for each cell switch)
Switch Current (Max)	+/- 5A	+/- 5A
Fundamental Output Voltage	61.21V	61.21V
Fundamental Output Current	3.061A	3.061A

TABLE III COMPARISON OF CONVENTIONAL MLI AND MLDCLI FOR SPWM SWITCHING SCHEME

PARAMETER	CONVENTIONAL NINE LEVEL CASCADED H BRIDGE MLI	NINE LEVEL CASCADED HALF-BRIDGE MLDCLI
No. Of Switches	2(m-1) = 16	m+3 = 12
No. Of Independent Gate Triggering Circuit	8	5
No. of Voltage Sources	(m-1)/2 = 4	(m-1)/2 = 4
THD	16.4%	15.4%
Switch Voltage (Max)	25V	100V(SPFB) and 25V (for each cell switch)
Switch Current (Max)	+/- 5A	+/- 5A
Fundamental Output Voltage	57.23V	56.72V
Fundamental Output Current	2.862A	2.862A

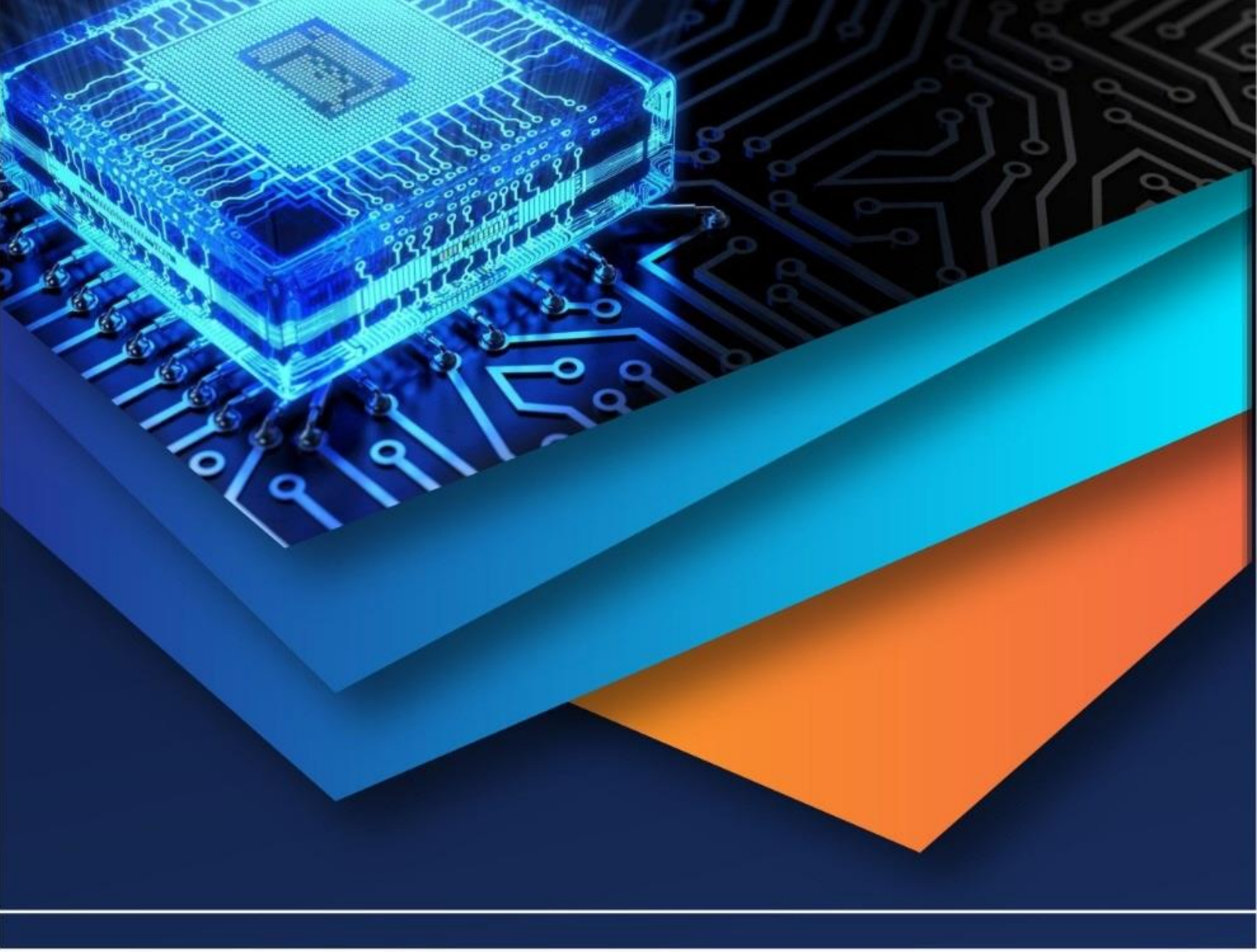
IV. CONCLUSIONS

The MLDCLI can achieve the same output as that of conventional MLI with reduced number of switches but a slight increase in VA/V rating of the switches. The cost of switches increases with increase in rating. Even though the rating is high for MLDCLI it has less number of switches and gate drive circuits, fewer assembly steps, more compact design which leads to overall economic savings. SPWM switching scheme requires more triangular number of carriers hence more computational complexity in conventional MLI as compared to MLDCLI. For both MLDCLI and conventional MLI the output THD is lesser than square wave switching scheme hence filtering requirement is less, thus reducing the values of bulky filters. LC or LCL type filters can be used for producing a sinusoidal output waveform at the inverter output. With advanced types of semiconductor switches, MLDCLI promises a better future and a very attractive option for high power applications.

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