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Current Mirror using FinFETs

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Abstract: ***In this paper basic current mirror circuit is implemented using FinFETs and conventional MOSFETs. Simulation results of Current mirror using MOSFETs & FinFETs have been compared on the basis of few important parameters and hence concluded FinFET as a better device. The performance of FinFET based current mirror is optimised by using very low voltage of 0.5 volts as supply voltage as compared to 1.8 volts for Mosfets. The size of FinFET is very small with gate length of just 7nm, hence occupying less area on chip. This review paper presents a comparative performance study of basic current mirror with two different devices. Hspice software is used for the research work.***
Keywords: Current mirror, FinFET, Compliance voltage

I. INTRODUCTION

Moore's law has validated the scaling of CMOS technologies over the past several decades. However planar transistor scaling below sub micrometer CMOS technology has reached its limits around sub-22-nm nodes, due to very poor electrostatic integrity, which is illustrated as degraded short-channel behavior and high leakage current [1][2].

FETs with multiple gates eliminate these problems because of tighter control of the channel potential by more gates wrapped around the body [3]. Amongst all multigate FETs, FinFETs have emerged as the best alternative from a fabrication perspective [4][5][6].

The main limitations of using CMOS transistors are high power dissipation and high leakage current. As technology advances, the devices are scaled down. Scaling causes severe problems like high sub-threshold slope & DIBL which are difficult to suppress and are overcome by the use of FinFET. Since FinFET provides high Ion/Ioff ratio, the characteristics of the device are improved. So, our aim is to use FinFET in Current Mirrors and study their characteristics and parameters. The problem refers to improve the parameters of Current Mirror circuit using FinFETs.

For designing analog integrated circuit, the most popular technique used is the current mirror. So, in this method, designing of the circuit can be done to copy the flow of current throughout one active device to another including the ability to control the current. Here, the flow of current can be duplicated in the form of inverting from device to device. Once the flow of current within the first active device is changed then the reflected output current from the other active device will also be varied. Therefore, the current mirror circuit is often referred to as a CCCS (Current Controlled Current Source).

II. THEORY OF FINFETS

Moore's FinFETs are widely used in today's electronics equipment due to its higher current output per voltage input as compared to MOSFETs. Additionally, the leakage current is lesser than that of MOSFETs [1]. These devices gained importance after 2001 when it was found that they have low power consumption for its operation over other devices. The FinFET device structure comprises of a silicon fin covered by shorted or independent gates on both sides of the fin, typically on a silicon-on-insulator substrate. In the SG mode of operation, the two gates are biased together to activate the device, providing with maximum gate drive. As devices get smaller further and further, the problem with conventional MOSFETs is increasing [2]. We can see short channel effects problems such as VT roll off, drain induced barrier lowering (DIBL), increasing leakage current and many more. To solve the problem several MOSFET has been introduced such as double gate, FinFET, Tri-gate, Fore-gate, all around gate [1][8] and so on. The electrostatic characteristic of FinFET such as current – voltage graph has been discussed. The distinct characteristic of the FinFET is that the conducting channel is covered by a thin Si "fin", that forms the gate of the device. The width of the fin (measured from source to drain) decides the effective channel length of the device. It is very important to know the characteristics of MOSFET to function efficiently, from this aspect we tried to discuss the qualitative feature of FinFET characteristics [2]. The FinFET model used in this research consists of a vertical Silicon fin controlled by self-aligned double gate.

The mathematical calculations related to FinFET are as shown below.

Linear region: It is the region in which Ids increases in a linear fashion with Vds, for a given Vgs > Vth.

Ids, in the linear region is given by:

$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V^2{}_{DS}] \quad \text{.....(1)}$$

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Where μn is mobility of the charge carriers in the channel (inversion) region, Cox is the gate oxide capacitance per unit area, W/L is device width to length ratio and Vth is threshold voltage.

Saturation Region: In this region Ids does not increase as Vds increases. Ids in the saturation region is given by:

$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \quad \text{.....(2)}$$

A. FinFET Model Used in this Research

The main advantage of the FinFET is the ability to significantly reduce the short channel effects. BSIM-CMG FinFET model is used to solve the issue of leakage current, power dissipation and speed observed in conventional MOSFET. The tied gate FinFET model used for the research is LUT_Dev1 & its specification is as follows:

1) Physical gate length = 7nm
2) Oxide thickness = 1.09nm (front and back)
3) Body thickness = 2.725nm
4) Fin height = 10.9nm
5) Source/drain doping = 1e20 /cm3
6) Source-side under lap = 1.09nm
7) Drain-side under lap = 1.09nm

B. Basic Mosfet Current Mirror

The basic current mirror can be implemented using MOSFETs (Fig: 1). Transistor M1 is working in the saturation or active mode, and so is M2. In this setup, the output current IOUT is directly proportional to IREF, as discussed next. Simulation results for Iout vs VDS curve for Basic Current Mirror is shown in fig 2. For a current mirror, neglecting channel length modulation:

$I_{out} = ½ \mu_n C_{ox} (W/L)_2 (V_{gs} - V_{th})^2$..... (1)
$I_{ref} = ½ \mu_n C_{ox} (W/L)_1 (V_{gs} - V_{th})^2$..... (2)
When eq.1 is divided by eq.2, we have $I_{out} = I_{ref} (W/L)_2 /(W/L)_1$

Limitations

1) As we can observe from the basic current mirror circuit that the current gain is poor and the output current is affected by channel length modulation. This is verified in eq. 3.

$$I_{OUT} = I_{REF} \frac{(W/L)_2 (1 + \lambda V_{DS2})}{(W/L)_1 (1 + \lambda V_{DS1})} \quad \text{.....(3)}$$

Here $V_{ds1} \neq V_{ds2}$

2) Output resistance is finite and small value.

III.METHODOLOGY

A basic current mirror using 2 mosfets and a resistor as shown in figure is simulated in Hspice software. The power supply of Vdd of 1.8V is used. The graph of Iout vs Vds is plotted. From the simulated graph we can observe the curve of Iout gradually rising towards the Iref value and at one point meets the Iref constant line.

The point of corresponding value of voltage at which Iout meets Iref is called the compliance voltage. It means the minimum value of voltage need to be maintained at the drain terminal of Mosfet 2 so that Iout=Iref. The main aim of current mirror of copying the current is fulfilled only at the instant when compliance voltage is achieved. The compliance voltage of current mirror using mosfet is 0.57volts. The Mosfet 1 has to be in saturation mode of operation and hence is in diode connected fashion i.e., drain and gate of mosfet M1 are shorted.M2 operates in linear mode. Dummy voltage V2 voltage varied from 0volts to 1.8volts (vdd) in steps of 0.01volts to get the output graph.

Similarly, A basic current mirror using 2 FinFETs and a resistor is simulated in Hspice software and compliance voltage required is of only 0.32volts which is far less than current mirror using mosfet.

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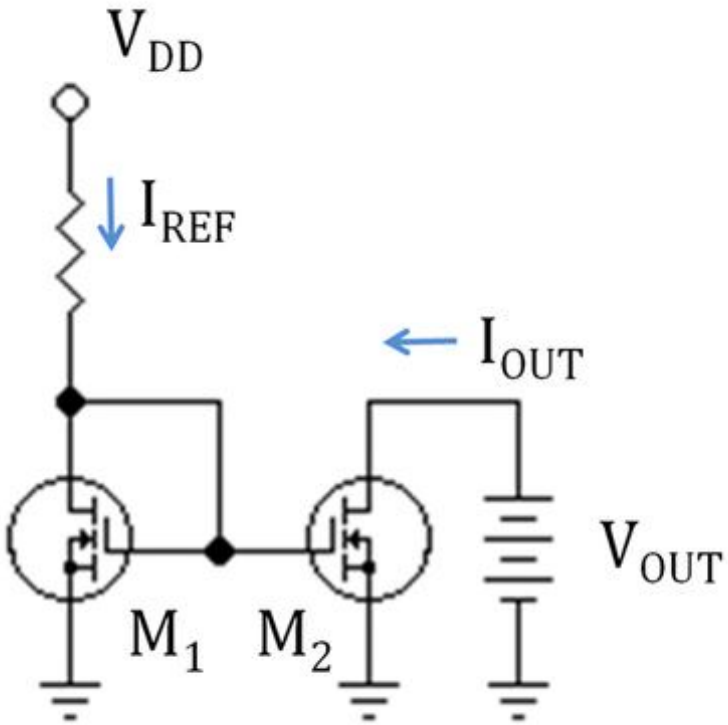

Fig. 1 Basic Current Mirror Circuit Using MOSFETs

IV. SIMULATION RESULT OF CURRENT MIRROR USING MOSFETS

A. *Simulated Graph*

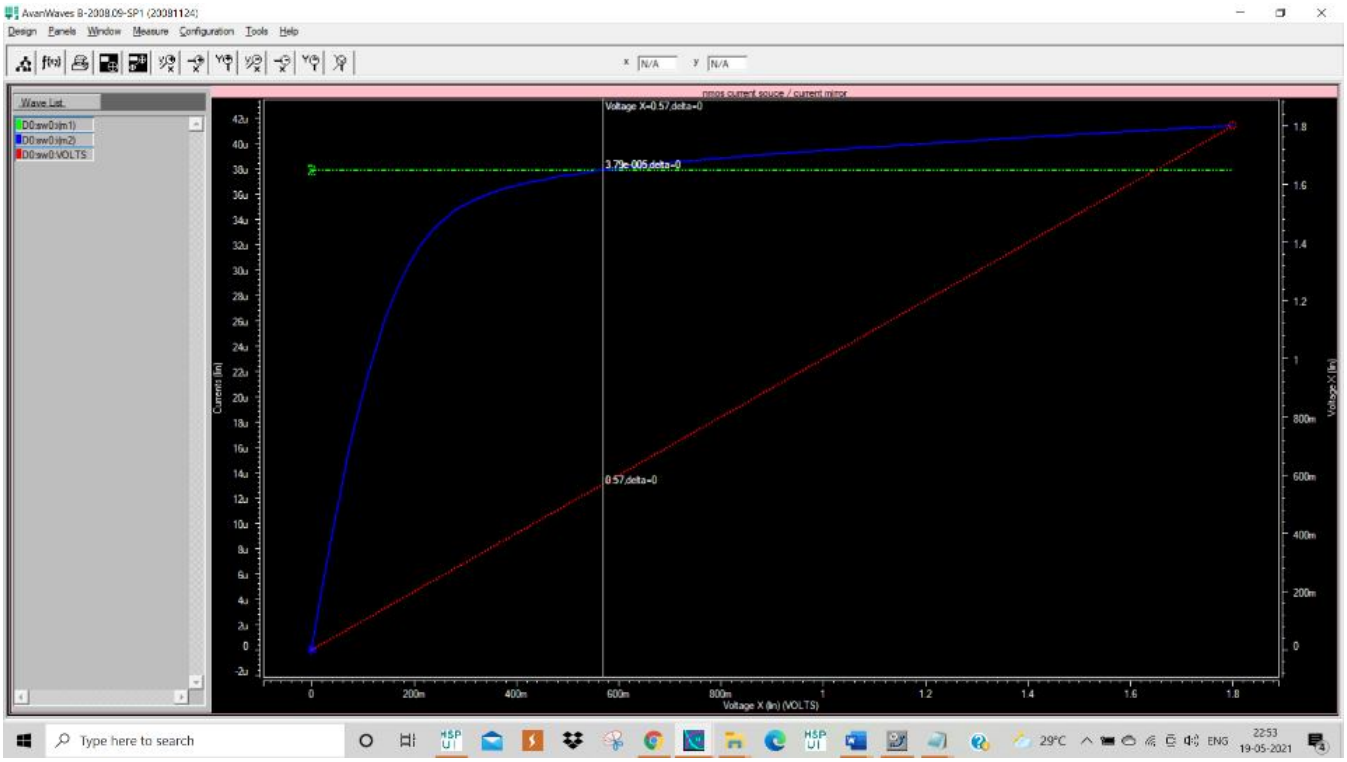

Fig. 2 Simulated graph of Iout vs Vds curve for Current Mirror using MOSFETs

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B. Table

Table 1 Parameters of Basic Current Mirror using MOSFETs

Parameters	MOSFET
Length of the channel	L = 3.6e-007 metre
Width of the channel	W=0.7um
Aspect Ratio	1.944
Minimum Drain voltage required (Vdd)	1.8 volts
Compliance voltage	0.57 volts
Total Voltage source power dissipation	68.1333 uwatts
Output current	37.8518uA
Maximum mirrored constant current	37.8518uA
Average power dissipation	109.0164e-06 watts
Total power dissipation	68.1335e-06 watts
Leakage power dissipation	34.0668e-12 watts
Voltage drop	1.2302 volts

C. Advantages

The main benefit of the MOSFET version is that FETs draw zero gate current. This means that no effort need be put in allowing for small extra currents in different parts of the current mirror circuit. Moreover, it is easy to manufacture MOSFETs on the same IC die with various channel widths or lengths. The aspect ratio controls how much current will flow through that channel, so we can make mirror circuits that provide multiples or sub-multiples of the reference current.

D. Disadvantages

As we can observe from the basic current mirror circuit current gain is less and the output current is affected by channel length modulation parameter. This can be cross checked in by equation below

$$I_{OUT} = I_{REF} \frac{(W/L)_2(1 + \lambda V_{DS2})}{(W/L)_1(1 + \lambda V_{DS1})}$$

Here $V_{ds1} \neq V_{ds2}$

V. SIMULATION RESULT OF CURRENT MIRROR USING FINFETS

A. Simulated Graph

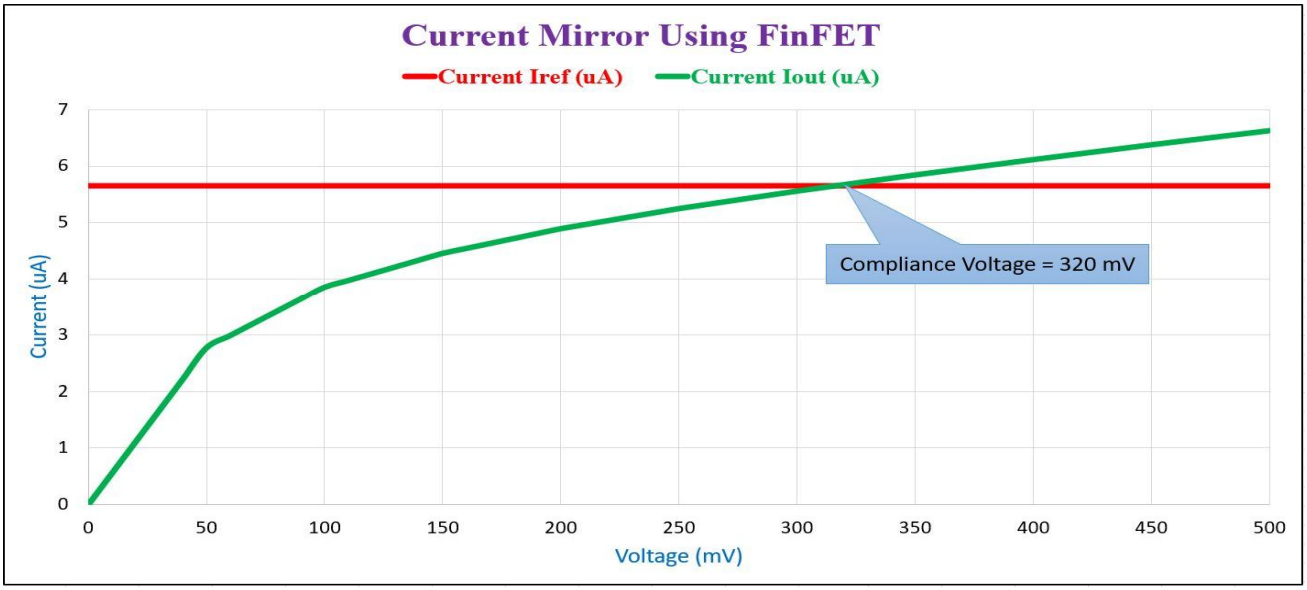

Fig. 3 Simulated graph of Iout vs Vds curve for Current Mirror using FinFETs

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B. Table

Table 2 Parameters of Basic Current Mirror using FinFETs

Parameters	FINFET
Length of the channel	7.0 e-009 metre
Width of the channel	W=24.525nm
Aspect Ratio	3.5
Minimum Drain voltage required (Vdd)	0.5 volts
Compliance voltage	0.32 volts
Total Voltage source power dissipation	2.8258 uwatts
Output current	10.1503pA
Maximum mirrored constant current	5.6515uA
Average power dissipation	1.038e-06 watts
Total power dissipation	2.826e-06 watts
Leakage power dissipation	1.413e-12 watts
Voltage drop	183.6752 mvolts

C. Advantages

The use of FinFETs in current mirror circuits will reduce the power dissipation and size of the circuit. Also, the current drawn will be less as compared to current mirror using MOSFETs.

D. Disadvantages

The output current of basic current mirror circuit using FinFETs has channel length modulation effects which can be eliminated using Cascode current mirror circuit which is the future scope of the research work.

VI. COMPARISON OF CURRENT MIRRORS

Table 3 Comparison of parameters of Basic Current Mirror circuit using MOSFETs and FinFETs

Parameters	MOSFET	FINFET
Length of the channel	L = 3.6e-007 metre	7.0 e-009 metre
Width of the channel	W=0.7um	W=24.525nm
Aspect Ratio	1.944	3.5
Minimum Drain voltage required (Vdd)	1.8 volts	0.5 volts
Compliance voltage	0.57 volts	0.32 volts
Total Voltage source power dissipation	68.1333 uwatts	2.8258 uwatts
Output current	37.8518uA	10.1503pA
Maximum mirrored constant current	37.8518uA	5.6515uA
Average power dissipation	109.0164e-06 watts	1.038e-06 watts
Total power dissipation	68.1335e-06 watts	2.826e-06 watts
Leakage power dissipation	34.0668e-12 watts	1.413e-12 watts
Voltage drop	1.2302 volts	183.6752 mvolts

VII. RESULTS AND DISCUSSION

As the size of the FINFET device itself is less, the size of overall circuit is also less. This increases the chip density and makes the system compact. The aspect ratio of current mirror circuit using FINFET is good enough as compared to that of current mirror circuits using MOSFETs. The compliance voltage, i.e., the minimum amount of voltage required to make output current equal to reference current is less. Also, the supply voltage required for FINFET based circuits is less and hence the power dissipation and voltage drop are also less.

VIII. APPLICATIONS

The current mirror is used to supply bias currents and active loads to circuits. It can also be used to model a more ideal current source. The required amount of current can be achieved by varying the aspect ratio of the FETs.

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IX. FUTURE SCOPE

Understanding the drawbacks of basic current mirror circuits, it can be improvised by using Cascode current mirror circuit and Wilson current mirror circuits which will be the future scope of the research. We can further improve the performance of current mirror circuit using Low voltage self cascode current mirror.

X. CONCLUSION

Thus, observing Table 3 Comparison of current mirrors using MOSFETs and FinFETs and knowing the advantages of FinFETs we conclude that current mirror using FinFETs is better than current mirror using MOSFETs.

XI. ACKNOWLEDGEMENT

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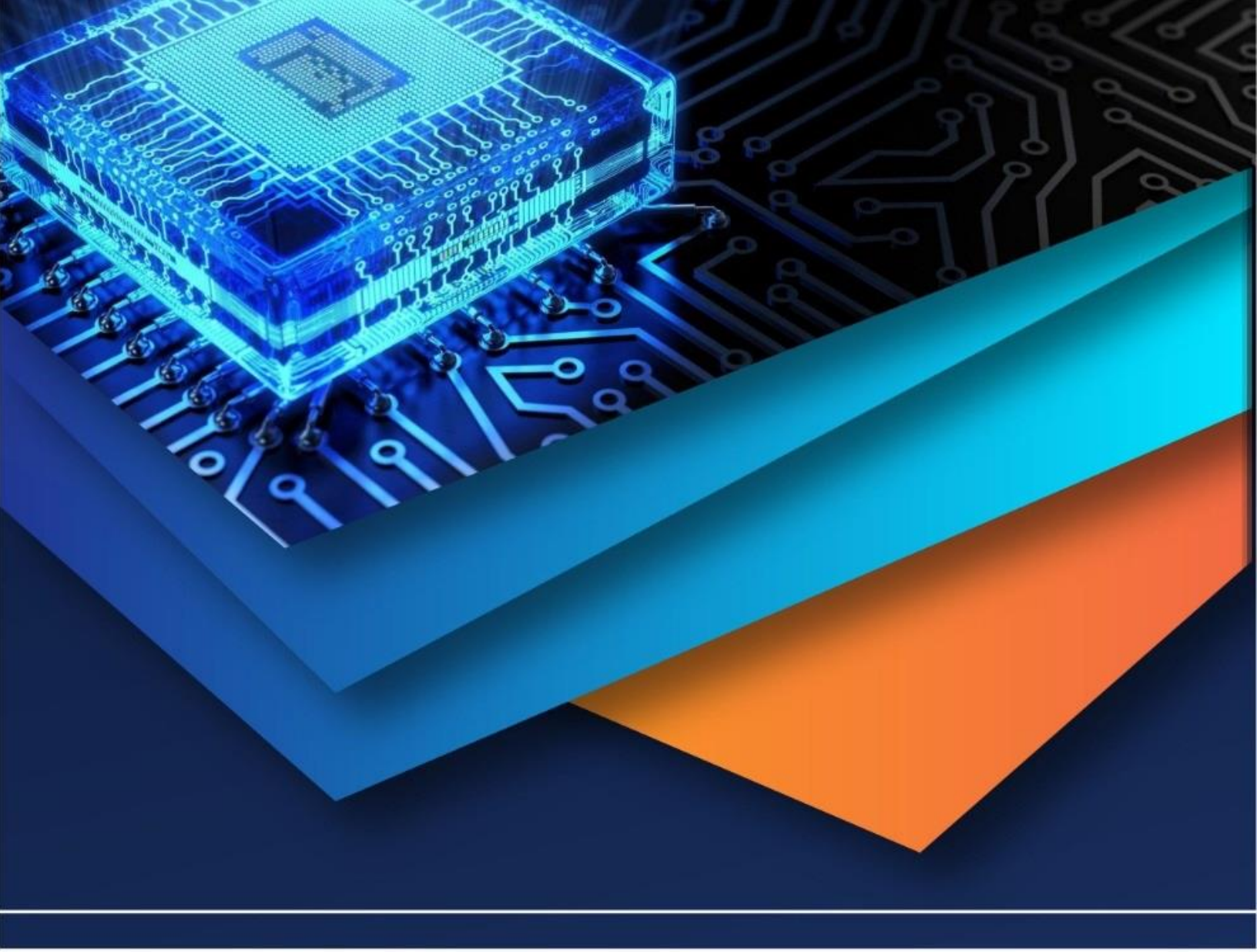

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