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Leakage Power Reduction in CMOS VLSI Circuits using Advance Leakage Reduction Method

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Abstract: ***Recently, consumption of power is key problem of logic circuits based on Very Large Scale Integration. More potentiality consumption isn't considered an appropriate for storage cell life for the use in cell operations and changes parameters such as optimality, efficiency etc, more consumption of power also provides for minimization of cell storage cycle. In present scenario static consumption of power is major troubles in logic circuits based on CMOS. Layout of drainage less circuit is typically complex. Several derived methods for minimization of consumption of potentiality for logic circuits based on CMOS. For this research paper, a technique called Advance Leakage reduction (AL reduction) is proposed to reduce the leakage power in CMOS logic circuits. To draw our structure circuit related to CMOS like Inverter, inverted AND, and NOR etc. we have seen the power and delay for circuits. Thispaper incorporates, analyzing of several minimization techniques as compared with proposed work to illustrate minimization in ratio of energy and time usage and time duration for propagation. LECTOR, Source biasing, Stack ONOFIC method is observed and analyzed with the proposed method to evaluate the leakage power consumption and propagation delay for logic circuits based on CMOS. Entire work has done in LT Spice Software with 180nm library of CMOS.***
Keywords: VLSI; Delay; Potentiality; AL reduction

I. INTRODUCTION

As we see the past duration of time, various electronic gadgets have achieved drastic development because of higher demand of them in the electronics industry. The new advancement for those movable gadget consist better enforcement and decreasing energy consumption like in laptops ,mac book and mobile devices.. For the good consummation of automated Very Large Scale Integrated systems such as microcontroller, processors, and other aspects, high power consumption is a serious issue. And also saves greater power by reducing static current [1].The relation between subthreshold current and V_{th} is inverse in nature i.e. if we decrease $V_{th.}$ At a particular value there is an exponential rise in subthreshold current, $V_{th.}$ Of a short channel MOS also decreases along with V_{ds} rise [2]. To overcome the delay degradation, threshold voltage (V_T) is to be reduced. Reduction in threshold voltage causes an exponential increase in sub-threshold leakage current. As one continues to scale down supply voltage and threshold voltage, the increased leakage power can dominate the dynamic switching power [3] .

The well-known method to achieve reduced leakage power in inverters makes use of transistor stacking[4].The static power dissipation due to sub threshold leakage currents, tunneling of electrons etc[5]. For parallel connected MOS transistors the DC current is estimated as the sum of the currents of each parallel connected transistor[6]. In case of series connected transistors leakage current calculation is typical due to its nonlinear characteristics[7,8].

For the fabrication of CMOS circuit, the product of length and width, power usage and time of propagation are the vital parameters. Nowadays, complementary metal oxide semiconductor (CMOS) circuit size minimized at very advanced level for enhancement of VLSI products[9]. Static power is the major parameter in manufacturing of hardware and software processing units[10]. The leakage part of current rise exponentially and diminished the physical parameters. , the leakage reduction can be achieved by controlling the dimensions such as Length of the Channel, Oxide Thickness, Junction Depth and Doping profile in a transistor. During active low input mode, each sleeper parallel with stacked transistors are turn off, which suppress the leakage current while saving the state [11, 12]. As per the ITRS mainly, power reduction is controlled via static potentiality. We proposed initially, discussion of static power reduction strategy ,previously for logic circuits based on CMOS. In this work a technique is proposed called AL reduction.

The rest part of this work is configured such as, in second part we have discussed about different static power techniques. Further, we are giving our proposed technique, after broad literature survey after this we have discussed our results which are based on this proposed work. At the end of this paper, conclusion drawn from this proposed techniques and its parameter analysis is mentioned here.

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II. RELATED WORK

A. LECTOR Technique

This technique involves two transistors for leakage control and sandwiched between PUN and PDN. The gate of both transistors is changed by the sources of each other. Stacking effect of both transistors between the ground and supply is the key point of this method for the drainage minimization. .The LECTOR method is shown by figure 1. Fundamental idea of LECTOR method is static potentiality shrinkage by inserting these NMOS sandwiched in PUN -PDN. For our research study we opt LECTOR method to various logic circuits based on CMOS and result that this static minimization technique the consumption of potentiality with respect to basic ancient technique and results, table depicts that this technique restored better result and static power is diminished.

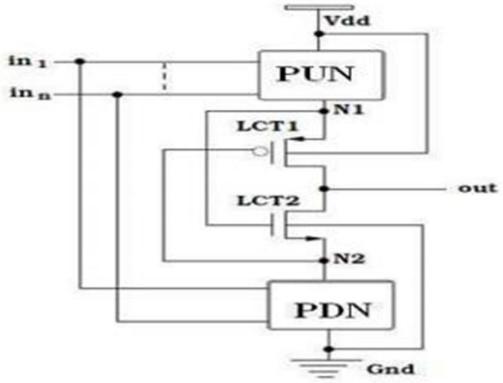

Fig. 1 Diagram of LECTOR technique

B. Source Biasing Method

Our basic objective to use this method i.e. increment in Vs of transistor by reducing static current which helps us to reduce leakage power reduction to fulfill our objective. The relation between subthreshold current and V_{th} is inverse in nature i.e. if we decrease $V_{th.}$ At a particular value there is an exponential rise in subthreshold current.Decrement in V_{ds} is done by increment in MOS source station voltage also known as source biasing. To implement this method CMOS inverter is taken.

When we applied '0' as input both NMOS will turn off and '1' as output .One more transistor of P type MOS i.e. PM2 as shown in figure 2.is kept in cut off mode as it delivers static current and creates an amount of potential of a particular value at the primary terminal i.e. source in addition to PMOS,NMOS is also used labeled as NM2 which directly connect to the static current supplied by previous transistor.

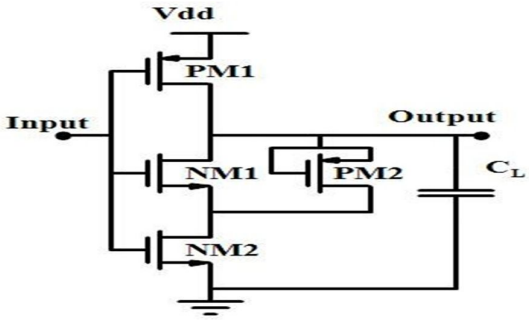

Fig. 2 Diagram of Source Biasing technique

C. Stack ONOFIC technique

As the name suggests there is a stacking of transistors is done by this method to reduce the static power. The right side PMOS is joined via gate of twoNMOS, gate terminal of PMOS(M6) is joined to the output. This method provides the large resistance when operated in OFF condition and small resistance when operated in ON condition. It changes the power consumption and delay of propagation of whole CMOS circuit

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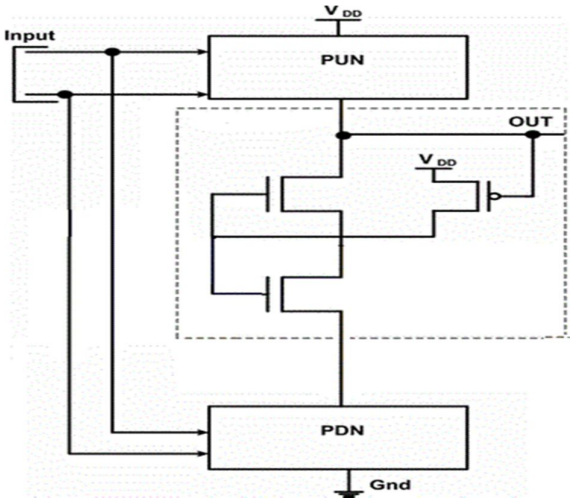


Fig. 3 Diagram of Stack ONOFIC technique

III. PROPOSED WORK

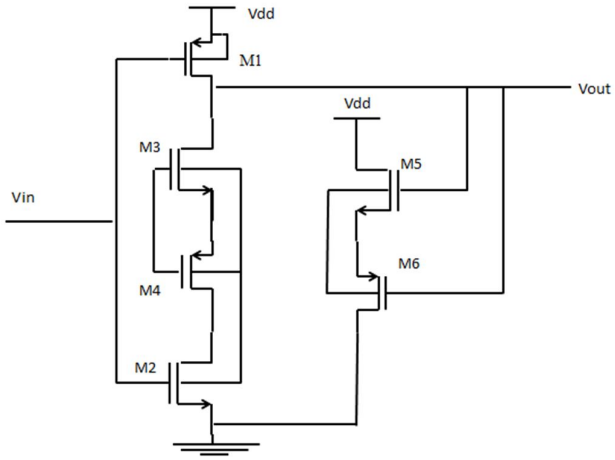


Fig. 4 CMOS inverter using Proposed Technique

In this technique two transistors one NMOS (M3) and other is NMOS (M4) is inserted between pull up and pull down networks. The substrate parts of NMOS (M3), PMOS (M4) and pull down network's transistor (M2) are connected with each other. Also we have taken two more transistors one NMOS(M5) and one PMOS(M6) at the right side of the circuit which has described above .The substrates of these transistors are interconnected and gates are connected to the output .The source of PMOS(M6) is connected to the ground. By applying this technique we obtained a very large reduction in the leakage power of the CMOS circuits. The CMOS inverter is proposed using this technique and we have also drawn results for NOR and NAND gates.

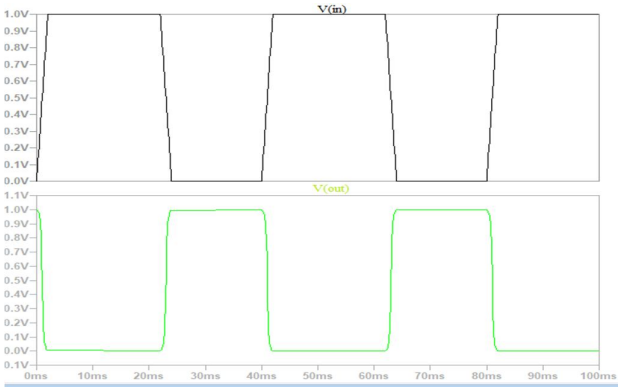


Fig. 4 CMOS inverter Waveforms

IV. RESULT AND DISCUSSION

On simulating the logic circuits based on CMOS , using 180nm technologies in LT Spice Tool and obtained the ststic power in nW. The leakage power is reduced by 50% by this technique. We have taken supply voltage Vdd=1.8V.(length)L=180nm,(width)W=360nm.And finally observe the operating point analysis.

Figure 5 shows the plot of leakage power dissipation for below tabular data using 180nm technologies.

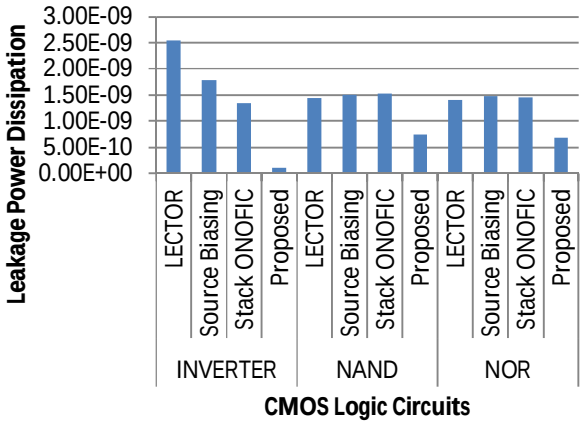


Figure 6 shows the plot of delay for below tabular data using 180nm technologies.

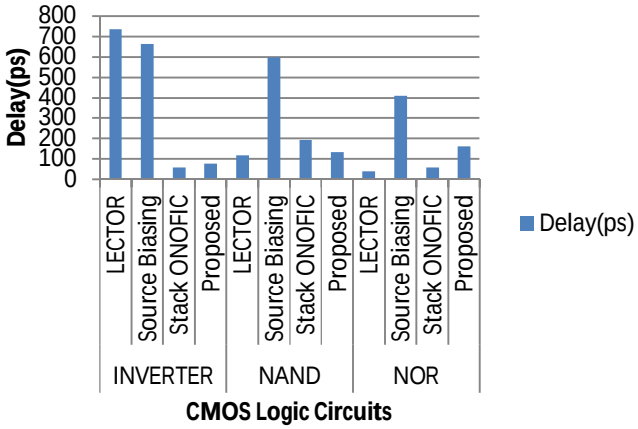


Table illustrates the static power consumption for logic circuits based on CMOS using 180nm technologies.

CMOS circuit	Use Technique	Consumption of Leakage Power(watts)	Propagation time(ps)
INVERTER	LECTOR	2.54E-09	736.781
	Source Biasing	1.78E-09	661.414
	Stack ONOFIC	1.34E-09	57.388
	Proposed	1.12E-10	76.3
NAND	LECTOR	1.45E-09	117.14
	Source	1.50E-09	597.293

	Biasing		
	Stack ONOFIC	1.53E-09	192.931
	Proposed	7.46E-10	132.23
NOR	LECTOR	1.40E-09	40.723
	Source Biasing	1.48E-09	410.01
	Stack ONOFIC	1.46E-09	57.388
	Proposed	6.86E-10	162.456

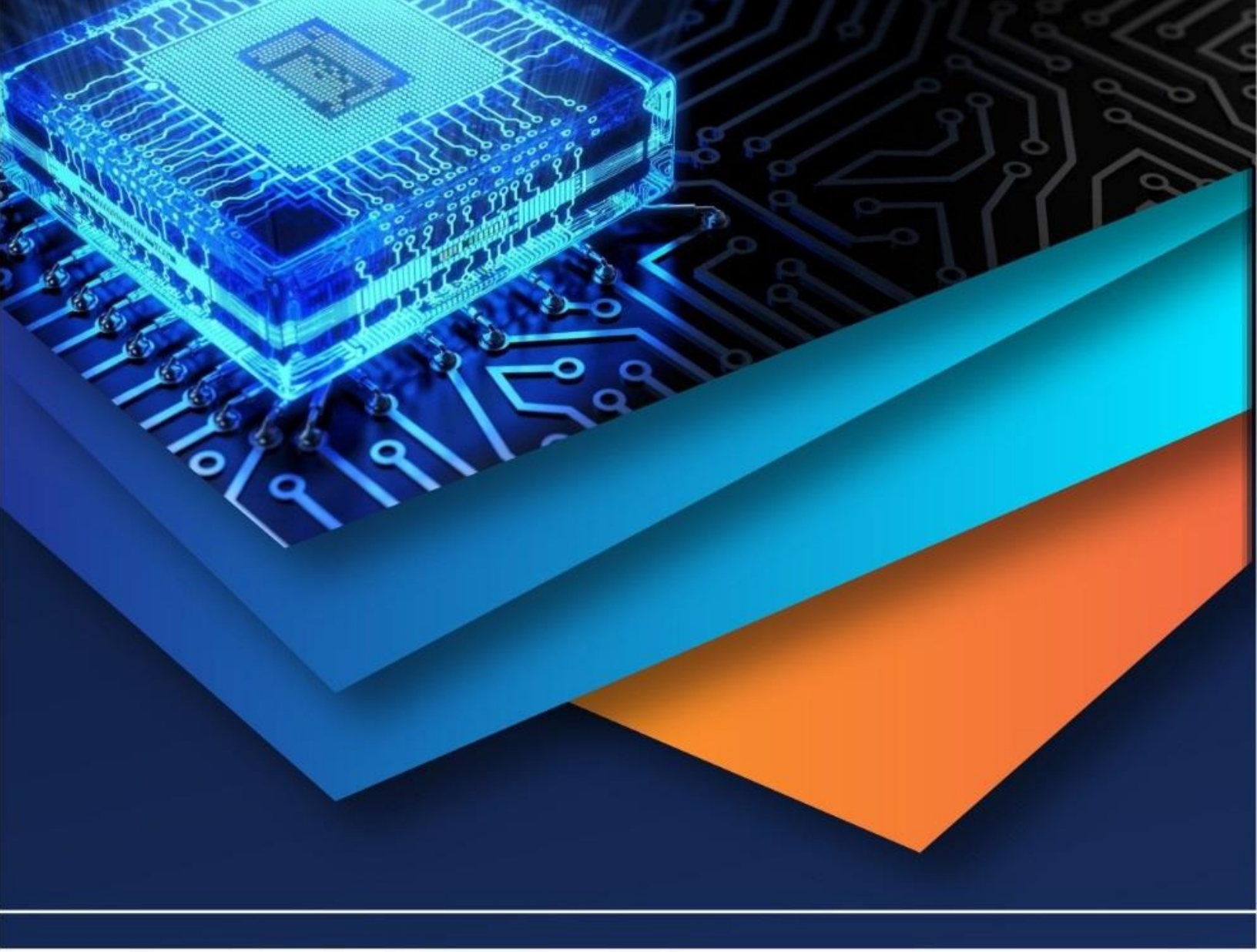
With the help of table it is observed that the powerdissipation (180 nm) in all CMOS logic circuits. By using this proposed technique the propagation delay also is reduced.

V. CONCLUSION

The static power is one of the most vital factors in the logic circuits based on CMOS . This AL reduction method produced minimized static power. The overall power consumption will also be less as the leakage power goes down The results are produced by LT Spice software with respect to logic circuits based on CMOS. It saved the power wastage of circuits as we observed. At the end we can concluded that with this technique static power and propagation delay will be reduced significantly.

REFERENCES

[1] Chanchal Kumar et.al, “Leakage power reduction in CMOS logic circuits using stack onofic technique”, ICICCS, 2018.
[2] Venkata Ramakrishna Nandyala and Kamala Kanta Mahapatra, “A circuit technique for leakage power reduction in CMOS VLSI circuits”, VLSI-SATA, 2016.
[3] Narender Hanchate, “LECTOR:A technique for leakage reduction in CMOS circuits”, IEEE transactions on VLSI systems, 2004.
[4] Preeti Verma and R.A. Mishra, “Leakage power and delay analysis of LECTOR based circuits”, ICCCT, 2011.
[5] Sreekala K.S and S.Krishnakumar, “Subthreshold leakage power reduction by feedback sleeper stack technique”, ICETT, 2016.
[6] A. Rjoub and M. Al-Ajlouni,” Efficient multi-threshold voltage techniques for minimum leakage current in nanoscale technology,” Int. J. Circuit Theory Appl., vol. 39, 1049, 2011.
[7] Dr. B.T. Geetha,et.al, “ Design Methodologies and Circuit Optimization Techniques for Low PowerCMOS VLSI Design”, ICPCSI, 2017.
[8] V. K. Bharathi and T. S. Reddy,” A Comprehensive Study on Power Reduction Techniques in Deep Submicron Technologies,” International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 4, no. 12, pp. 9639-9644, 2015.
[9] V. K. Sharma, S. Patel and M. Pattanaik,” High Performance Process Variations Aware Technique for Sub- threshold 8T-SRAM Cell,” Wireless Pers. Commun., vol. 78, 57, 2014.
[10] M. S. Islam, M. S. Nasrin, N. Mansur and N. Tasneem,” Dual Stack Method: A Novel Approach to Low Leakage and Speed Power Product VLSI Design,” IEEE Int. Conf. Electr. Comp. Eng. 2010.
[11] Marc Belleville, Olivier Thomas, Alexandre Valentian and Fabien Clermidy,” Designing digital circuits with nano- scale devices: challenges and opportunities,” Solid-State Electronics, vol. 84, pp. 38-45, June 2013.
[12] V.K. Sharma, M. Pattanaik and B. Raj,” ONOFIC approach: low power high speed nanoscale VLSI circuits design,” International Journal of Electronics, Vol. 101, no. 1, pp. 61-73, 2014.



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